IDT®
Migrating from the PLX PCI 6150-BB66B to the Tsi350™ PCI-to-PCI Bridge

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1. Migrating from the PLX PCI 6150-BB66B to the Tsi350 PCI-to-PCI Bridge

This document provides information that helps system designers migrate from the PLX PCI 6150-BB66B to the IDT Tsi350. The following topics are discussed:

1.1 Overview

The Tsi350 is pin out and package compatible with the PLX PCI 6150-BB66B (PCI 6150) PCI-to-PCI Bridge. The Tsi350 can be used as a drop in replacement for the PLX PCI 6150 without any modifications to the system board provided the PLX device is being used to support the same functionality as the Intel 21150.

The Tsi350 and PCI6150 are available in both a 208-pin PQFP and 256-pin PBGA package with similar mechanical parameters that allow both these chips to be soldered on to a common foot print on the system board.

1.2 Feature Compatibility

1.2.1 208-pin PQFP

The Tsi350 (Tsi350-66CQ and Tsi350-66CQY) and the PCI6150 (PCI6150-BB66PC and PCI6150-BB66PC G) are feature and pinout compatible with the exception that the PLX device supports an EEPROM interface that is not present in the IDT part.

1.2.2 256-pin PBGA

The Tsi350 (Tsi350-66CLVZ1) and the PCI6150 (PCI6150-BB66BC G) are feature and pinout compatible with a few minor exceptions:

- The PLX device supports an EEPROM interface that is not present in the IDT part.
- The PLX device supports PCI Hot Swap and the IDT part does not support PCI Hot Swap.

1.3 Software Compatibility

The Tsi350 and PCI6150 are fully software compatible within the standard PCI configuration space, with the exception of the values returned by the vendor ID, device ID, and revision ID registers.

Refer to the Tsi350 *User Manual* for more information on using device specific features and registers which are outside the standard PCI configuration space.

1.3.1 Vendor ID Register, Offset 0x01 – 0x00

The PCI6150 vendor ID returns 0x3388 when this register is read.

Bits	Type	Reset Value	Description
15:0	R	0x1011	This 16-bit read only field contains the Vendor ID.

1.3.2 Device ID Register, Offset 0x03 – 0x02

The PCI6150 device ID returns 0x0022 when this register is read.

Bits	Type	Value on Reset	Description
15:0	R	0x0023	This 16-bit read only field contains the Device ID.

1.3.3 Revision ID Register, Offset 0x08

The PCI6150 device ID returns 0x04 when this register is read.

Bits	Type	Value on Reset	Description
7:4	R	0x60	This field specifies the Revision ID for the bridge device.

1.4 Pin Compatibility

1.4.1 208-pin PQFP Package

Table 2 shows the differences in the pin list between the two devices as well as any design implications caused by these differences. The pin list is in numerical order.

Table 1: Pin List Differences

Pin#	Tsi350 Pin Name	PLX PCI 6150 Pin Name	Implication
51	VDD	OSCSEL#	None if PLX device is using P_CLKIN to generate S_CLKO[9:0].
54	VSS	OSCIN	None if PLX device is using P_CLKIN to generate S_CLKO[9:0].
103	VDD	EE_EN#	None if EEPROM not used in PLX
106	MS1	EJECT_EN#	None, see Note 1
155	MS0	GPIO3FN#	None, see Note 1
158	VSS	EEPCLK	None if EEPROM not used in PLX
160	VSS	EEPDATA	None if EEPROM not used in PLX

Notes:

1. In Tsi350 if both MS0 and MS1 signals are 0, the device is PCI Hot Swap enabled, synchronous mode (P_CLK used as source for S_CLK_O[9:0]). In the PCI6150, when EJECT_EN# is a 0, it enables PCI Hot Swap capability with GPIO3 functioning as EJECT input. In the PCI6150 when GPIO3FN# is 0, it enables PCI Hot Swap and GPIO3 acts as the Ejector input.

Please see the *Tsi350 User Manual* for complete description of Tsi350 MS0, MS1 input combinations. The Tsi350 is compatible with the PCI6150 under most combinations.

1.4.2 256-pin PBGA Package

Table 2 shows the differences in the pin list between the two devices as well as any design implications caused by these differences. The pin list is in numerical order.

Table 2: Pin List Differences

Pin #	Tsi350 Pin Name	PLX PCI 6150 Pin Name	Implication
B14	MS0	GPIO3FN#	None, see Note 1
C14	VSS	EEPCLK	None if EEPROM interface is not used
C15	VDD	EE_EN#	None if EEPROM interface is not used
D14	VSS	EEPDATA	None if EEPROM interface is not used
J14	Reserved	ENUM#	None, see Note 1
J16	Reserved	PIN_LED/EJECT	None, see Note 1
K15	MSK_IN	OSCIN	None, see Note 2
K16	CONFIG66	OSCSEL#	None, see Note 3
R16	MS1	EJECT_EN#	None, see Note 1

Notes

1. The Tsi350 does not support PCI Hot Swap in this package.
2. The Tsi350 and PCI6150 use different methods to operate the optional asynchronous clocking methodology. If asynchronous clocking is enabled in PLX design the Tsi350 uses MSK_IN as the clock in.
3. The Tsi350 uses the CONFIG66 input to specify it ability to operate at 66MHz. The PCI6150 uses the OSCSEL# input to configure synchronous/asynchronous operation of the secondary clock outputs.