RENESAS

Network Search Engine [R8A20686BG-G]

Control IP Solution

This document is an overview of Renesas Network Search Engine (NSE) Control IP solution.

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1. NSE Control IP Solution

1.1 Introduction

The motivation behind Renesas' NSE control IP development is to provide NSE search solution for network applications.

NSE control IP supports scalable customization from low access to maximum performance to enable high-level programmable network search solutions. In addition, the API provided by Renesas ensures seamless to NSE device, and dynamic reprogrammable search configurations. This solution can certainly help accelerate time to market.
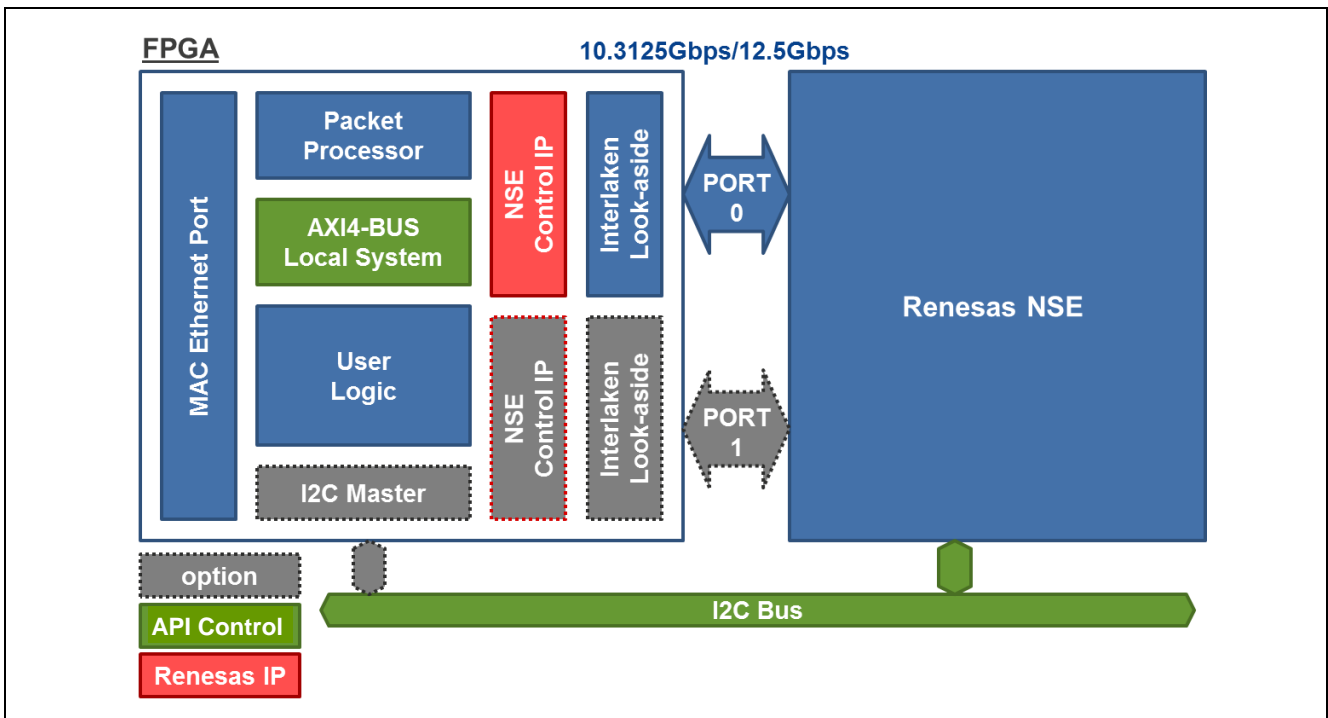

Figure 1   Structure of FPGA + Renesas NSE

1.2　　Target Applications

NSE Control IP Solution's performance and features are suitable for the following applications.

- ✓ Broadband Network Router/Switch
  →Maximum 2 Billion Searches per second

- ✓ L2-L4 Security Control (ACL)
  →Multiple Lookup ports (up to 8 ports) make it possible to search with different configurations.

- ✓ Application Identification
  →Application Identification by using port number search

- ✓ Applicable for SDN
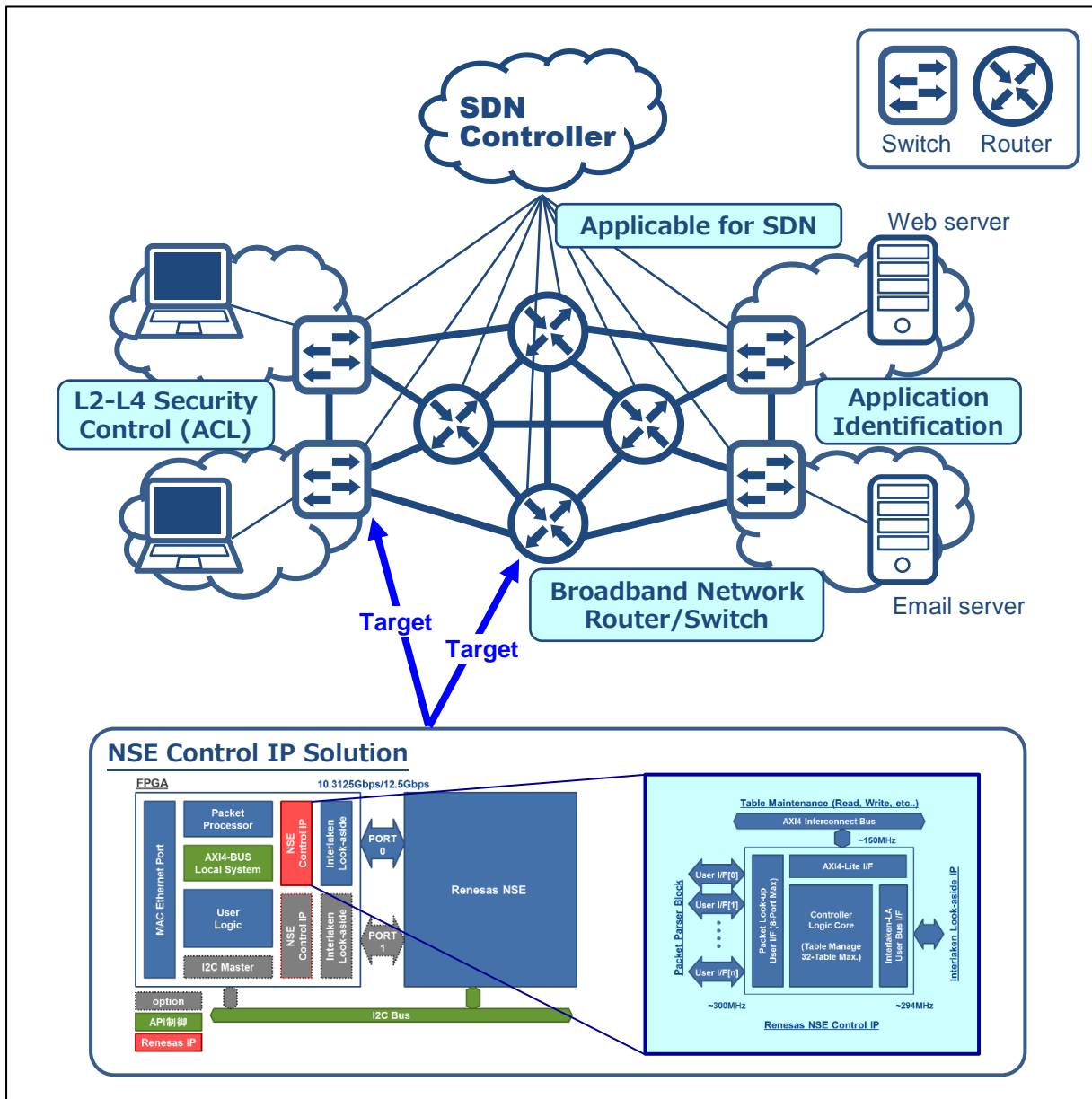 →Search configuration is programmable during search process.

Figure 2　　Target Applications of NSE Control IP Solution

1.3   What's NSE?

The Renesas' NSE [R8A20686BG-G] is a Network Search Engine that provides two high-speed Interlaken Look-Aside ports and two independent memory banks enabling multi-threaded configurations and supports over 1 million rules and 2 billion searches/sec.

Key features of NSE

- ✓ Available in 40Mb or 80Mb density [R8A20646BG-G/R8A20686BG-G]
- ✓ Dual Interlaken-LA ports
- ✓ 24TX + 24RX lanes, 12+12 per IL-LA port
- ✓ 10.3125Gbps/12.5Gbps Serial Interlaken-LA bus interface
- ✓ Full Ternary TCAM core memory cells
- ✓ Flexible search key width of 80/160/320/640bits
- ✓ 500Msps maximum bank search rate
- ✓ Multi TCAM array bank support
- ✓ 4x parallel search in single-bank configuration
- ✓ 2x parallel search in dual-bank configuration
- ✓ Valid bit per 80-bit entry for table management
- ✓ I2C interface for SerDes configuration
- ✓ IEEE 1149.1 test port
- ✓ 0.9V core power supply
- ✓ 1.80V I/O voltage
- ✓ 37.5x37.5mm2 1292pins FC-BGA package

For more information, please refer to the datasheet.

1.4   Control IP Features

Key features of control IP

- 2Bsps Key Search Support

- Separate I/F for Search Key Look-up User IF & AXI-4 Local Bus Access I/F (Table maintenance)

- Integrated Synchronizer

- Multiple look-up ports support (up to 8 ports)

- Multiple table configurations support (up to 32 tables)

- Support L2-L4 key search

- Enable dynamic table configuration & key configuration on live traffic

- Support dynamic block masked search

- Provide APIs for all configuration & operations
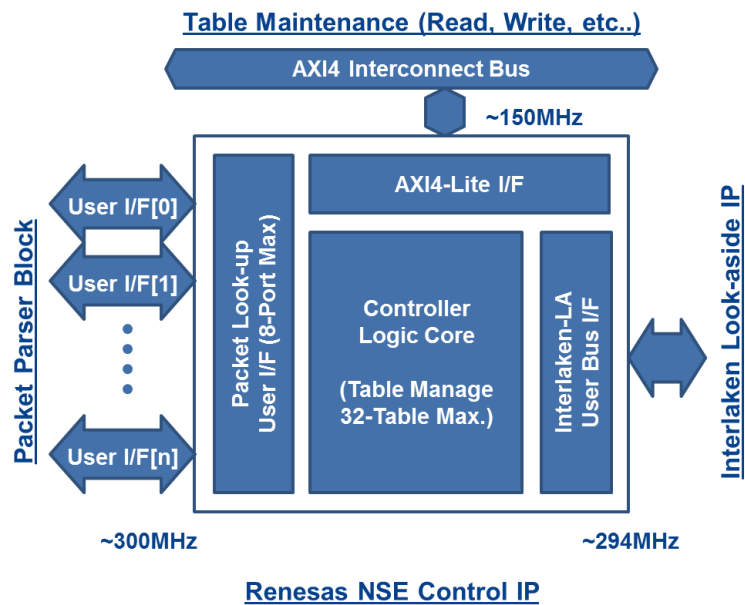
Figure 3   Structure of NSE control IP

1.5   Control IP API

Renesas API makes it easy to control NSE device. Configuration and usage of NSE functions require minimum prior knowledge of NSE. By using these APIs, it is possible for engineers who are not familiar with the register specification to operate the Control IP and to perform search functions.
Figure 4 shows examples of Control IP API commands.

Command Name	Description
REL_SNSE_Ctrl_ConfigureTable	Configuration of Table profile (can built 32 isolated table for max., and change the profile on live traffic.)
REL_SNSE_Ctrl_UpdateLookupIF	Lookup IF profile handling (can change lookup key profile without system reboot)
REL_SNSE_Ctrl_ActivateTable	Table activation & initialization
REL_SNSE_Ctrl_WriteEntry	Write the data and mask to the entry index
REL_SNSE_Ctrl_EraseEntry	Invalidate the data of the entry index
REL_SNSE_Ctrl_ReadEntry	Read the data and mask from the entry index (Parity check supported)
REL_SNSE_Ctrl_LookupChk	Lookup the key and report the index address for debug purpose
REL_SNSE_Ctrl_WriteBlkMask	Write NSE block mask register value of the table
REL_SNSE_Ctrl_ReadBlkMsk	Read NSE block mask register value of the table
REL_SNSE_Ctrl_WriteRegister	Write access to NSE device register space
REL_SNSE_Ctrl_ReadRegister	Read access to NSE device register space
⋮	⋮

Figure 4   Examples of Control IP API commands

1.6   Configurations

To support various user requests, NSE Control IP supports a wide range of configurations.
Figure 5 shows example of configurations.

Parameter	Valid Value	Description
N_OF_TABLE_PRF	1~32	The number of Lookup Table Profile to be used.
N_OF_LUP_IF	1~8	The number of Lookup IF
N_OF_PAR_LUP	1~4	The number of Parallel Lookup, i.e. number of Sub Table to be built in the device.
DYN_PRF_CTRL	YES or NO	Whether NSE device Profile Register is to be dynamically controlled from User IF or not. Please set this parameter "YES" if the user needs to customize natively NSE device table lookup profile.
DYN_BMR_CTRL	YES or NO	Whether NSE device Block Mask Register is to be dynamically controlled from User IF or not. Please set this parameter "YES" if the user needs to customize natively NSE device table block mask register.
PACKET_MON	YES or NO	The Packet Monitor feature.
Bank	X or Y	Target of bank to access.
L#_KEY_WIDTH	1~80	Key size of each User IF (byte)
⋮	⋮	⋮

Figure 5   Example of Control IP configurations

2. Development Support Environment

2.1 Reference Design with Verified Interoperability

Renesas development support tools consist of 1) reference board (RDK board) 2) RDK software tools, 3) sample design including verified control IP, 4) complete verification environment, and 5) complete evaluation environment. With already verified interoperability between the FPGA and NSE, these tools enable users to begin FPGA design and verification in parallel with network equipment system development. This will reduce the total development time and time-to-market.
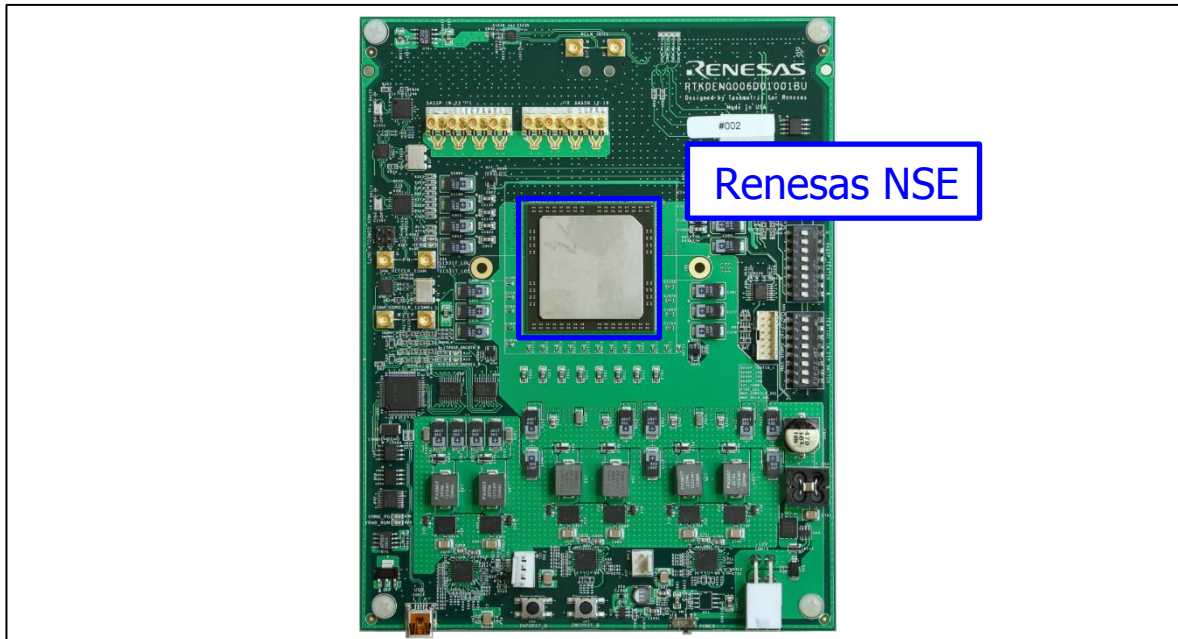
Figure 6   Reference Board
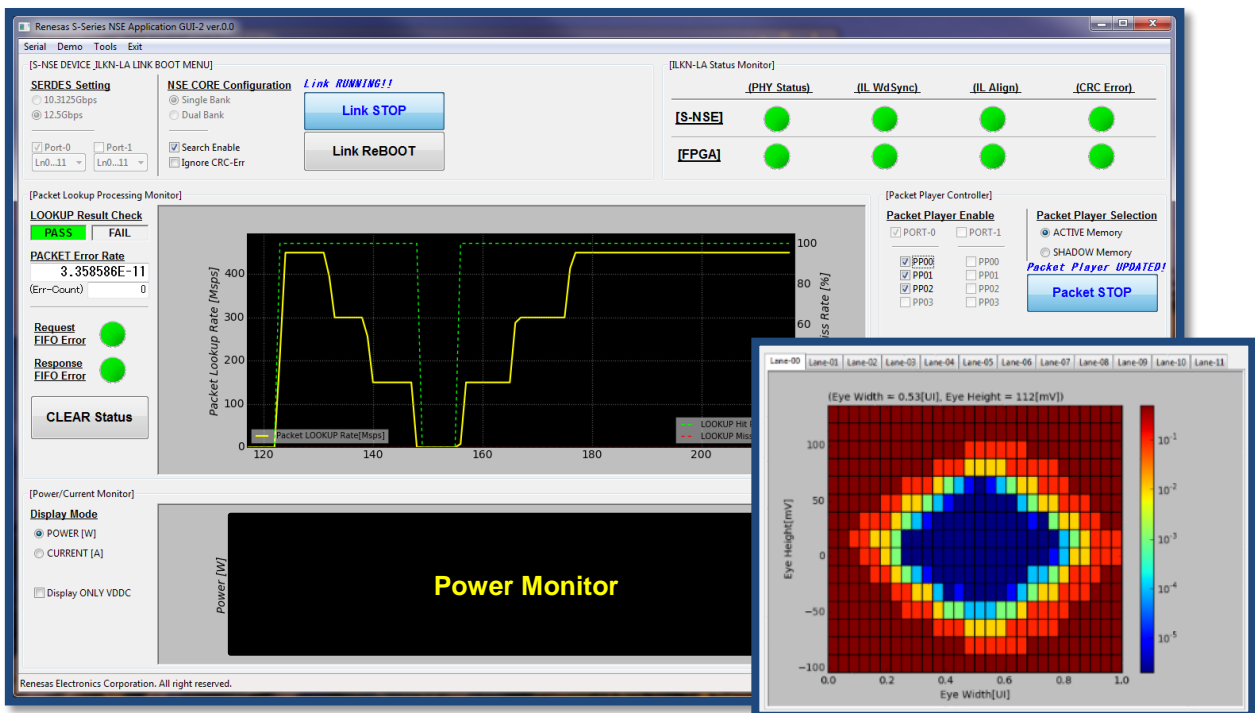
Figure 7   RDK Software Tools

Appendix

A.1 Glossary

ACL   [Access Control List]
ACL(Access Control List) is a list that is described an access rule of source/destination IP address, port number, TCP flag statement in network router, etc. The list consists of rules that are checked in order from the top. The list is used as packet filtering.

API   [Application Programming Interface]
API(Application Programming Interface) is a particular set of rules ('code') and specifications that software programs can follow to communicate with each other.
It serves as an interface between different software programs and facilitates their interaction.

FC-BGA   [Flip Chip Ball Grid Array]
FC-BGA(Flip Chip Ball Grid Array) is a BGA package by using Flip Chip packaging technology. BGA stands for Ball Grid Array, and it is a package that balls as terminals are set in a grid array. Flip Chip packaging technology means connections between the surface of the die and package substrate by using grid arrayed bumps as terminals.
FC-BGA has features of smaller mounting area and better electric characteristics than wire bonding package.

IL-LA   [Interlaken Look-Aside]
IL-LA**(**Interlaken Look-Aside) is a scalable chip-to-chip interconnect protocol designed to enable transmission speeds from 10Gbps to 150Gbps.

I2C   [Inter-Integrated Circuit]
I2C(Inter-Integrated Circuit) is a bi-directional two-wire serial bus designed by Philips Semiconductors, which provides a communication link between integrated circuits (ICs).
I2C has three data transfer speeds by using two wires for clock and data.
Standard is 100Kbps, Fast-mode is 400Kbps, and high-speed mode supports speeds up to 3.4Mbpss

NSE   [Network Search Engine]
Network Search Engines are specialized devices that provide high-speed network address lookups, a core function of network equipment.

SDN   [Software Defined Networking]
SDN**(**Software Defined Networking) is a technology or concept that enables the changing of network structure or configuration flexibly and dynamically by software that centrally controls network equipment.

TCAM   [Ternary Content Addressable Memory]
TCAM (ternary content-addressable memory) is a specialized type of high-speed memory that searches its entire contents in a single clock cycle.
This memory outputs the address of stored data which matches input data.
The term "ternary" refers to the memory's ability to store and query data using three different states: 0, 1 and X(Don't care).

Website and Support

Renesas Electronics Website
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Revision History

Rev.	Date	Description	
		Page	**Summary**
Rev.1.00	Sep, 2016		Rev. 1.00 Issued

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