

This layout guide provides some important information about the PCB layout of SLG59M1556V applications.

SILEGO STDFN 1.0x1.0-4L PKG

Unit: um

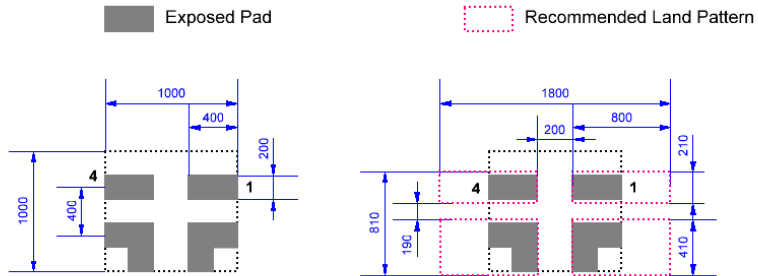


Figure 2. SLG59M1556V Package Dimensions and Recommended Land Pattern

Please solder your SLG59M1556V here

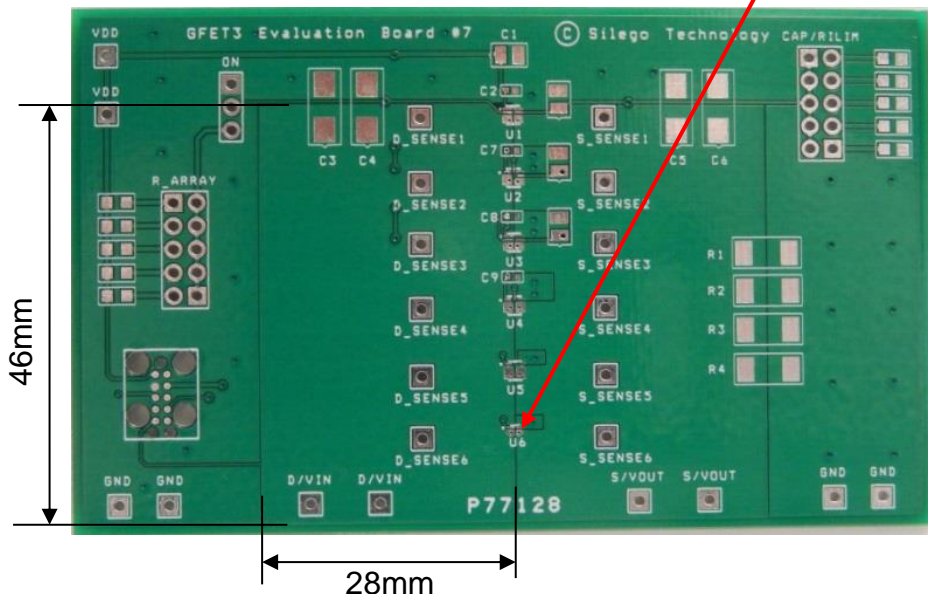


Figure 3. SLG59M1556V Evaluation Test Board

Note: Evaluation board has D_Sense and S_Sense pads. Please use them only for RDS(ON) evaluation.

2. Power and Ground Planes

2.1. The trace length from the control IC to the ON pin (PIN1) should be as short as possible and must avoid crossing this trace with power rails.

2.2. The D/VIN and S/VOUT pins carry significant current. Please note how the D/VIN and S/VOUT pads are placed directly on the power planes in Figure 3, which minimizes the RDS(ON) associated with long, narrow traces. The D/VIN, S/VOUT and GND pins dissipate most of the heat generated during high-load current condition. The layout shown in Figure 3 is illustrating a proper solution for heat to transfer as efficiently as possible out of the device.

2.3. The GND pin (PIN4) should be connected to GND.

2.4. 2 oz. copper is recommended for higher currents.