

This layout guide provides some important information about the PCB layout of SLG59M1713V applications.

SILEGO STQFN 1.6 x 2.5 - 16L PKG

Unit: um

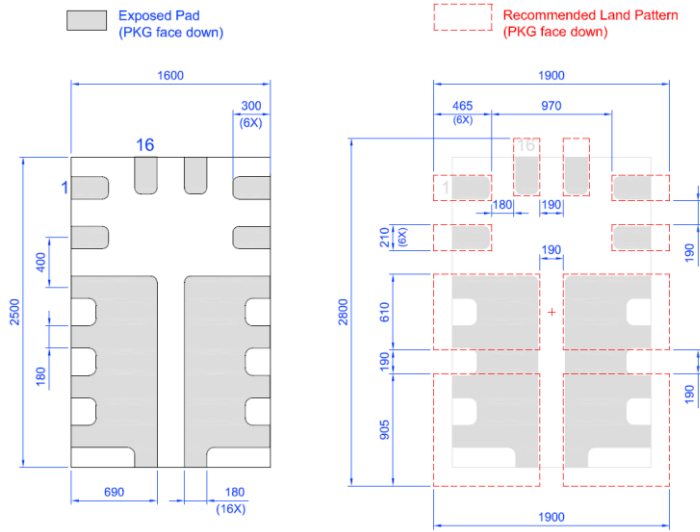


Figure 2. SLG59M1713V Package Dimensions and Recommended Land Pattern

Please solder your SLG59M1713V here

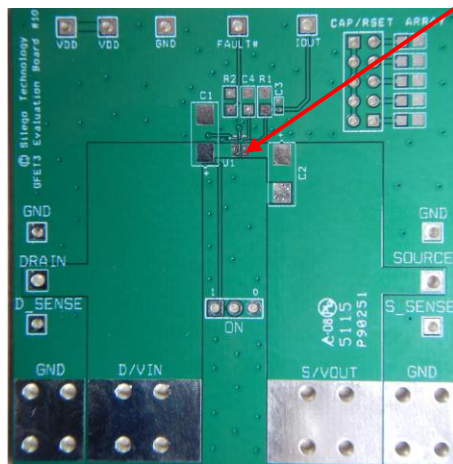


Figure 3. SLG59M1713V Evaluation Test Board

Note: Evaluation board has D_Sense and S_Sense pads. Please use them only for RDS(ON) evaluation.

2. Power and Ground Planes

2.1. The trace length from the control IC to the ON pin should be as short as possible and must avoid crossing this trace with power rails.

2.2. The VIN and VOUT pins carry significant current.

Please note how the VIN and VOUT pads are placed directly on the power planes in Figure 3, which minimizes the RDS(ON) associated with long, narrow traces. The VIN and VOUT pins dissipate most of the heat generated during high-load current condition. The layout shown in Figure 3 is illustrating a proper solution for heat to transfer as efficiently as possible out of the device.

2.3. The GND pin (PIN15) should be connected to GND.

2.4. 2 oz. copper is recommended for high current operation.

2.5. For testing, please connect as short as possible AWG14 or heavier gauge wires to VIN and VOUT terminals to avoid inductance influence on GFET3 during ON/OFF, Short circuit and Active Current Limit tests.

3. Basic Test Setup and Connections

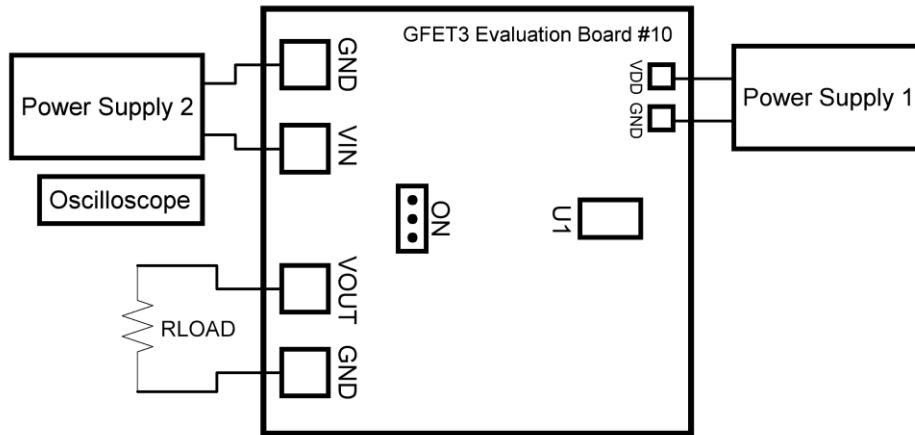


Figure 5. Typical connections for GFET3 Evaluation

2.1 EVB Configuration

1. Connect oscilloscope probes to VIN, VOUT, ON, etc.
2. Turn ON Power Supply 1 and set desirable VDD in range of 2.5V...5.5V
3. Turn ON Power Supply 2 and set desirable VIN in range of 0.8V...VDD
4. Switch ON to High or Low to evaluate GFET3 operation