Current Sharing Technique for VRMs

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Introduction

This paper describes an inexpensive and effective current sharing technique that enhances the performance and flexibility of voltage regulator modules (VRMs) intended for VRM 9.0 applications. As will be described later, this standardization will allow for greater interoperability between products from different manufacturers and result in benefits to OEMs and end users involved in the Computer OEM marketplace.

The Problem and Opportunity

The distributed power architecture has numerous advantages in microprocessor based systems. The point-of-load regulator in this system maintains high precision while supplying the dynamic load typical of microprocessors. The industry has evolved the point-of load converter into the VRM complete with standard form-factor and performance specifications. High-performance desktop computers, workstations, and servers use multiple microprocessors to satisfy the computing throughput demanded of these platforms. These applications use one VRM for each microprocessor to take advantage of the modularity and economy of scale offered by the VRM.

It is desirable to power the multiple processors from common power and ground planes to improve the speed and integrity of the interconnecting signals. Tying all of the VRM outputs to common power planes requires a mechanism to insure that each VRM equally shares its portion of the load.

This paper proposes a simple current sharing technique that can meet the requirements of VRM 9.0. For illustrative purposes we focus on a dual processor architecture which includes two VRMs as shown in Figure 1.

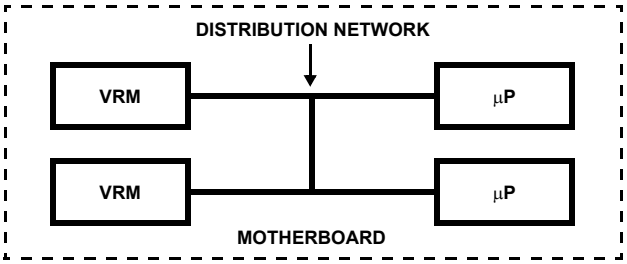

FIGURE 1. DUAL PROCESSOR/VRM ARCHITECTURE

At any given time, the two microprocessors demand different levels of current due to their processing activity and the status of their activation and stand-by states. It is desirable that the two VRMs be configured so that they share, approximately equally, the total current demand of the processors. This equalizes the load on the VRMs and results in higher reliability due to the reduced peak thermal demands and also will allow both VRMs to respond to dynamic demands from either processor, resulting in enhanced dynamic performance.

The overall goal is to have the VRMs share current so that the difference in current between the two VRMs is less than 10% of the total processor currents. But there are other criteria that are also desired. The current sharing method should:

- Be inexpensive and reliable
- Operate standalone or in configurations of up to eight parallel modules
- Configure itself automatically when the VRM is installed
- Operate with similar VRMs from different suppliers
- Operate with discrete voltage regulators (VRs) or packaged VRMs

If the above criteria can be met, VRMs from different suppliers – either packaged modules or discrete on-board solutions – will automatically share current within the 10% requirement. It will be much easier to develop second sourcing strategies and to provide field replacement and service of VRMs. We present here a methodology of accomplishing these goals, and offer it to the power and OEM communities as a solution to their common design objectives.

Droop Regulation for Increased Dynamic Headroom

The current sharing technique presented here depends upon the droop voltage regulation characteristic designed into high performance VRMs, so we will first briefly discuss the operation and implementation of this function. Droop regulation is a technique for deliberately adding a slope to the output voltage vs. output current regulation characteristic so that additional dynamic headroom is available both at the low current and high current regions, as shown in Figure 2. This slope can be achieved either by increasing the source impedance or by means of electronic control of the regulation characteristic. The output DC voltage remains within the regulation limits over all values of load current, but is skewed to a higher value at light load and to a lower value at heavy load. When operating at light load, an increasing current load transient will generate a negative-going voltage transition, and the output voltage is now biased so that there is a maximum amount of headroom for this transient before reaching the lower regulation limit. Correspondingly, a reduction in current when operating at heavy load will generate a positive-going transient, and there is now also increased headroom to accommodate it.

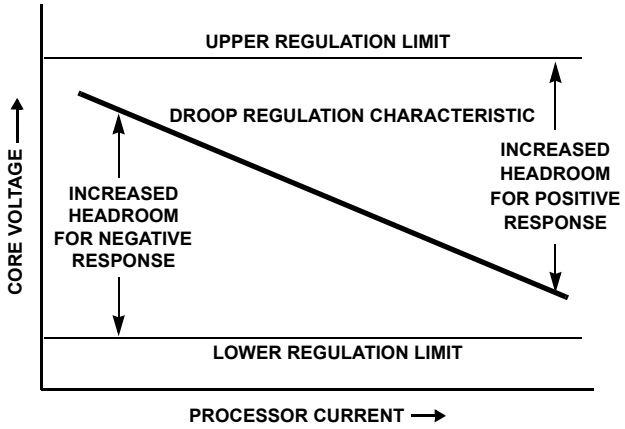

FIGURE 2. DROOP REGULATION CHARACTERISTIC

The exact implementation of the droop regulation function is dependent upon the control IC or circuitry used. For purposes of understanding, we will look at the technique utilized in the Intersil HIP6301 VRM controller. As we will see later, the current sharing approach will operate successfully even if the internal implementation of the droop function is different for different VRM suppliers.

Refer to Figure 3 for a simplified schematic of the droop regulation function in the Intersil HIP6301. For simplicity purposes we show only a two-phase VRM, but the concept is similar for additional phases.

The current in each channel of the VRM is sensed by measuring the voltage drop across $r_{DS(ON)}$ of the lower MOSFET when it is conducting. This sensed current is then used to balance the two (or more) channel currents as indicated in the diagram. Consequently, the VRM has internal current sharing for its own channels, but no provision for current sharing with an additional VRM. The sensed channel currents are also used to control additional current sources. The outputs of these current sources will be proportional to the individual channel currents, and their sum will represent the total current output of the VRM. As can be seen from the diagram, the only DC path for these currents is the resistor R_{FB} which returns to the output, V_{CORE}. The summed channel currents, flowing through this resistor, develop a voltage drop, V_{DROOP}, which offsets the error amplifier in the direction to decrease the VRM output voltage as the output current increases. In the HIP6301, the value of I_{DROOP} that corresponds to full output current from the VRM is 50µA. This value of current and the desired voltage droop characteristic will determine the selection of the value of R_{FB}. We will use the voltage V_{DROOP}, which is proportional to the VRM output current, as the basis of the VRM current sharing technique described below. The technique will also be compatible with other droop regulation techniques that develop a scalable voltage proportional to the VRM output current.

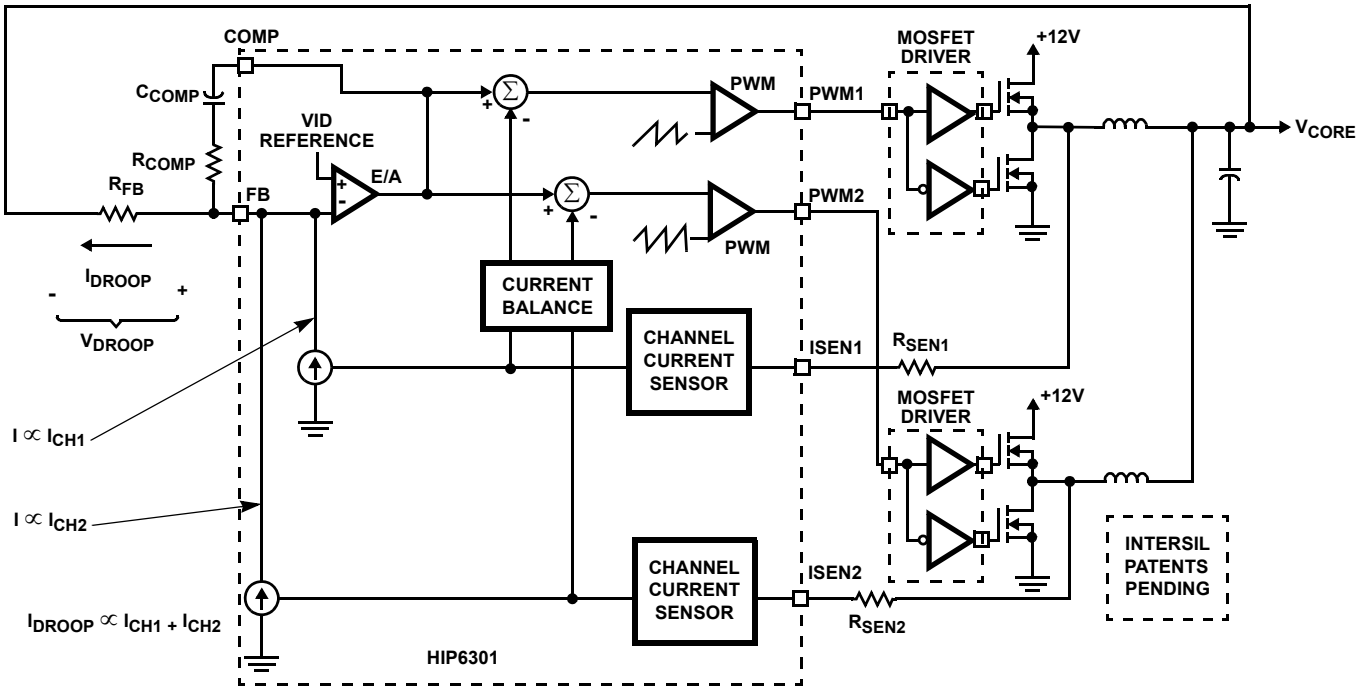

FIGURE 3. IMPLEMENTATION OF DROOP REGULATION

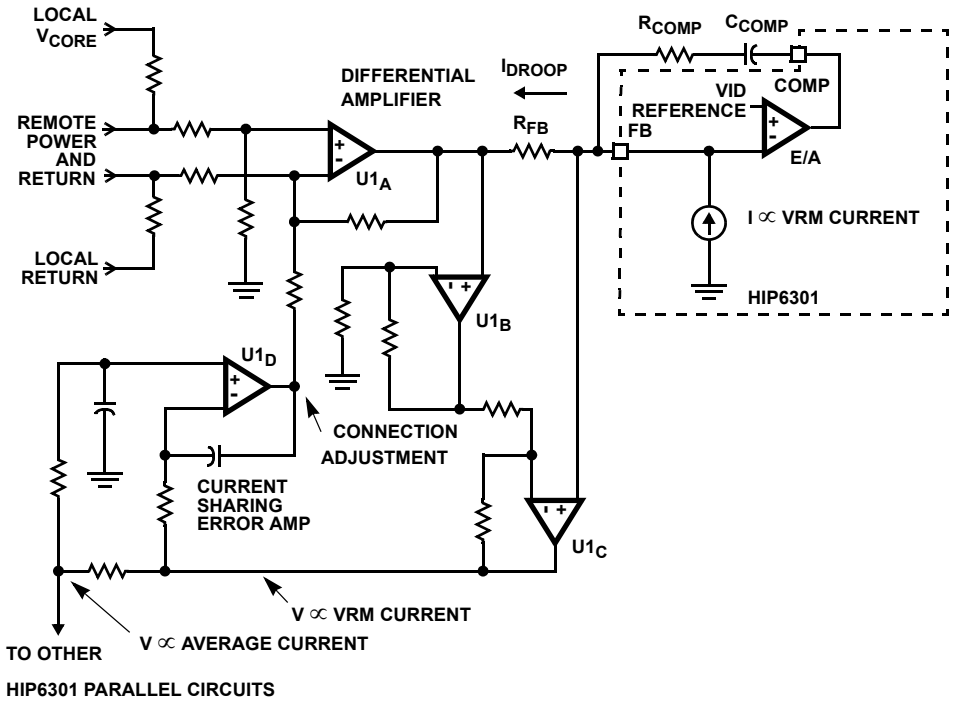

FIGURE 4. CURRENT SHARING CIRCUITRY

Circuit Description

The circuitry used to achieve the current sharing between VRMs is shown in Figure 4. It consists of a single quad op amp, U1, along with associated small resistors and capacitors. $U1_A$ is used as a differential amplifier for the purpose of achieving differential remote sensing close to the processors. There are also local sense resistors to protect the VRM from overvoltage conditions in the event of an open sense line. The output of $U1_A$ connects to R_{FB} at the same location as V_{CORE} in Figure 3. I_{DROOP} flows through R_{FB} as described in the previous section. The voltage drop across R_{FB}, V_{DROOP}, is amplified by $U1_B$ and $U1_C$ to achieve a voltage that is proportional to the total output current of this VRM.

$U1_D$ is the current sharing error amplifier. The voltage developed by $U1_B$ and $U1_C$, representing the output current of the VRM, is presented to its inverting input. This same voltage is sent through a summing resistor to the common current sharing connection to the other VRM. This node then represents the average current from both VRMs. $U1_D$ compares the VRM current with the average current of both VRMs and makes an appropriate correction to the inverting input of the differential amplifier, $U1_A$. This correction will force both VRMs to achieve the same output current to within the specified tolerance.

If another control IC or circuit is used in place of the Intersil HIP6301, the current sharing can still function so long as the V_{DROOP} signal is appropriately scaled to the same full current value. If this is done, VRMs and discrete circuits from different suppliers may work together to achieve the desired current sharing performance.

Figure 5 shows the complete system implementation when two VRMs are interconnected with the current sharing technique. The circuitry dedicated to the current sharing function is labelled in the figure. Note that each VRM receives remote sensing information from the common load bus.

Implementation and Performance

The proposed current sharing technique was implemented by Artesyn Technologies® in a prototype four phase VRM using the Intersil HIP6301 control IC. The current sharing implementation was done with one quad op-amp along with a few discrete resistors and two small capacitors, and takes up a minimal amount of additional board space on the VRM as seen in Figure 6. This minimal component count and board space, along with one signal pin on the VRM connector for current sharing, results in an economical and reliable solution.

A test set-up configured with two VRMs was used to evaluate the current sharing performance of the interconnected VRMs. The load currents on the two load connections could be varied independently via electronic loads so that the current contribution of each VRM could be measured as a function of the currents on each load.

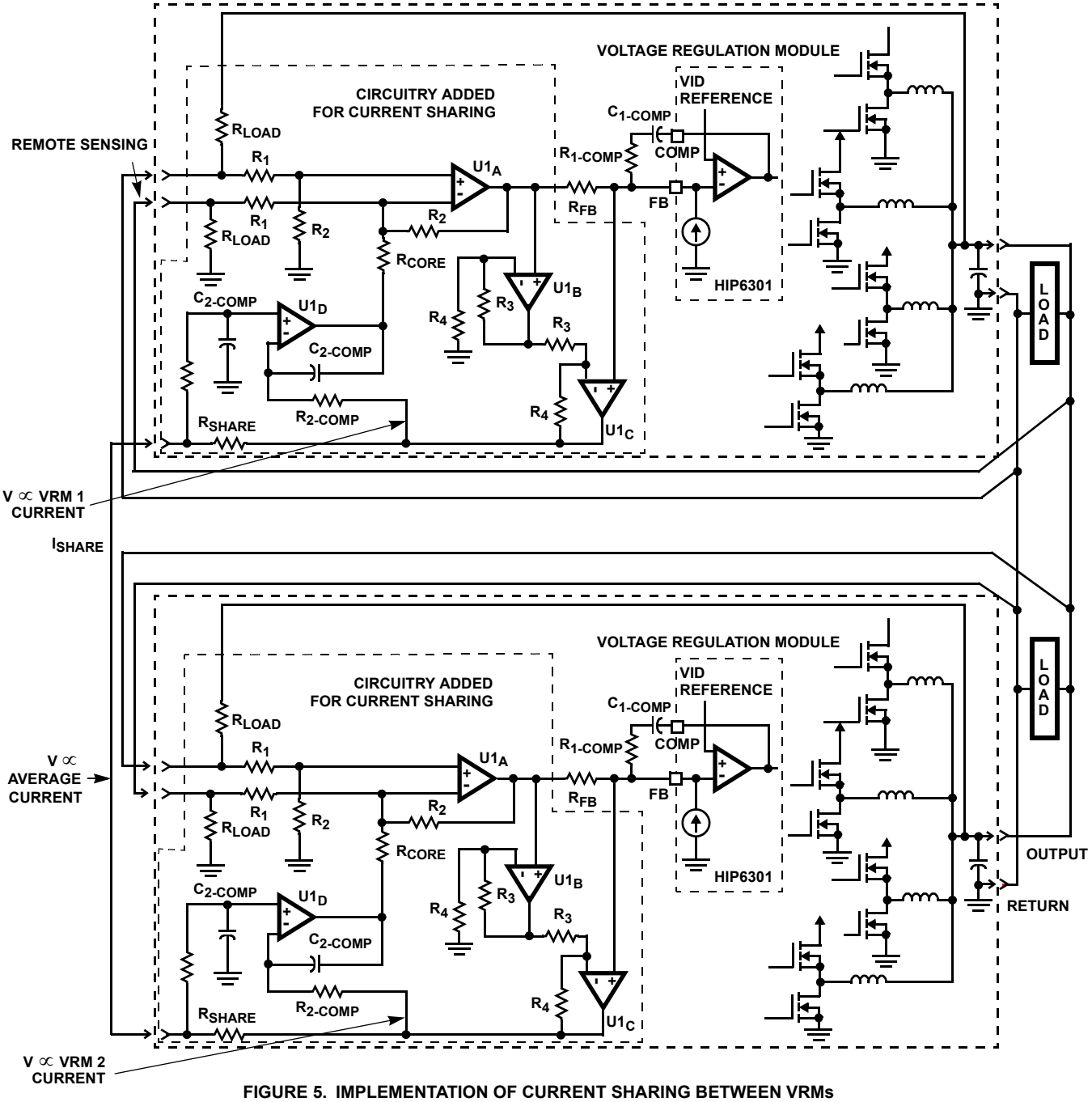

FIGURE 5. IMPLEMENTATION OF CURRENT SHARING BETWEEN VRMs

Several data points were obtained, ranging from balanced 4A loads up to a completely unbalanced load with 100A on one load and 0A on the other. The resulting current sharing performance is shown in Table 1. The percentage of current sharing is shown along with the absolute difference in current between the two VRMs. Note that, under all conditions, the current sharing is well below the 10% objective.

The contribution of the current sharing connection is graphically illustrated in Figure 7. In this test the current sharing connection was kept open initially in a situation with a large imbalance between the VRMs. There was a load current of 45A, but the imbalance caused one VRM to sink 5A of current while the other VRM sourced 50A, 45A for the load and 5A for the first VRM. After connecting the current sharing lines, the two VRMs established equal currents of 22.5A in less than 2ms.

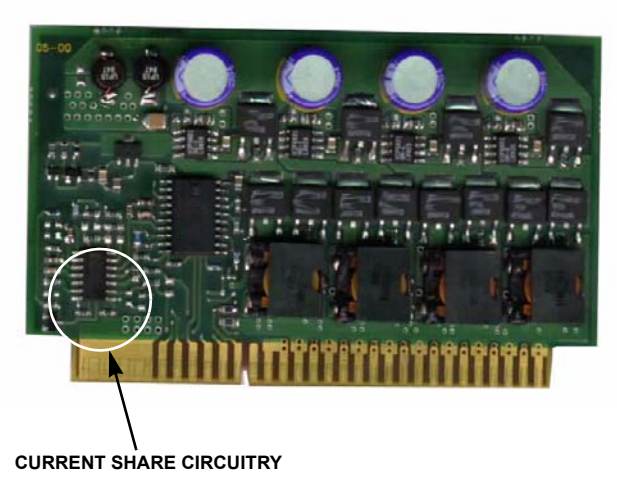

Photo Courtesy of Artesyn Technologies

FIGURE 6. PHYSICAL REALIZATION OF PROPOSED CIRCUIT

TABLE 1. CURRENT SHARING PERFORMANCE

LOAD 1 (A)	LOAD 2 (A)	VRM 1 (A)	VRM 2 (A)
4	4	3.70	4.30
8	8	7.50	8.50
0	16	7.35	8.65
30	0	16.25	13.75
30	30	28.10	31.90
0	60	27.60	32.40
50	50	47.00	53.00
0	100	46.40	53.50

Summary

A VRM current sharing technique has been presented that should meet the desired technical requirements and be very attractive for both power module suppliers and OEMs in the computing marketplace. Standardizing upon a common approach as suggested here provides the advantage of interoperability between various vendors greatly simplifying the logistics of multi-sourcing.

It is the intent of Intersil to make this concept and the resulting circuits freely and openly available to the power module community without licensing or royalties.

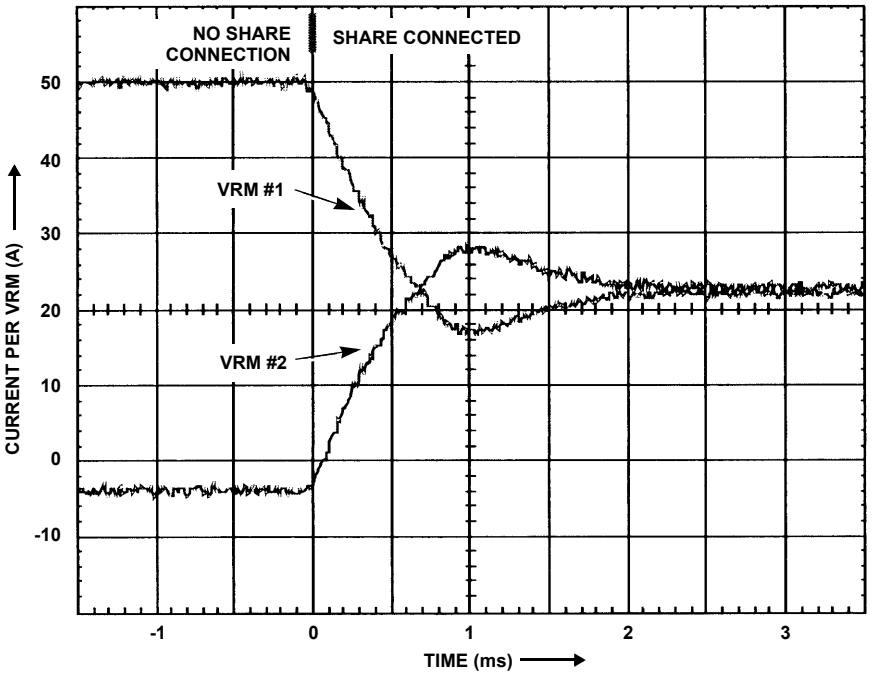

FIGURE 7. CURRENT SHARING PERFORMANCE

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