Full-Duplex Transceivers

Transmitting Full-Duplex Data over a Single Twisted Pair Cable

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Abstract

This document describes the concept and design of transmitting full-duplex data over a single Unshielded Twisted Pair (UTP) cable. The interface connection is a 350ft point-to-point data link using the ISL32705E isolated full-duplex transceivers as signal sources at both cable ends. One transceiver transmits data at rate of 2Mbps, the other at 4Mbps.

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1. Introduction

Higher data throughput, shorter response time, and lower installation costs are the key drivers behind the ongoing improvement efforts in industrial network design. For these reasons, allowing the immediate and continuous exchange of binary data has made the full-duplex bus the preferred interface choice in point-to-point connections. Unlike the half-duplex interface, which transmits or receives data one direction at a time, the full-duplex interface does both simultaneously. This promptness however, comes at the expense of increased cabling effort and installation cost (Figure 1).

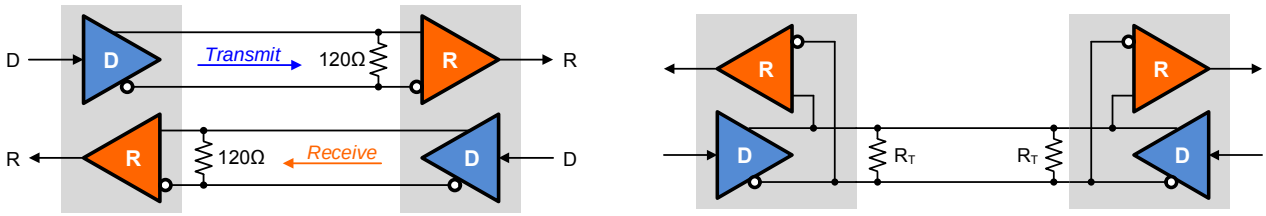

Figure 1. Full-Duplex Interface Requires Twice the Cabling Effort of a Half-Duplex Interface

To counteract this drawback, the world of RS-485 users is seeing a new type of interface emerging that allows for full-duplex data transmission over a single twisted-pair cable.

Violating one of RS-485's fundamental principles of avoiding bus contention at all times, this point-to-point interface relies on bus contention by keeping two full-duplex transceivers permanently enabled.

To enhance interface noise immunity, the transceivers are galvanically isolated. This isolation keeps the bus free from common-mode noise, ensuring reliable data transmission in electrical noisy environments with common-mode voltages of up to ±600V.

Full-duplex communication over a single signal pair requires 4-to-2 wire conversions between the transceivers and the bus cable to distinguish the incoming (receive) data from the outgoing (transmit) data (Figure 2).

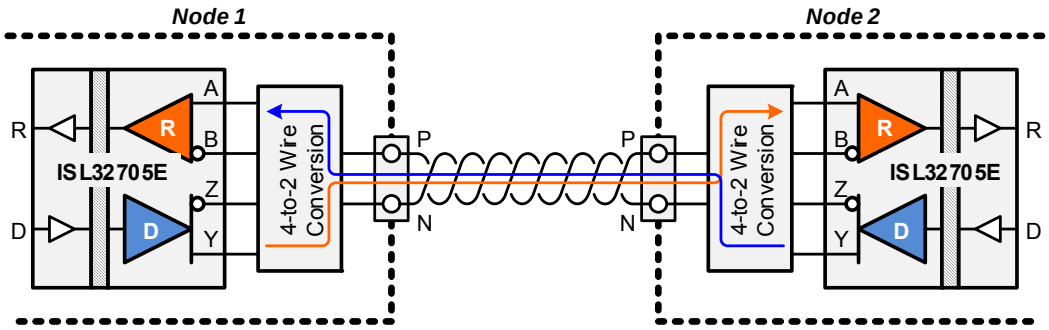

Figure 2. Full-Duplex Transmission over Single Twisted Pair Requiring 4-to-2 Wire Conversion

The design of a 4-to-2 wire converter can be tricky. Although there are circuits available for solving the data separation digitally, their high component count and complicated PCB layout can result in expensive designs. This approach also has a major drawback: the circuits work only in a low-noise lab environment. In addition, exposing the circuits to high common-mode voltages causes them to cease operation.

To provide designers with a robust high-speed solution that transmits 4Mbps over 350ft cable length while tolerating high common-mode voltages, this document discusses the design of a bus node, made up of an isolated full-duplex transceiver and six resistors, performing current limiting, line termination, and 4-to-2 wire conversion.

2. Bus Node Design

There are three main aspects to consider during the bus node design (Figure 3):

- Current limiting: Because both transceivers are consistently active, bus contention occurs, causing the flow of large differential currents. In addition, large ground potential differences between the transceiver grounds also cause large common-mode currents to flow. To prevent the drivers from overloading and eventually experiencing thermal shut down, current limiting resistors (R_S) must be placed into a driver's output path.
- Bus node termination: Preventing signal reflections on the line, the bus node impedance must match the characteristic impedance of the bus cable. This is accomplished with the termination resistor, R_T.
- 4-to-2 wire conversion: Resistive voltage dividers consisting of the bus resistors (R_B), the driver output resistors (R_D), and the receiver input impedance (R_{IN}) extract the receive signal from the full-duplex data on the bus.

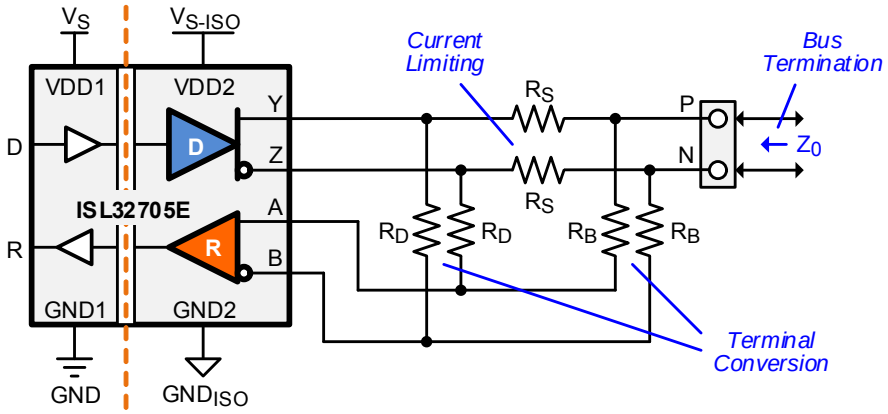

Figure 3. Three Main Aspects of the Bus Node Design

3. Driver Output Parameters, R_O and V_0

Because both drivers are always active, their output impedance (R_O) and differential electromotive force (V_0) affect the calculation of all resistor values as well as the voltage relations on the bus. The parameters are quickly determined by drawing a straight, best-fit line through the driver's V-I characteristic, provided in the ISL32705E data sheet. For the transceiver in Figure 4, these parameters are $V_0 = 4.5V$ and $R_O = V_0/I_O = 50\Omega$.

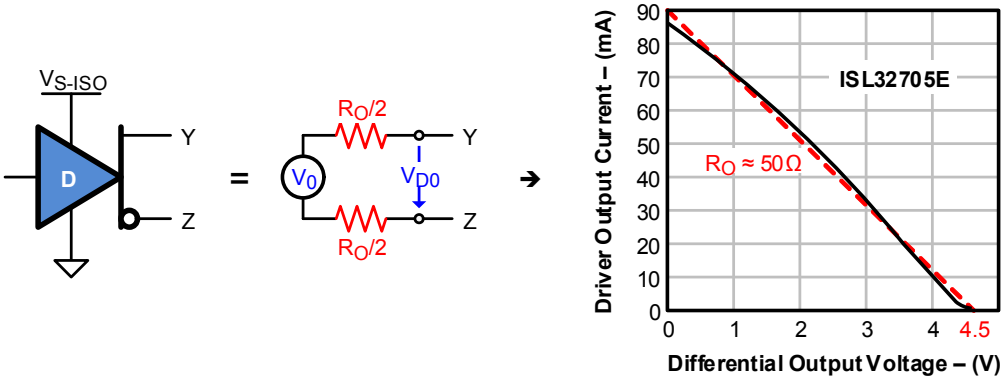

Figure 4. Determining the Driver Output Characteristics with $R_O = 50\Omega$ and $V_0 = 4.5V$

4. Current Limiting Resistors, R_S

The value of R_S is calculated so that the two driver output currents are limited to normal operating values at the maximum voltage difference. For example, if both driver outputs are of opposite polarity, the typical voltage difference between them is 3.3V. Limiting the output current to about 30mA requires a total resistance of 3.3V/30mA = 110Ω and 55Ω for each R_S. Using the closest standard value easily available, each R_S becomes 60.4Ω.

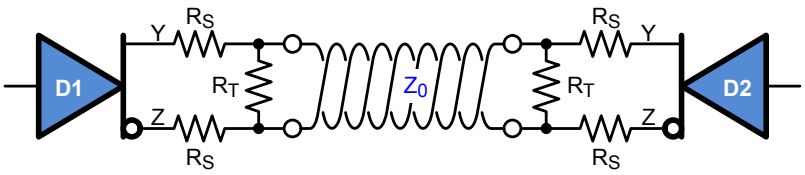

Figure 5. Single-Ended, Point-to-Point Data Link

5. Line Termination

To prevent signal reflections on the bus, the input impedance of a bus node must match the characteristic cable impedance, Z_0. In this case, it means the combined impedance of the termination resistor (R_T) in parallel to the series circuit of the two R_S resistors and the driver output impedance (R_O) should equal Z_0.

(EQ. 1) $$R_T \| (2R_S + R_O) = Z_0$$

Because R_T is the only option to tune the bus node impedance towards Z_0, we solve (EQ. 1) for R_T:

(EQ. 2) $$R_T = \frac{(2R_S + R_O) \cdot Z_0}{2R_S + R_O - Z_0}$$

Inserting the values R_S = 60.4Ω, R_O = 50Ω, and Z_0 = 100Ω (for Cat-5 cable) yields 241Ω, and choosing the next higher value from the E-96 series of standard resistor values makes R_T = 243Ω.

6. 4-to-2 Wire Conversion

The 4-to-2 wire converter enables a bus node to extract the output signal of the opposite bus node from the full-duplex signal on the bus. It does so by subtracting its own driver output from the bus voltage. Focusing on node 1 (Figure 6), we establish the equation for the bus voltage V_{B1} with G_1 and G_2 as the generic gain coefficients:

(EQ. 3) $$V_{Bl} = V_{Dl} \cdot G_1 + V_{D2} \cdot G_2$$

Solving for the V_{D2} component gives us the attenuated output of bus node 2:

(EQ. 4) $$V_{D2} = \frac{V_{Bl} - V_{Dl} \cdot G_1}{G_2}$$

Circuit-wise, (EQ. 4) can be resolved with multiple difference amplifiers. With each amplifier stage requiring four gain resistors, the component count increases significantly, making this solution an expensive and complex design.

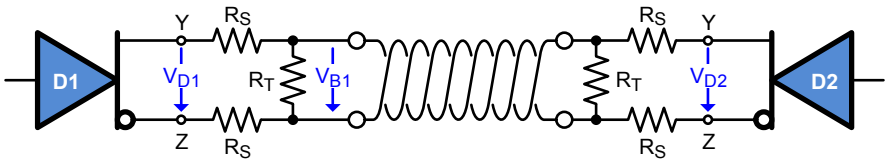

Figure 6. $V_{B1} = V_{D1} \times G_1 + V_{D2} \times G_2$

However, if we split V_{D1} and V_{B1} into their individual line voltages ($V_{D1} = V_Y - V_Z$, $V_{B1} = V_P - V_N$) and add them through resistive voltage dividers (see Figure 7), we can define the voltages at the summing points as the receiver input voltages, V_A and V_B:

(EQ. 5) $$V_A = \frac{V_P}{G_{V1}} + \frac{V_Z}{G_{V2}}$$

(EQ. 6) $$V_B = \frac{V_N}{G_{V1}} + \frac{V_Y}{G_{V2}}$$

where G_{V1} and G_{V2} are the generic gain factors of the voltage dividers.

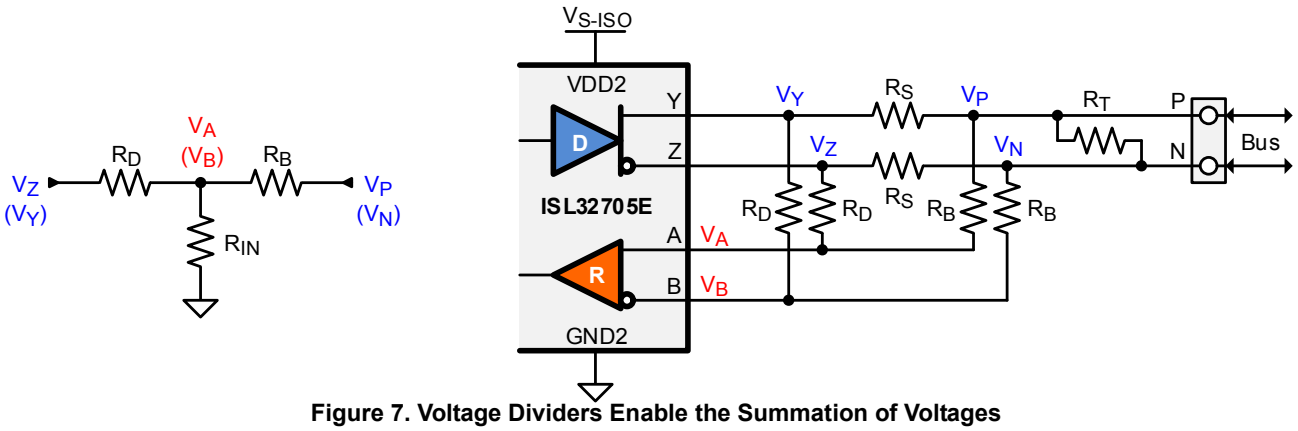

Figure 7. Voltage Dividers Enable the Summation of Voltages

Then, building the difference $V_A - V_B$ gives the actual receiver input voltage:

(EQ. 7) $$V_{AB} = \frac{V_{B1}}{G_{V1}} - \frac{V_{D1}}{G_{V2}} = \frac{V_{B1} \cdot G_{V2} - V_{D1} \cdot G_{V1}}{G_{V1} \cdot G_{V2}}$$

Comparing the gain coefficients in (EQ. 4) with those in (EQ. 5) results in $G_1 = G_{V1}$, $G_2 = G_{V1} \cdot G_{V2}$, and $G_{V2} = 1$, which proves the validity of the voltage divider concept.

For practical applications, the receiver input impedance (R_{IN}) must be considered, because it causes a reduction in gain factors. To minimize the impact of R_{IN}, it is recommended to make the value of R_B smaller than 0.1 R_{IN}, but larger than 1kΩ to maintain low differential bus loading:

(EQ. 8) $$0.1R_{IN} \geq R_B \geq 1k\Omega$$

The ratio of R_B/R_D should match the ratio of V_{B1}/V_{D1}, aka G_1, thus demanding that $R_D = R_B/G_1$. However, G_1 is a nonlinear function of L (the length of the bus cable), R_S, R_T, and Z_0, resulting in a complex algebraic expression. To simplify, (EQ. 7) presents the final equation to calculate R_D:

(EQ. 9) $$R_D = R_B\left(1 + \frac{2R_S}{R_T \| (0.056 \cdot L + Z_0)}\right)$$

where L is the cable length in ft.

7. Application Example

Figures 8 and 9 show the design and scope shot of a 4Mbps high-speed full-duplex data link over 350ft Cat-5 cable. Each bus node includes an isolated 4Mbps full-duplex transceiver and a resistor network of R_S = 60.4Ω, R_D = 2.49kΩ, R_B = 1kΩ, and R_T = 243Ω.

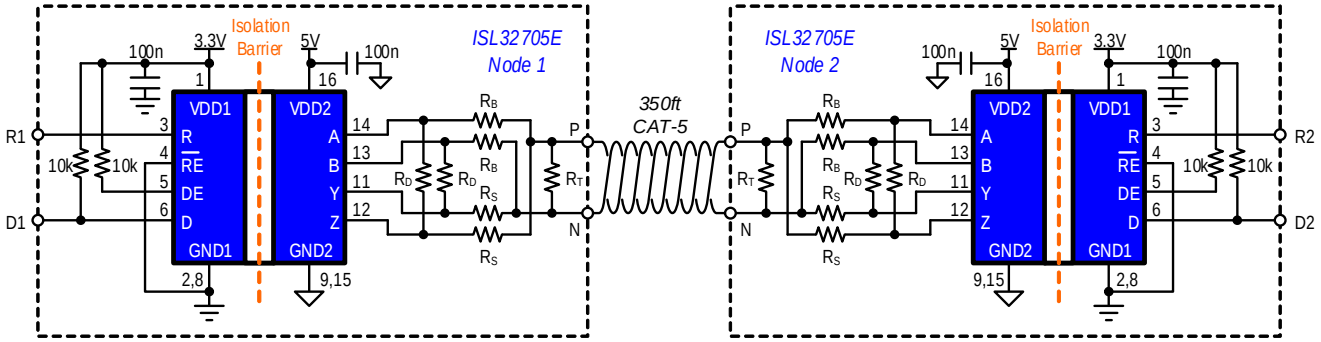

Figure 8. Full-Duplex Transmission of 2Mbps Data at Node 1 and 4Mbps Data at Node 2

The driver inputs are fed with logic signals of different data rates. D1 receives a 2Mbps signal and D2 receives a 4Mbps signal at a random phase shift. Figure 9 shows that the receiver output of node 2 (R2) correctly displays the input data of D1, and vice versa, R1 displays the input data of D2.

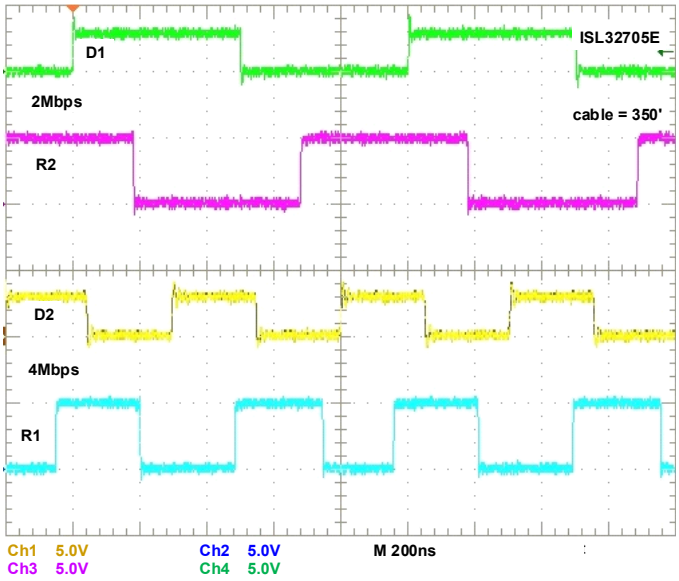

Figure 9. Full-Duplex 2Mbps and 4Mbps Data Correctly Decoded

8. Conclusion

Transmitting full-duplex data over a single twisted pair cable is made possible through 4-to-2 wire converters, which connect the 4-pin bus I/O of full-duplex transceivers to two bus cable conductors. To maintain a simple and inexpensive bus node design, voltage dividers are used to extract the receive signal from the full-duplex mix on the bus. Although this document describes a high-speed data link using the isolated full-duplex transceiver ISL32705E, Renesas provides a wide range of full-duplex transceivers for various data rates, output drives, and common-mode voltages.

9. Revision History

Rev.	Date	Description
0.00	Nov 2, 2017	Initial release