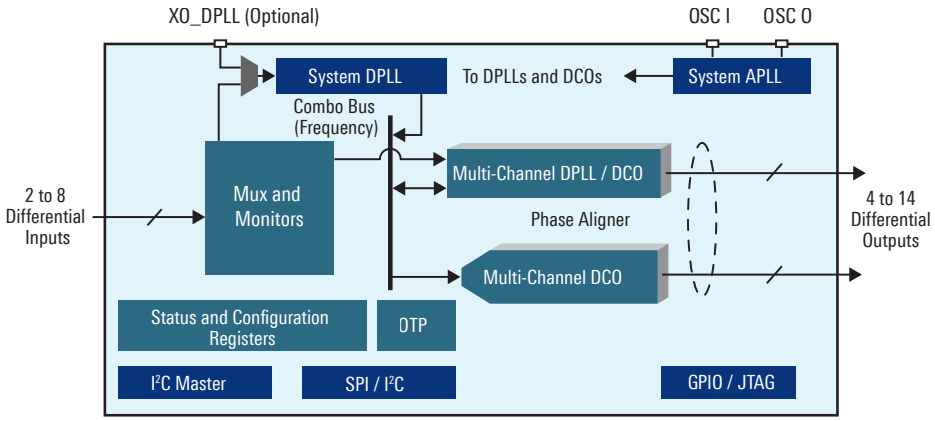
RENESAS
BIG IDEAS FOR EVERY SPACE

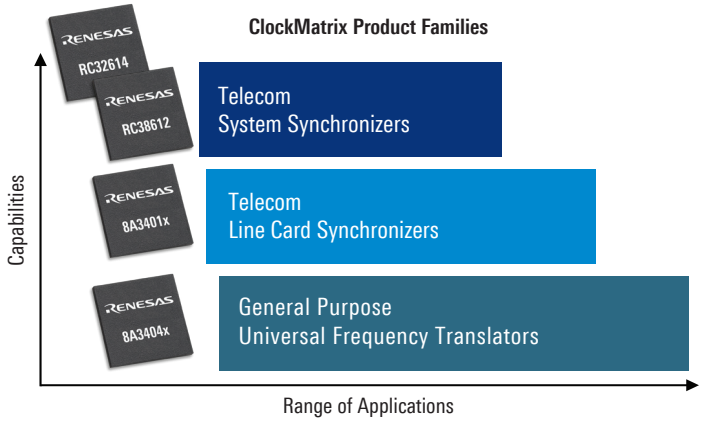
CLOCKMATRIX™ OVERVIEW

The Renesas ClockMatrix family of multi-channel timing devices reduces the complexity and cost of clock trees by replacing multiple timing chips with a single timing resource. The devices support a wide range of frequencies and signal types at their inputs and outputs.



ClockMatrix devices include two types of timing channels: Digital PLL / Digitally Controlled Oscillator (DPLL/DCO) channels and DCO only channels. Any DCO can free run based on the local oscillator. They can be controlled by external software or they can be connected to a DPLL channel to supply additional outputs and frequencies for that DPLL.

A wide range of simple to complex timing and synchronization applications are covered by the ClockMatrix family using its flexible architecture, a common register set and a few package types.



In the ClockMatrix family, the Universal Frequency Translator™ (UFT) devices perform jitter attenuation and frequency translation functions for general purpose applications.

System synchronizers generate ITU-T compliant clocks for telecom systems while the telecom line card synchronizers generate ITU-T complaint clocks for line cards locked to a system synchronizer.

Highly flexible multi-channel timing devices

- Up to 8 independent channels
- Timings channels configurable as DPLLs or DCOs
- Generates any frequency from 0.5Hz to 1GHz

Ultra-low jitter

ClockMatrix

- 150fs RMS (typ) 12kHz to 20MHz
- Suitable for up to 28Gbps PHYs

ClockMatrix 2

- 88fs RMS (typ) 12kHz to 20MHz
- Suitable for 56/112Gbps PHYs

Precision time sync.

- Supports cTE < 5ns for G.8273.2 Classes A, B, C, D
- Input to output phase skew< 100ps
- Output to output phase skew < 50ps

Applications

- IEEE 1588
- Synchronous Ethernet
- eCPRI and CPRI (ClockMatrix)
- Up to 28Gbps PHYs (ClockMatrix)
- 56/112Gbps PHYs (ClockMatrix 2)
- 400/800Gbps optical transport and wireline network applications (ClockMatrix 2)
- 5G fronthaul and backhaul (ClockMatrix)
- Routers / Switches
- OTN and PTN equipment
- Baseband and Radio Units

Standard compliance

- ITU-T G.8262
- ITU-T G.8262.1
- ITU-T G.8273.2

CLOCKMATRIX FAMILY OVERVIEW

ClockMatrix 2 devices deliver improved performance with phase jitter as low as 88 fs-rms. The highly integrated devices provide all the functionality needed to implement an IEEE 1588 clock solution with jitter attenuation capabilities resulting in ultra-low jitter clock outputs for Synchronous Ethernet PHYs with data rates up to 112Gbps, reducing design complexity and bill of materials (BOM) requirements, while also allowing customers to apply the timing devices to a wide variety of network applications.

ClockMatrix Family Comparison

	System Synchronizers	Line Card Synchronizers	Universal Frequency Translators
Jitter Attenuation	Yes	Yes	Yes
Frequency Translation	Yes	Yes	Yes
Hitless Reference Switching	Yes	Yes	Yes
DPLL Loop Filters	0.09mHz to 12kHz	17Hz to 12kHz	17Hz to 12kHz
Reference Frequencies	0.5Hz to 1GHz	1kHz to 1GHz	1kHz to 1GHz
Output Frequencies	0.5Hz to 1GHz	0.5Hz to 1GHz	0.5Hz to 1GHz
Align Clocks with Input Sync Pulse	Yes	Yes	Yes
Sync Pulse over PWM	Yes	Yes	No
Data over PWM	Yes	Yes	No
EEC1 and EEC2 per G.8262	Yes	No	No
eEEC per G.8262.1	Yes	No	No
Telecom Boundary Clock per G.8273.2	Yes	No	No

System Synchronizer Family									Line Card Synchronizer Family		
	8A34001	8A34002	8A34003	8A34004	8A34005	8A34046	RC38612	RC32614 (ClockMatrix 2)	8A34011	8A34012	8A34013
Inputs (Diff / SE)	8 /16	7 /14	2 / 4	2 / 4	2/ 4	4 / 8	5/ 10	4/ 8	8 / 16	7 /14	2 / 4
Outputs (Diff / SE)	12 / 24	8 / 16	4 / 8	4 / 8	12 / 24	12 / 24	12 / 24	14 / 24	12 / 24	8 / 16	4 / 8
DPLL / DCO Channels	8	4	4	2	4	4	6	6	8	4	4
DCO Channels	0	0	0	0	0	4	0	0	0	0	0
Package	10 x 10 mm 144-CABGA	10 x 10 mm 72-QFN	7 x 7 mm 48-QFN	7 x 7 mm 48-QFN	10 x 10 mm 72-QFN	10 x 10 mm 72-QFN	10 x 10 mm 72-QFN	10 x 10 mm 144-CABGA	10 x 10 mm 144-CABGA	10 x 10 mm 72-QFN	7 x 7 mm 48-QFN

Universal Frequency Translator Family

	8A34041	8A34042	8A34043	8A34044	8A34045
Inputs (Diff / SE)	8 / 16	7 / 14	2 / 4	4 / 8	2 / 4
Outputs (Diff / SE)	12 / 24	8 / 16	4 / 8	12 / 24	12 / 24
DPLL / DCO Channels	8	4	4	4	2
DCO Channels	0	0	0	4	6
Package	10 x 10 mm 144-CABGA	10 x 10 mm 72-QFN	7 x 7 mm 48-QFN	10 x 10 mm 72-QFN	10 x 10 mm 72-QFN

To learn how PTP Clock Manager software can help you easily implement synchronization in IEEE 1588 systems visit **renesas.com/clockmanager**

To request samples, download documentation or learn more visit **renesas.com/clockmatrix**

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