RENESAS

PCI EXPRESS® TIMING SOLUTIONS

Comprehensive timing portfolio from the industry's leader in timing solutions

renesas.com/pcietiming

Renesas' industry-leading PCIe® timing portfolio provides the most complete solution for networking, storage, compute, accelerator, and industrial applications.

Our PCIe clock generators, zero-delay / fanout buffers, and fanout multiplexers support PCIe Gen7 data rates and derivatives. These devices are all designed to work together to form a complete solution. Renesas' patented LP-HCSL outputs with integrated terminations eliminate up to 4 resistors per differential output, saving board space and reducing output power by up to 90% over standard HCSL outputs.

Our extensive selection of timing devices allows designers to implement the most complex PCI Express clock trees while maintaining timing margin, minimizing board space, and reducing power consumption, thus ensuring robust system operation.
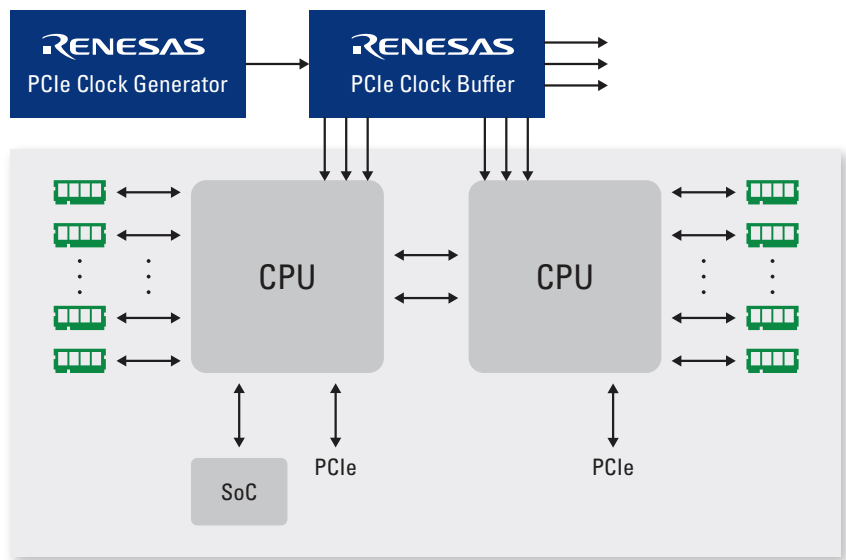
Peformance

- PCIe Gen7, 128GT/s
- PCIe Gen6, 64GT/s
- PCIe Gen5, 32GT/s

Integration

- Integrated terminations save up to 160 mm^2 board area
- Integrated crystal load capacitors on programmable devices
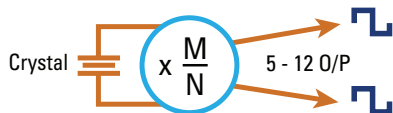- Integrated devices crystal options available

Security
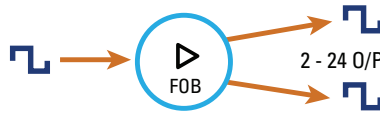
- Software write protection available

PCI Express Gen7 Timing Solutions

### R21 Clock Generator

Crystal — x $\frac{M}{N}$ — 5 - 12 O/P

- Integrated the termination resistors and crystal for space saving and simplified design
- Flexible power rails 1.8V, 2.5V, and 3.3V
- Simultaneous spread/non-spread clock outputs

RC190/RC191 Fanout Buffer

FOB — 2 - 24 O/P

- Eliminate up to 96 resistors
- Save up to 160 mm^2 of area[†]
- As small as 16 mm^2
- Selectable output impedance 33, 85, and 100-Ω
- SSC compatible
- Flexible power rails 1.8V and 3.3V

RC192/RC193 Multiplexer

2 In — FOB — 2 - 16 O/P
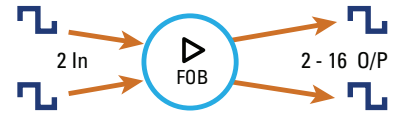
- Eliminate up to 64 resistors
- Save up to 110 mm^2 of area[†]
- As small as 9 mm^2
- Selectable output impedance 33, 85, and 100-Ω
- SSC compatible
- Flexible power rails 1.8V and 3.3V

[†] Compared to traditional HCSL outputs

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PCIe Gen7 Timing Solutions for CC, SRNS, SRIS Architectures

Function	Voltage	Part Number	Output Count	Zout (Ω)	Features	Package Type	Package Size (mm)
Fanout Buffer	3.3V	RC19002A	2	85/100 selectable	LOS, PDT, ACP, FSS	QFN-20	3 x 3
		RC19004A	4	85	LOS, PDT, ACP, FSS, SBI, Write Protect	QFN-24	4 x 4
		RC19008A	8			QFN-40	5 x 5
		RC19013A	13			QFN-56	7 x 7
		RC19016A	16			QFN-64	9 x 9
		RC19020A	20		LOS, PDT, ACP, FSS, SBI, Write Protect, DB2000QL pinout	GQFN-80	6 x 6
		9QXL2001C	20		DB2000QL for PCIe Gen6	GQFN-80	6 x 6
		RC19020A072	20		LOS, PDT, ACP, FSS, SBI, Write Protect, DB2000Q pinout	QFN-72	10 x 10
		9QXL2000C	20		DB2000Q for PCIe Gen6	QFN-72	10 x 10
		RC19024A	24		LOS, PDT, ACP, FSS, SBI, Write Protect	QFN-100	8 x 8
		RC19004A100	4	100	LOS, PDT, ACP, FSS, SBI, Write Protect	QFN-24	4 x 4
		RC19008A100	8			QFN-40	5 x 5
		RC19013A100	13			QFN-56	7 x 7
		RC19016A100	16			QFN-64	9 x 9
	1.8V	RC19102A	2	33/85/100 selectable	LOS, PDT, ACP, FSS	QFN-20	3 x 3
		RC19104A	4		LOS, PDT, ACP, FSS, Write Protect	QFN-24	4 x 4
		RC19108A	8			QFN-40	6 x 6
Multiplexer	3.3V	RC19202A	2	85/100 selectable	2-inputs, LOS, PDT, ACP, FSS, SBI, Write Protect	QFN-20	3 x 3
		RC19204A	4			QFN-28	4 x 4
		RC19208A	8			QFN-48	6 x 6
		RC19216A	16			GQFN-80	6 x 6
	1.8V	RC19302A	2	33/85/100 selectable	LOS, PDT, ACP, FSS	QFN-20	3 x 3
		RC19304A	4		LOS, PDT, ACP, FSS, Write Protect	QFN-24	4 x 4
		RC19308A	8			QFN-48	6 x 6
Generator	1.8V/2.5V/3.3V	RC21005B	5	Programmable	Integrated crystal option, IODx4, FODx3	LGA-32	4 x 4
		RC21008B	8			QFN-40 / LGA-40	5 x 5
		RC21012B	12			QFN-48 / LGA-48	6 x 6

PCIe Gen6 Timing Solutions for CC, SRNS, SRIS Architectures

Function	Voltage	Part Number	Output Count	Zout (Ω)	Features	Package Type	Package Size (mm)
Multiplexer	1.8V-3.3V	9DML4493	4	85/100 programmable	4-inputs, PDT	QFN-32	5 x 5
Generator	3.3V	9SQ440	20	85	CK440Q, PDT, SBI	QFN-100	8 x 8
	1.8V-3.3V	9FGV1002	4	85/100 programmable	Integrated crystal options available. See datasheet.	QFN-24	4 x 4
		9FGV1006	2			LGA-16	3 x 3
	3.3V	9FGL0241 9FGL0251	2	100/85	ZDB, Wake-On-LAN support	QFN-24	4 x 4
		9FGL0441 9FGL0451	4			QFN-32	5 x 5
		9FGL0641 9FGL0651	6			QFN-40	5 x 5
		9FGL0841 9FGL0851	8			QFN-48	6 x 6

Features description:

LOS: Loss of Signal output indicates when input clock is lost.

PDT: Power Down Tolerant pins can be driven even if VDD is not applied to the device.

ACP: Automatic Clock Parking places the outputs in a low/low state if the input clock is lost.

FSS: Flexible Startup Sequencing allows power, control pins and/or input clocks to be applied in any order.

SBI: 4-wire Side Band Interface, similar to the 9SQ440, allows rapid hardware control of output enables.

Write Protect: Software write protection bits prevent unintended SMBus writes.

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PCIe Gen5 Timing Solutions for CC, SRNS, SRIS Architectures

Function	Voltage	Part Number	PCIe Outputs	Zout (Ω)	Comments	Package Type	Package Size (mm)
Zero-Delay / Fan-out Buffer	3.3V	9ZXL0451	4	85		QFN-32	5 x 5
		9ZXL0631 9ZXL0651	6	33 85		QFN-40	5 x 5
		9ZXL0831 9ZXL0851	8	33 85	DB800ZL	QFN-48	6 x 6
		9ZXL1231 9ZXL1251	12	33 85	DB1200ZL	QFN-64	9 x 9
		9ZXL1530 9ZXL1550	15	33 85		QFN-64	9 x 9
		9ZXL1930 9ZXL1950	19	33 85	DB1900Z	QFN-72	10 x 10
	1.8V	9DBV0231 9DBV0241	2	33 100		QFN-24	4 x 4
		9DBV0431 9DBV0441	4	33 100		QFN-32	5 x 5
		9DBV0631 9DBV0641	6	33 100		QFN-40	5 x 5
		9DBV0831 9DBV0841	8	33 100		QFN-48	6 x 6
Fanout Buffer	1.8V	9DBV0531 9DBV0541	5	33 100		QFN-32	5 x 5
		9DBV0731 9DBV0741	7	33 100		QFN-40	5 x 5
		9DBV0931 9DBV0941	9	33 100		QFN-48	6 x 6
Multiplexer	3.3V	9DML0441 9DML0451	4	100 85	2 inputs	QFN-24	4 x 4
		9DML2855	8	85		QFN-48	6 x 6
		9ZML1245 9ZML1255	12	100 85		QFN-72	10 x 10
	1.8V	9DMV0131 9DMV0141	1	33 100	2 inputs	QFN-16	3 x 3

To request samples, download documentation or learn more visit: **renesas.com/pcietiming**

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