Product Change Notice (PCN)

Subject: Change Substrate Supplier to ASEE for PBGA-119 and PBGA-416
Publication Date: 2/21/2022
Effective Date: 5/21/2022

Revision Description:
Initial Release

Description of Change:
Renesas is changing the substrate supplier to ASEE, Taiwan as a result of the current supplier UMTC, Taiwan discontinued the manufacturing of substrate for product PBGA-119 and PBGA-416. ASEE has decades of experience and expertise in Flip Chip BGA/CSP substrates and is ranked among the top 10 worldwide substrate suppliers in terms of revenue. Refer to appendix for the company profile.

There will be no changes to the substrate design, physical dimensions and electrical performance. ASEE will be exactly the same as UMTC substrate in terms of form, fit and function.

Refer to appendix for comparison between the current substrate suppliers versus the newly qualified substrate supplier.

Affected Product List: Refer Appendix B.

Reason for Change:
The current substrate supplier discontinued the manufacturing line on the select packages.

Impact on Fit, Form, Function, Quality & Reliability:
The change will have no impact on the product form, fit, function, quality, reliability and environmental compliance of the products.

Product Identification:
Assembly Lot# traceable to the substrate material supplier

Qualification Status: Completed. Refer Appendix A
Sample Availability Date: 2/21/2021
Material Declaration: Available on request

Note:

1. Acknowledgement must be received by Renesas within 30 days or Renesas will consider the change as approved.
2. If timely acknowledgement is provided by Customer, then Customer shall have 90 days from the date of receipt of this PCN to make any objections to this PCN. If

Customer fails to make objections to this PCN within 90 days of the receipt of the PCN then Renesas will consider the PCN changes as approved.

3. If customer cannot accept the PCN then customer must provide Renesas with a last time buy demand and purchase order.

For additional information regarding this notice, please contact idt-pcn@lm.renesas.com

Appendix A – Comparison of Substrate Design and Materials

Descriptions	PBGA-416		PBGA-119	
	UMTC	ASEE	UMTC	ASEE
Finger Space (mm)	0.06 min.	0.06 min.	0.04 min.	0.04 min.
Finger Width (mm)	0.025 min.	0.025 min.	0.075 min.	0.075 min.
Trace Space (mm)	0.035 min.	0.035 min.	0.040 min.	0.040 min.
Trace Width (mm)	0.035 min.	0.035 min.	0.060 min.	0.060 min.
Ball Pad Opening (mm)	0.5+/-50	0.5+/-50	0.65+/-50	0.63+/-50
Ball Pad Metal Size (mm)	0.6+/-50	0.6+/-50	0.81+/-50	0.81+/-50
Core Thickness (mm)	0.15 (ref.)	0.15 (ref.)	0.15 (ref.)	0.15 (ref.)
Build-up	0.1 (ref.)	0.1 (ref.)	0.1 (ref.)	0.1 (ref.)
Hole Fill	PHP-900 IR-6	PHP-900 IR-6	PHP-900 IR-6	PHP-900 IR-6
Core Material	HL832NX-A	HL832NX-A	HL832NX-A	HL832NX-A
Build-up Material	GHPL830NX-A	GHPL830NX-A	GHPL830NX-A	GHPL830NX-A
Solder Mask	AUS308	AUS308	AUS308	AUS308
Surface Finish (Finger)	NiAu	NiAu	NiAu	NiAu
Surface Finish (Fiducials and External)	NiAu	NiAu	NiAu	NiAu

Appendix A – Comparison of Process Control

Substrate Process	QC Items	UMTC	ASEE
Lamination	Thickness	Yes	Yes
Mechanical Drill	Accuracy	Yes	Yes
Circuit Formation	Trace width	Yes	Yes
	Trace space	Yes	Yes
	Finger width	Yes	Yes
	Finger space	Yes	Yes
Cu Plating	Cu Thickness	Yes	Yes
Solder Mask	SM Thickness	Yes	Yes
	Total Thickness	Yes	Yes
	SRO Size	Yes	Yes
Surface Finish	Ni Thickness	Yes	Yes
	Au Thickness	Yes	Yes
	Finger Width	Yes	Yes
	Finger Space	Yes	Yes
Router	Strip Size	Yes	Yes

Appendix A - Qualification Results

Affected Packages: PBGA-119 and PBGA-416
Qual Vehicle: PBGA-416
Qual Plan & Results: Tests are in accordance with JEDEC47 recommended tests.

Test Descriptions	Test Method	Test Results (Rej/SS)		
		Lot 1	Lot 2	Lot 3
* Temperature Cycling (-55°C to 125°C, 700 cycles)	JESD22-A104	0/25	0/25	0/25
* Unbiased Temperature Humidity (uHAST) (130°C/85% RH, 96 Hrs)	JESD22-A110	0/25	0/25	-
* Temperature Humidity Bias (HAST) (130°C/85% RH, 96 Hrs)	JESD22-A110	-	-	0/25
Solder Ball Shear Test	JESD22-B117	0/5	0/5	0/5
Moisture Sensitivity Level, MSL	J-STD-20 / MSL 3, 260°C	0/25	0/25	0/25

**Tests were subjected to Preconditioning per JESD22-A113 prior to stress test*

Appendix B – Affected Product List

71V2556S100BG9	71V3556SA133BGGI8	71V3559S85BGI	71V3577S80BGG8
71V2556S133BG9	71V3556SA133BGI	71V3559S85BGI8	71V3577S80BGGI
71V2556SA100BG	71V3556SA133BGI8	71V35761SA166BG	71V3577S80BGGI8
71V2556SA100BG8	71V3556SA150BG	71V35761SA166BG8	71V3577S80BGI
71V2556SA100BGG	71V3556SA150BG8	71V35761SA166BGG	71V3577S80BGI8
71V2556SA100BGG8	71V3556SA150BGG	71V35761SA166BGG8	71V3577S85BG
71V2556SA100BGGI	71V3556SA150BGG8	71V35761SA166BGGI	71V3577S85BG/2799
71V2556SA100BGGI8	71V3556SA150BGGI	71V35761SA166BGGI8	71V3577S85BG8
71V2556SA100BGI	71V3556SA150BGGI8	71V35761SA166BGI	71V3577S85BG8/2799
71V2556SA100BGI8	71V3556SA166BG	71V35761SA166BGI8	71V3577S85BGG
71V2556SA133BG	71V3556SA166BG8	71V35761SA183BG	71V3577S85BGG8
71V2556SA133BG8	71V3556SA166BGG	71V35761SA183BG8	71V3577S85BGI
71V2556SA133BGG	71V3556SA166BGG8	71V35761SA183BGG	71V3577S85BGI8
71V2556SA133BGG8	71V3556SA166BGGI	71V35761SA183BGG8	71V65603S100BG
71V2556SA133BGI	71V3556SA166BGGI8	71V35761SA183BGGI	71V65603S100BG8
71V2556SA133BGI8	71V3556SA166BGI	71V35761SA183BGGI8	71V65603S100BGI
71V2556SA166BG	71V3556SA166BGI8	71V35761SA183BGI	71V65603S100BGI8
71V2556SA166BG8	71V3557S75BG	71V35761SA183BGI8	71V65603S133BG
71V25761S200BG	71V3557S75BG8	71V35761SA200BG	71V65603S133BG8
71V25761S200BG8	71V3557S80BG	71V35761SA200BG8	71V65603S133BGG
71V3556SA100BG	71V3557S80BG8	71V35761SA200BGG	71V65603S133BGG8
71V3556SA100BG8	71V3557S80BGI	71V35761SA200BGG8	71V65603S133BGGI
71V3556SA100BGG	71V3557S80BGI8	71V3577S75BG	71V65603S133BGGI8
71V3556SA100BGG8	71V3557S85BG	71V3577S75BG8	71V65603S133BGI
71V3556SA100BGGI	71V3557S85BG8	71V3577S75BGG	71V65603S133BGI8
71V3556SA100BGGI8	71V3557S85BGI	71V3577S75BGG8	71V65603S150BG
71V3556SA100BGI	71V3557S85BGI8	71V3577S75BGGI	71V65603S150BG8
71V3556SA100BGI8	71V3559S75BG	71V3577S75BGGI8	71V65603S150BGG
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71V3556SA133BGG8	71V3559S85BG	71V3577S80BG8	71V65703S75BG
71V3556SA133BGGI	71V3559S85BG8	71V3577S80BGG	71V65703S75BG8

71V65703S75BGG	71V65803S133BGG	71V67603S133BGGI8	71V67703S85BG8
71V65703S75BGG8	71V65803S133BGG8	71V67603S133BGI	71V67703S85BGG
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71V65703S85BGGI	71V65903S85BGG	71V67603S150BGI8	71V67803S150BG8
71V65703S85BGGI8	71V65903S85BGG8	71V67703S75BG	71V67803S166BG
71V65703S85BGI	71V65903S85BGGI	71V67703S75BG8	71V67803S166BG8
71V65703S85BGI8	71V67602S133BGG	71V67703S75BGG	82P2816BBBG
71V65803S100BG	71V67602S133BGG8	71V67703S75BGG8	82P2816BBBG8
71V65803S100BG8	71V67602S150BGG	71V67703S75BGGI	82P2910BBBG
71V65803S100BGG	71V67602S150BGG8	71V67703S75BGGI8	82P2910BBBG8
71V65803S100BGG8	71V67602S166BGG	71V67703S80BG	82P2917ABBG
71V65803S100BGGI	71V67602S166BGG8	71V67703S80BG8	82P2917ABBG8
71V65803S100BGGI8	71V67603S133BG	71V67703S80BGG	82P2917BBBG
71V65803S100BGI	71V67603S133BG8	71V67703S80BGG8	82P2917BBBG8
71V65803S100BGI8	71V67603S133BGG	71V67703S80BGGI	
71V65803S133BG	71V67603S133BGG8	71V67703S80BGGI8	
71V65803S133BG8	71V67603S133BGGI	71V67703S85BG	

ASE GROUP

ASE ELECTRONICS COMPANY PROFILE

ASEE
Business Promotion
Jan, 2022

CONTENT

- ASE GROUP
- MANUFACTURING LOCATION
- MISSION
- MAJOR MILESTONE
- ORGANIZATION
- PRODUCT LINE-UP & TECH ROADMAP
- KEY QUALITY CERTIFICATES

ASE GROUP

GLOBAL MANUFACTURING STRENGTH & LEADERSHIP

17 facilities

Worldwide - Assembly, Testing & Material, EMS

全球封裝、測試與材料廠及系統組裝廠

1984

Flagship factory in Kaohsiung, Taiwan

日月光高雄旗艦廠建立

68,000 (as of Dec. 31, 2017)

Employees across operations, engineering, R&D, and sales & marketing

運營、工程、研發設計、業務與行銷等員工人數

MANUFACTURING LOCATION

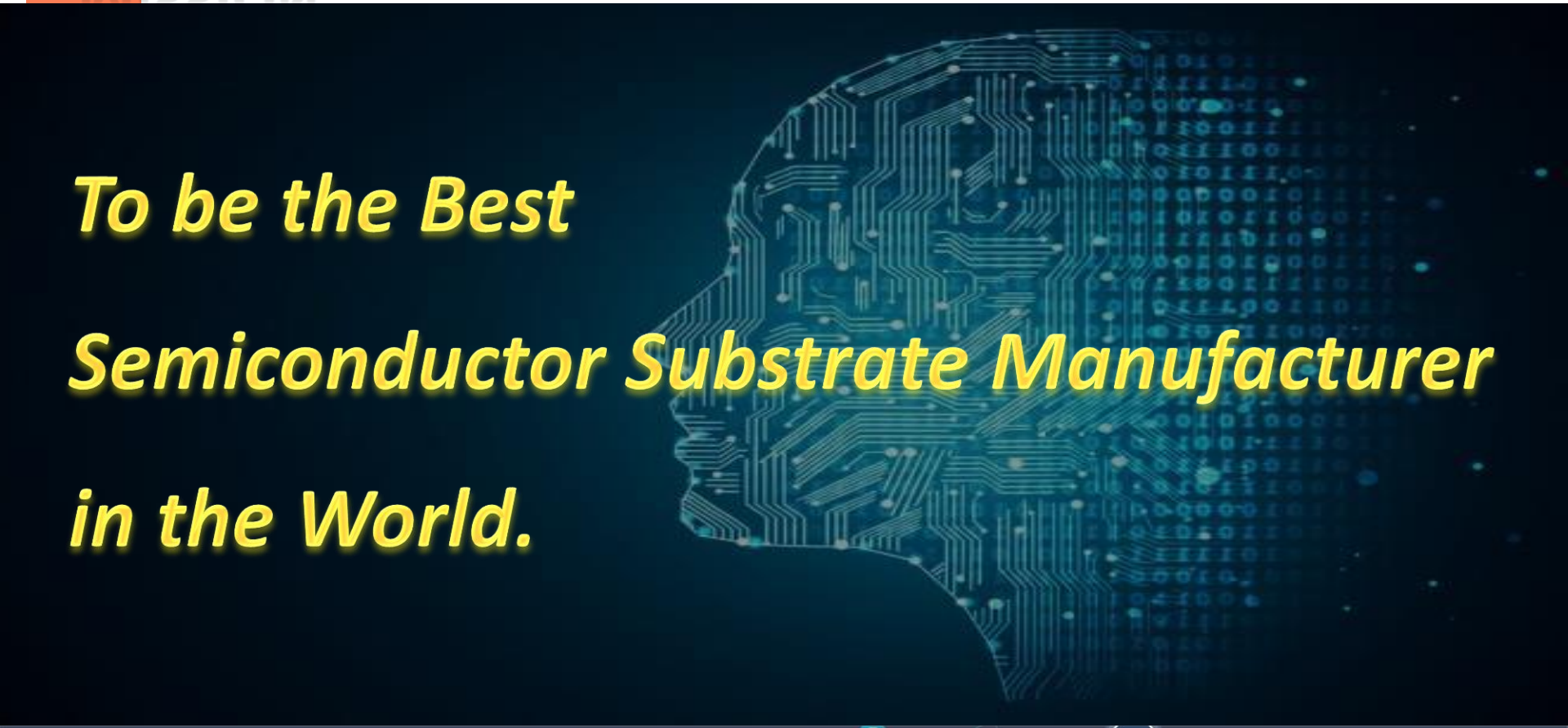
ASE Kaohsiung outlook

- Operation began from 1995
- Capacity: 38K M^2/Month
- Manpower : 1,000
- Manufacture: 650
- PE, RD & QA: 350

ASE Shanghai outlook

- Operation began from 2003
- Capacity: 57K M^2/Month
- Manpower : 1,500
- Manufacture: 1,120
- PE, RD & QA: 380

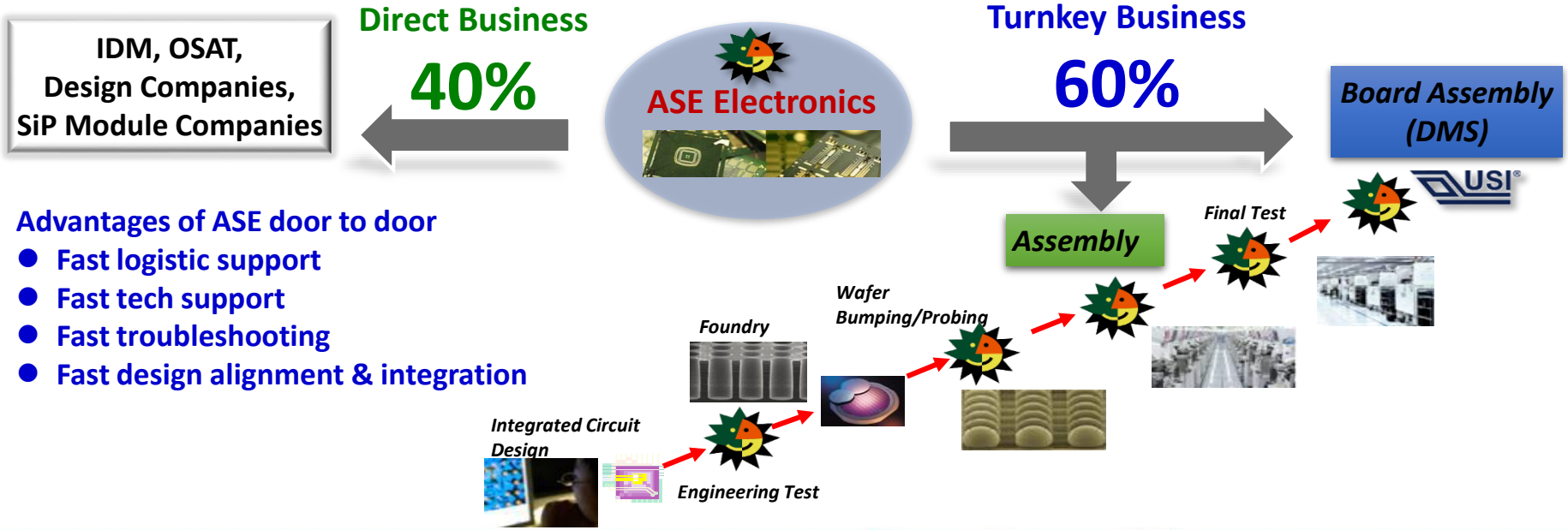
MISSION



ASEMTL ROLE IN SEMICONDUCTOR

Two business models

1. Turnkey: Provide door to door substrate service to ASEKH
2. Direct: Supply substrates to IDM customer & Design company.



Advantages of ASE door to door

- Fast logistic support
- Fast tech support
- Fast troubleshooting
- Fast design alignment & integration

MILESTONE KH SITE

Advanced

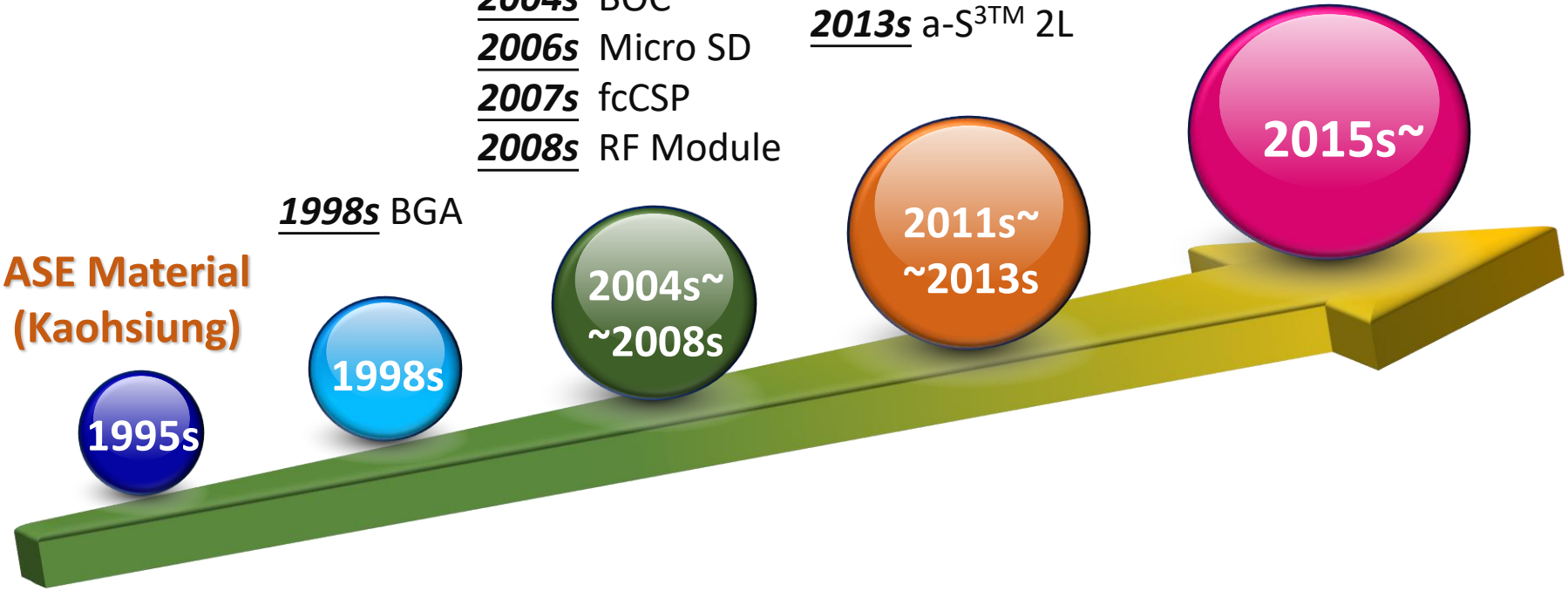
2015s SIP Module

2011s a-S^{3TM} 1L
2013s a-S^{3TM} 2L

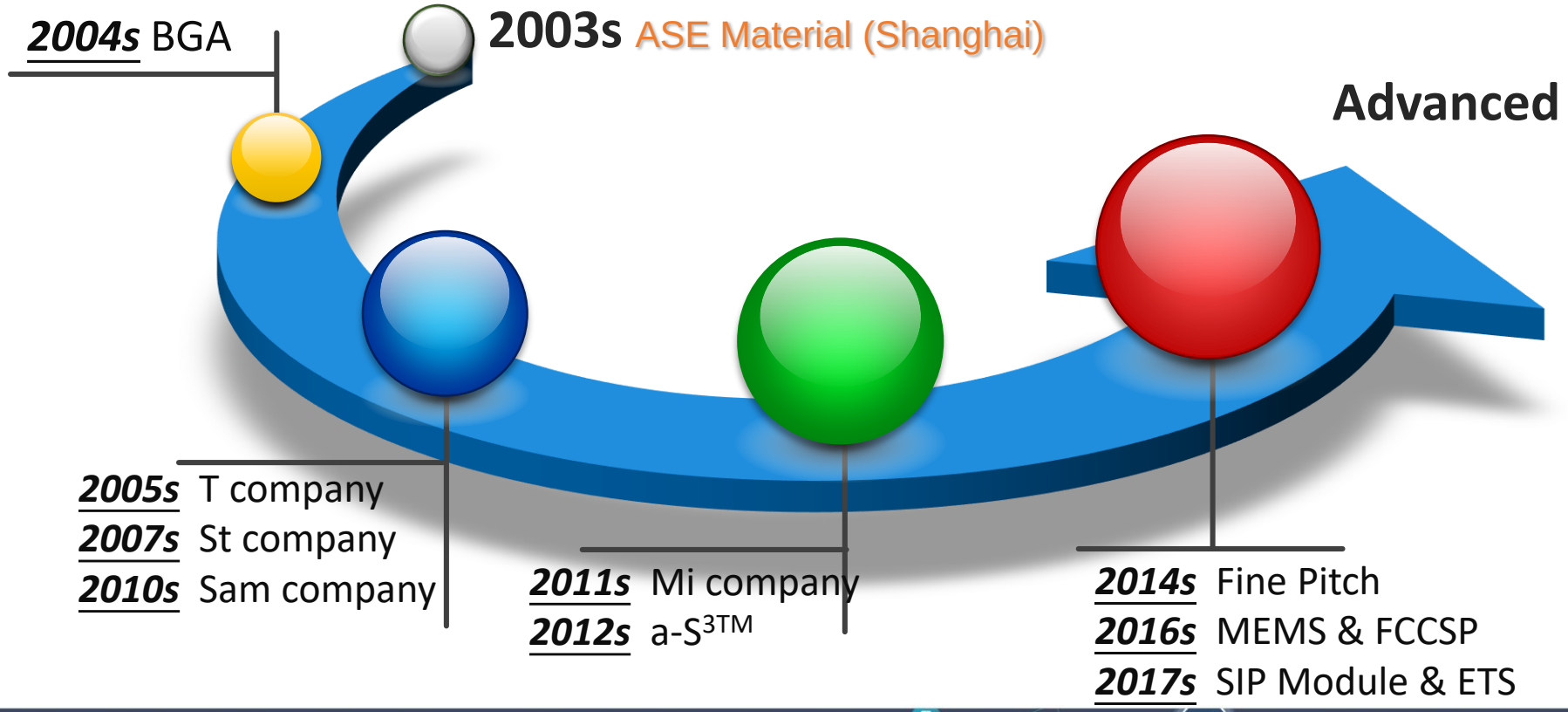
2004s BOC
2006s Micro SD
2007s fcCSP
2008s RF Module

1998s BGA

ASE Material (Kaohsiung)



MILESTONE SH SITE



MBU ORGANIZATION

ASE Material Business Unit

GM JJ Lee

SH Site

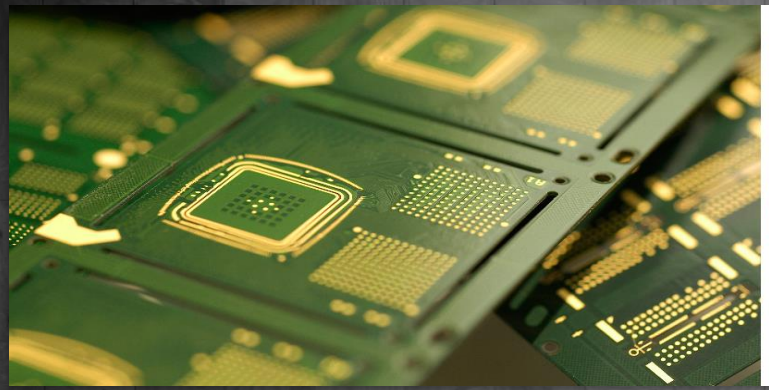
GM Chung Lin

KH Site

VP DY Chen

MBU ORGANIZATION

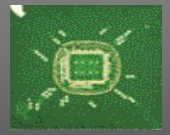
PRODUCT LINE-UP

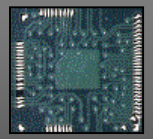


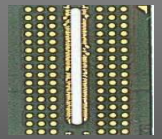
- Wire Bond Substrate
- Flip Chip Substrate
- Advanced Substrate

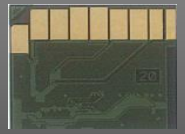
PRODUCT LINE-UP

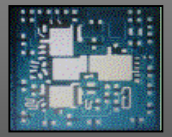
Wire Bond Substrate

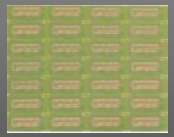

PBGA


CSP


BOC


Memory Module

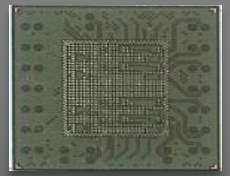

Module


a-S³

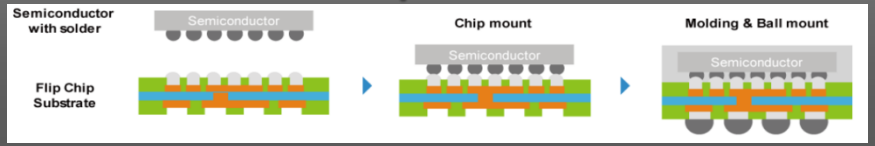
- PBGA & CSP Substrate
- BOC (DDR Substrate)
- Memory Card Substrate
- Module Substrate
- a-S³ (Single Sided Substrate)

PRODUCT LINE-UP

Flip Chip Substrate



✓High I/O
✓High accuracy
✓Low profile



■ 1L ETS

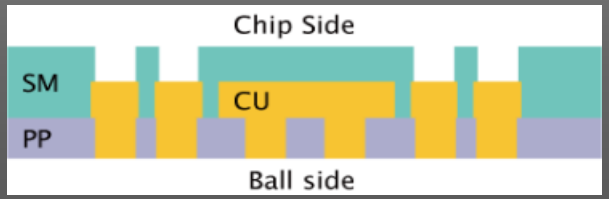
- Very thin substrate & advanced pattern design
- Same process flow in assembly (even though thin substrate)
- Cost effective fan-out solution

■ EPP + EPS

- Passives embedded in coreless substrate
- Fine pattern capability in embedded trace layer
- Double-side interconnection for flexible design
- Good electrical performance

PRODUCT LINE-UP

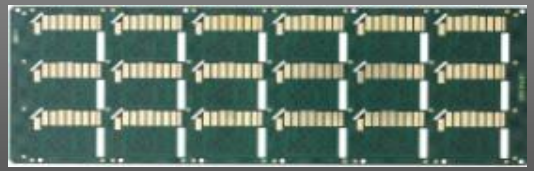
a-S³ (Single Sided Substrate)



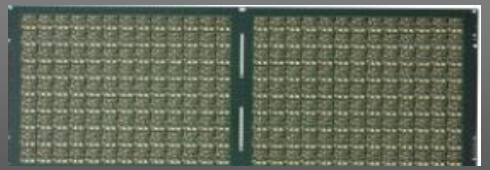
- **a-S³ (Single Sided Substrate)**
  Made by single side build-up flow
  - Cost reduction
  - Low profile

PRODUCT LINE-UP

Memory Card Substrate



Module Substrate



■ Memory Card Substrate

- High efficient substrate design
- Plating facility for soft Au for wire-bonding and hard Au plating for permanent coating
- Warpage control
- Substrate total thickness down to 0.1mm
- Etch Back

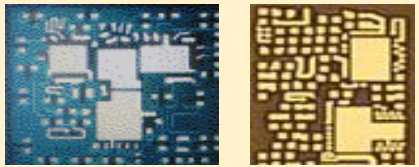
■ Module Substrate

- Compact size
- Cost effective
- Light weight
- Integration of multiple devices in one
- Better performance in terms of connectivity and electrically making electrical paths shorter

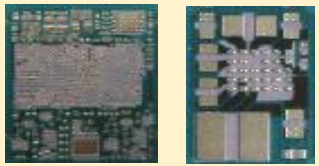
ASEM-KH Substrate Category

SiP Module

Layer : 1+2+1 / 2+2+2 / 3+2+3



RF Module

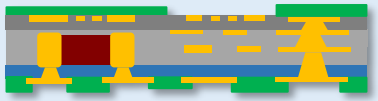


SiP Module

Wireless Module / AP / RF / Memory

EPS/EDS

Layer : 1L / 2L / 4L / 1+2+1



Chip Last Fan-Out

2L ETS+EPS

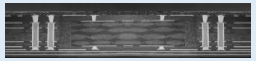
4L ETS+EPS

Chip First Fan-Out

a-EASI

1+2+1 EPS

4L EDS

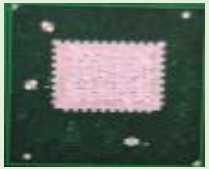


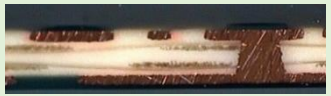
8L EPS

Power Management / ATV / Wireless

fcCSP

Layer : 2L/ 1+1+1 / 1+2+1



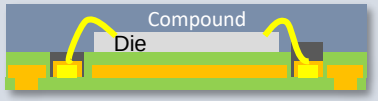


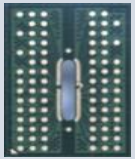
fcCSP

Graphic / DRAM / Consumer 3C / DSP / Smart phone

W/B

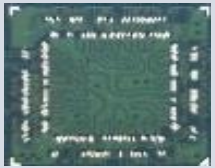
Layer : 1L / 2L / 3L / 4L / 1+2+1 / 2+2+2





BOC

PBGA



CSP

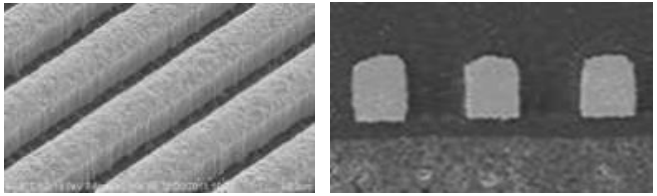
a-S^3 1L

Consumer 3C / DRAM / Flash / eMCP

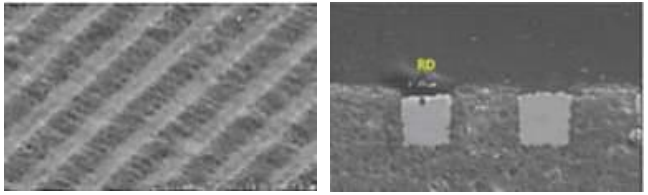
Pattern Technology

Item		HVM	NPI	2022	2023	2024
Pattern L/S	Subtractive	30/30	25/30	25/30	25/25	20/25
	mSAP	18/18	16/16	16/16	12/16	10/15
	ETS	13/13	8/10	8/10	6/8	5/5
Bond Finger FP/FW		80/40	75/35	65/35	60/30	55/30

※ mSAP : modified Semi - Additive
Line / Space : 18um / 18um



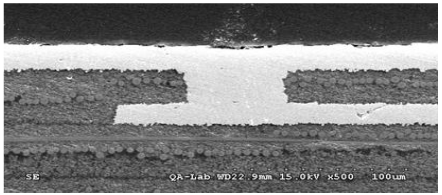
※ ETS: Embedded Trace Substrate
Line / Space : 8um / 10um



Via Capability

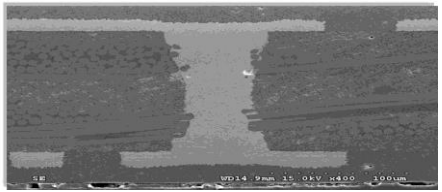
Item		HVM	NPI	2022	2023	2024
Via/Pad	IVH/Pad	90/180	75/150	75/125	75/115	70/105
	BVH/Pad	65/100	60/100	60/90	60/90	55/85
	X-Via/Pad	75/175	75/150	75/125	75/115	75/115
	PTH/Pad	100/200	100/175	90/170	90/170	80/170

※ BVH Cu filled



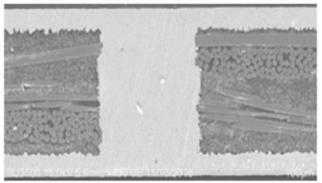
Via Diameter : 60 +/- 15um
Cu THK : 18+/- 4 um
PP : 25 um
Dimple Depth: Max.10um

※ X-Via Cu Filled



Via Diameter: 75 +/- 15um
Cu THK : 18+/- 4 um
Core : 150 um
Dimple Depth: Max.10um

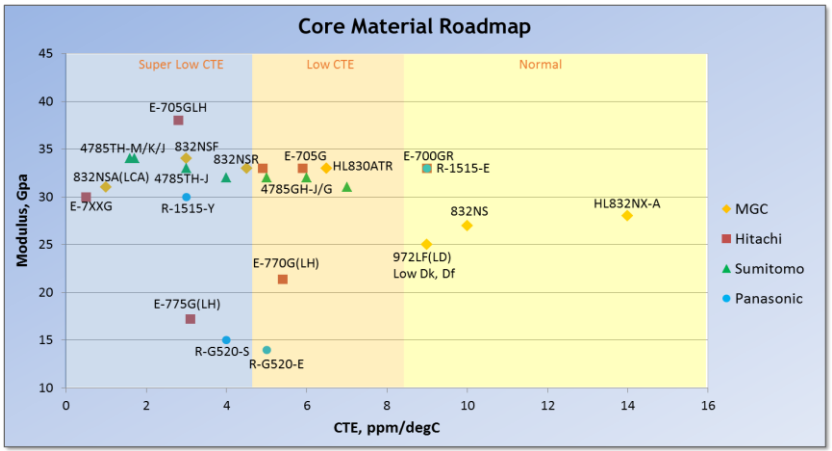
※ PTH Cu filled

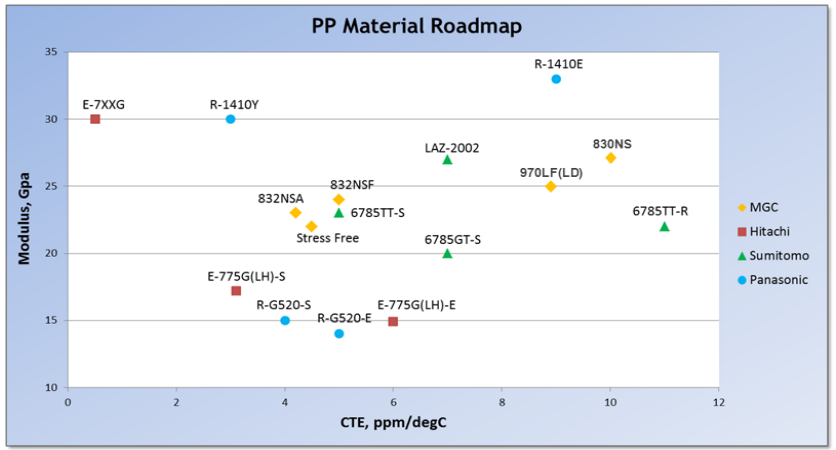


Via Diameter : 100 +/- 30um
Core : 100 um
Dimple Depth: Max.10um

Core Material

Item		HVM	LVM	2022	2023	2024
Dielectric layer	PP thickness	25	22	20	17	15
	CCL thickness	40	→	40	40	40
	Dk/Df	4.4/0.006	→	<3/0.003	<2.5/0.001	
	CTE	<10	→	<5	<3	



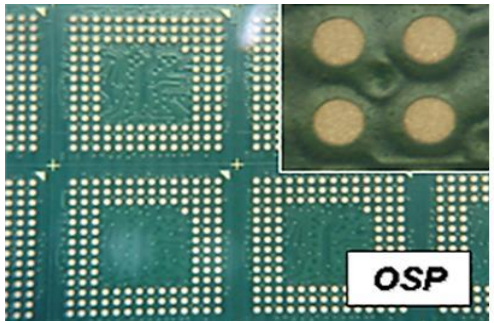


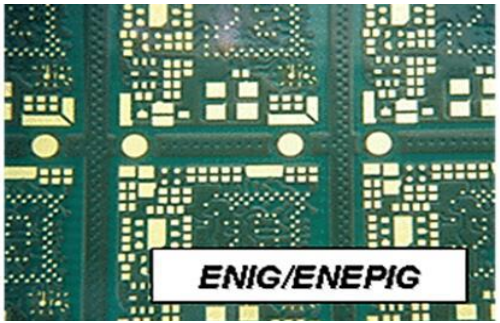
Cu thickness

Item	HVM	NPI	2022	2023	2024
Tenting	10,12,13,15,18 Min 13,15,17,18,20 ±5	13,15,17,18,20±4.5	13,15,17,18,20 ±4.5	13,15,17,18,20 ±4	
MSAP	17 ±5	15 ±4	15±4	13,15 ±3	

Surface Finish Technology

Item	HVM	LVM	2022	2023	2024
SR	AUS308 / AUS320 / AUS410 / SR1	D10ME / AUS320E	SR1-Z / MG1-Z / SR3 / AZ3-F		
Min. SRO	80	70	60	60	40
SR Registration	±15	±12.5	±10	±10	±8
Metal Finish	NiAu / ENIG / ENEPIG / OSP (TAMURA/SHIKOKU)	→	NiAu / ENIG / ENEPIG / OSP (TAMURA/SHIKOKU)		

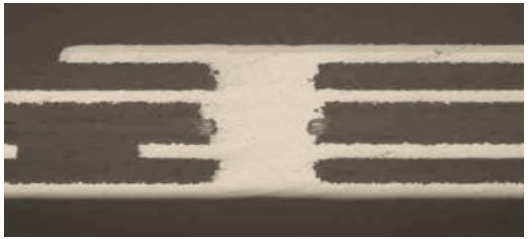




Stackups

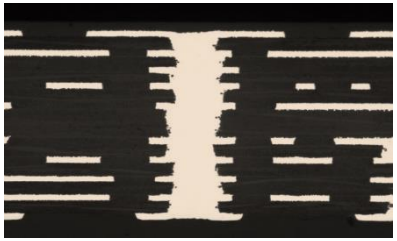
Item	HVM	LVM	2022	2023	2024
Cored Layer structure	2/4/6 1+2+1/2+2+2/3+2+3	4+2+4	5+2+5		
Coreless Layer structure	1/2/3/4/5	6/8	10		

※ Cored 1+2+1 layer



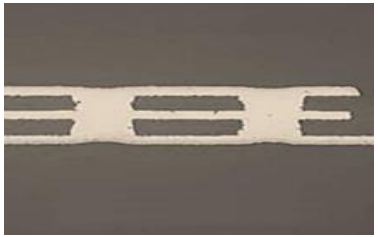
Stack via, Cu filled
Core: 40um
PP: 20 um
Via : 70 um

※ Cored 4+2+4 Layer



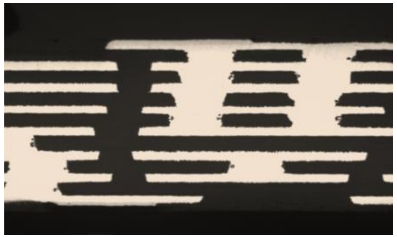
Stack via, Cu filled
Core: 50um
PP: 20 um
Via : 80 um

※Coreless 3L



Stack via, Cu filled
Coreless 3 Layer / 8 Layer
PP: 20 um
Via : 75 um

※Coreless 8L



KEY QUALITY CERTIFICATES

- 1999
  ISO 9001:2015
- 2003
  IATF 16949:2016
- 2007
  QC 080000
- 2016
  ISO 26262:2018

Thank You

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