Product Change Notice

(PCN tracking number : CST-R2-AJ095 Rev.1.0)

August 5, 2016

To: Valued RENESAS Customer,

Renesas Product Summary: Standard SRAM (SOP, µTSOP and FBGA) products.

Change Description:
1. Site change of Final-test process
2. Product integration by EOL of "-5SR, -7SI, -7SR" products and by part name unification to "-5SI" product

Reason for Change:
1. Due to obsolescence of manufacturing equipment
2. For long-time, stable supply by improvement of mass production efficiency

Identification: Identifiable by RENESAS internal code, printed on the shipping label

Anticipated Impact:
1. Packing specification is changed accompanied with the site change of Final-test process
2. Electrical characteristics of "-5SI" product is completely upper-compatible with "-5SR, -7SI, -7SR" products.

Date of Change: From January 2017 onward

Schedule:
1. Regarding the site change of Final-test process (excluding EOL products),
   Mass production of the post-change products from January 2017, in order of preparations.

2. Regarding the EOL of "-5SR, -7SI, -7SR" products,
   Last-Time-Buy quantity forecast to RENESAS: June, 2017
   Last Time to Order: December, 2017
   Last Time to Ship: December, 2018
   Commercial samples of unified "-5SI" product: From December, 2016

Supplemental Information: Please see the page 3 to 5 and the attachments (Appendix for CST-R2-AJ095).

Contact: General Purpose Analog and Power Solution Department 3,
General Purpose Analog and Power Business Division,
2nd Solution Business Unit

Internal Reference:

Attachments: Appendix for CST-R2-AJ095

In case of any questions, please contact your Renesas sales representative.

Customer Response (to be returned by email or mail)

☐ Acknowledge	Company: _____
☐ Acceptable	Name & Position: _____
☐ Unacceptable (pls. comment)	Email: _____
☐ Not applicable	Phone: _____

Note: Acknowledgement must be received by Renesas within 30 days of delivery of the PCN or Renesas will consider the change as approved. If timely acknowledgement is provided by Customer, then Customer shall have 90 days from the date of receipt of this PCN in which to make any objections to the PCN. If Customer fails to make objections to this PCN within 90 days of the receipt of the PCN then Renesas will consider the PCN changes as approved. If customer cannot accept the PCN then customer must provide Renesas with a last time buy demand and purchase order.

Comments

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Signature of customer

1. Background of Change

Renesas announces 2 types of Product Changes on Standard SRAM (SOP, µTSOP and FBGA) products.
One is a site change of final-test process due to obsolescence of manufacturing equipment.
The other is a product integration by EOL of "-5SR, -7SI, -7SR" products and by part name unification to "-5SI" product. It aims for long-time, stable supply by improvement of mass production efficiency.
We greatly appreciate your kind understanding and early approval for this notification.

2. Details of Change

(1) The site of Final-test process is transferred from "Renesas Semiconductor Beijing" to "Powertech Technology Inc."

(2) Regarding the EOL of "-5SR, -7SI, -7SR" products,
(a) "Access and Temperature grades" of "-5SR, -7SI, -7SR" in 256Kb to 4Mb Low Power SRAM products are put to EOL, and part name of the products are unified to "-5SI".
(b) Electrical characteristics (DC/AC) of unified "-5SI" product are completely upper-compatible with "-5SR, -7SI, -7SR" products.
(c) The unified "-5SI" products are processed under the post-change condition as described in above (1).
(d) "Access and Temperature grades" which is laser-marked on package's surface, is changed from "-5SR, -7SI, -7SR" to "-5SI."

(3) Regarding these changes,
(a) There are no changes in the site of Front-end (Wafer) process or revision of photomasks.
(b) There are no changes in the site of Assembly process or assembly materials.
(c) There are no changes in Reliability and quality level.
(d) There are no changes in Electrical characteristics (DC/AC), excluding "-5SR, -7SI, -7SR" of pre-change products.
(e) Packing specification is changed. For more detailed information, see the appendix for CST-R2-AJ095.

Comparison

Item		Pre Change	Post Change
Final test	Company	Renesas Semiconductor Beijing	Powertech Technology Inc.
	Country	China	Taiwan
Packing specification	Magazine packing (Tube packing)	Please see the appendix.	Please see the appendix.
	Tray packing	Please see the appendix.	Please see the appendix.
	Tape & Reel packing	Please see the appendix.	Please see the appendix.

3. Release Support and Milestones

Sample submission	(1) Regarding the site change of Back-end process (excluding EOL products), we are not planning to supply samples. (2) Regarding the EOL of "-5SR, -7SI, -7SR" products, we will supply commercial samples of unified "-5SI" from December, 2016.
Renesas report	(1) Regarding the site change of Back-end process (excluding EOL products), we are not planning to submit the reliability report. (2) Regarding the EOL of "-5SR, -7SI, -7SR" products, we will submit the reliability report of unified "-5SI" from December, 2016.

4. Identification

Identifiable by RENESAS internal code, printed on the shipping label

5. Schedule

(1) Regarding the site change of Back-end process (excluding EOL products),
Mass production of the post-change products from January 2017, in order of preparations.

(2) Regarding the EOL of "-5SR, -7SI, -7SR" products,
Last-Time-Buy quantity forecast to RENESAS: June, 2017
Last Time to Order: December, 2017
Last Time to Ship: December, 2018
Commercial samples of unified "-5SI" product: From December, 2016

6. Supplemental Information

Please see the attachments (Appendix for CST-R2-AJ095).

7. Product list

Package type	Product Type (Memory Cap., Supply Voltage)	Orderable part name	
		Pre Change	Post Change
28pin-SOP	256Kb 5V	R1LP5256ESP-5SI, -5SR, -7SI, -7SR#B0 / #S0	R1LP5256ESP-5SI#B0 / #S0
	256Kb 3V	R1LV5256ESP-5SI, -5SR, -7SI, -7SR#B0 / #S0	R1LV5256ESP-5SI#B0 / #S0
32pin-SOP	1Mb 5V	R1LP0108ESN-5SI, -5SR, -7SI, -7SR#B0 / #S0	R1LP0108ESN-5SI#B0 / #S0
	1Mb 3V	R1LV0108ESN-5SI, -5SR, -7SI, -7SR#B0 / #S0	R1LV0108ESN-5SI#B0 / #S0
	4Mb 5V	R1LP0408DSP-5SI, -5SR, -7SI, -7SR#B0 / #S0	R1LP0408DSP-5SI#B0 / #S0
	4Mb 3V	RMLV0408EGSP-4S2#CA0 / #HA0	←
48ball-FBGA	4Mb 3V	RMLV0416EGBG-4S2#AC0 / #KC0	←
	8Mb 3V	RMLV0816BGBG-4S2#AC0 / #KC0	←
	16Mb 3V	R1LV1616HBG-4SI, 5SI#B0 / #S0	←
		RMLV1616AGBG-5S2#AC0 / #KC0	←
	32Mb 3V	RMWV3216AGBG-5S2#AC0 / #KC0	←
	64Mb 3V	R1WV6416RBG-5SI#B0 / #S0	←
52pin-µTSOP	8Mb 3V	RMLV0816BGSD-4S2#AC0 / #HC0	←
	16Mb 3V	RMLV1616AGSD-5S2#AC0 / #HC0	←
	32Mb 3V	R1LV3216RSD-5SI#B0 / #S0	←
	64Mb 3V	R1WV6416RSD-5SI#B0 / #S0	←

To: Valued RENESAS customer,

General Purpose Analog and Power Solution Department 3
General Purpose Analog and Power Business Division
2nd Solution Business Unit
Renesas Electronics Corporation

August 5, 2016

Appendix for CST-R2-AJ095

(Standard SRAM (SOP, µTSOP, FBGA) products)

This appendix states the detailed information of PCN: CST-R2-AJ095 (Site change of Final-test process and product integration by EOL of “-5SR, -7SI, -7SR” products).

Contents

1. Product List

(1) 28pin-SOP, 32pin-SOP package

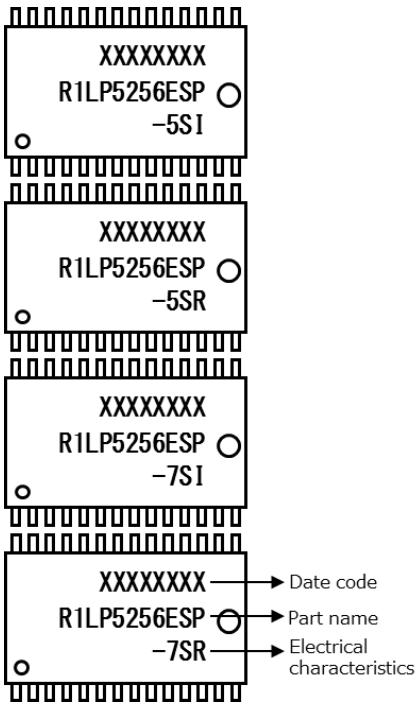
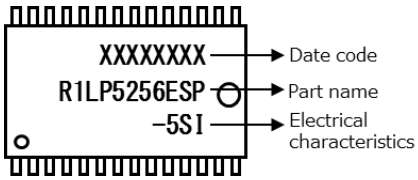
Package Type	Product Type (Memory Cap., Supply Voltage)	Organi-zation (bit)	Orderable Part Name		Packing Type	Page No. of Comparison Table
			Pre Change	**Post Change**		
28pin-SOP	256Kb 5V	x8	R1LP5256ESP-5SI#B0	R1LP5256ESP-5SI#B0	Magazine	p.4, p.20, pp.21-22
			R1LP5256ESP-5SR#B0			
			R1LP5256ESP-7SI#B0			
			R1LP5256ESP-7SR#B0			
			R1LP5256ESP-5SI#S0	R1LP5256ESP-5SI#S0	Tape & Reel	
			R1LP5256ESP-5SR#S0			
			R1LP5256ESP-7SI#S0			
			R1LP5256ESP-7SR#S0			
	256Kb 3V	x8	R1LV5256ESP-5SI#B0	R1LV5256ESP-5SI#B0	Magazine	p.5, p.20, pp.23-24
			R1LV5256ESP-5SR#B0			
			R1LV5256ESP-7SI#B0			
			R1LV5256ESP-7SR#B0			
			R1LV5256ESP-5SI#S0	R1LV5256ESP-5SI#S0	Tape & Reel	
			R1LV5256ESP-5SR#S0			
			R1LV5256ESP-7SI#S0			
			R1LV5256ESP-7SR#S0			
32pin-SOP	1Mb 5V	x8	R1LP0108ESN-5SI#B0	R1LP0108ESN-5SI#B0	Magazine	p.6, p.20, pp.25-26
			R1LP0108ESN-5SR#B0			
			R1LP0108ESN-7SI#B0			
			R1LP0108ESN-7SR#B0			
			R1LP0108ESN-5SI#S0	R1LP0108ESN-5SI#S0	Tape & Reel	
			R1LP0108ESN-5SR#S0			
			R1LP0108ESN-7SI#S0			
			R1LP0108ESN-7SR#S0			
	1Mb 3V	X8	R1LV0108ESN-5SI#B0	R1LV0108ESN-5SI#B0	Magazine	p.7, p.20, pp.27-28
			R1LV0108ESN-5SR#B0			
			R1LV0108ESN-7SI#B0			
			R1LV0108ESN-7SR#B0			
			R1LV0108ESN-5SI#S0	R1LV0108ESN-5SI#S0	Tape & Reel	
			R1LV0108ESN-5SR#S0			
			R1LV0108ESN-7SI#S0			
			R1LV0108ESN-7SR#S0			
	4Mb 5V	X8	R1LP0408DSP-5SI#B0	R1LP0408DSP-5SI#B0	Magazine	p.8, p.20, pp.29-30
			R1LP0408DSP-5SR#B0			
			R1LP0408DSP-7SI#B0			
			R1LP0408DSP-7SR#B0			
			R1LP0408DSP-5SI#S0	R1LP0408DSP-5SI#S0	Tape & Reel	
			R1LP0408DSP-5SR#S0			
			R1LP0408DSP-7SI#S0			
			R1LP0408DSP-7SR#S0			
	4Mb 3V	x8	RMLV0408EGSP-4S2#CA0	←	Magazine	p.9
			RMLV0408EGSP-4S2#HA0	←	Tape & Reel	

(2) 48ball-FBGA, 52pin-µTSOP package

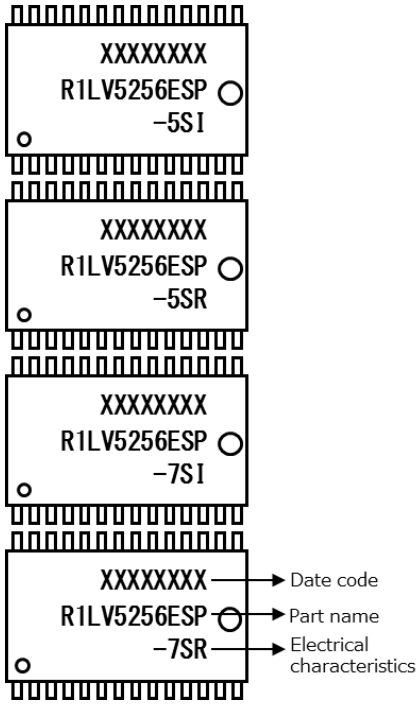
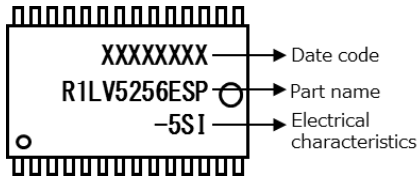
Package Type	Product Type (Memory Cap., Supply Voltage)	Organi-zation (bit)	Orderable Part Name		Packing Type	Page No. of Comparison Table
			Pre Change	**Post Change**		
48ball-FBGA	4Mb 3V	x16	RMLV0416EGBG-4S2#AC0	←	Tray	p.10
			RMLV0416EGBG-4S2#KC0	←	Tape & Reel	
	8Mb 3V	x16	RMLV0816BGBG-4S2#AC0	←	Tray	p.11
			RMLV0816BGBG-4S2#KC0	←	Tape & Reel	
	16Mb 3V	x16	R1LV1616HBG-4SI#B0	←	Tray	p.12
			R1LV1616HBG-4SI#S0	←	Tape & Reel	
			R1LV1616HBG-5SI#B0	←	Tray	
			R1LV1616HBG-5SI#S0	←	Tape & Reel	
			RMLV1616AGBG-5S2#AC0	←	Tray	p.13
			RMLV1616AGBG-5S2#KC0	←	Tape & Reel	
	32Mb 3V	x16	RMWV3216AGBG-5S2#AC0	←	Tray	p.14
			RMWV3216AGBG-5S2#KC0	←	Tape & Reel	
	64Mb 3V	x16	R1WV6416RBG-5SI#B0	←	Tray	p.15
			R1WV6416RBG-5SI#S0	←	Tape & Reel	
52pin-µTSOP	8Mb 3V	x16	RMLV0816BGSD-4S2#AC0	←	Tray	p.16
			RMLV0816BGSD-4S2#HC0	←	Tape & Reel	
	16Mb 3V	x16	RMLV1616AGSD-5S2#AC0	←	Tray	p.17
			RMLV1616AGSD-5S2#HC0	←	Tape & Reel	
	32Mb 3V	x16	R1LV3216RSD-5SI#B0	←	Tray	p.18
			R1LV3216RSD-5SI#S0	←	Tape & Reel	
	64Mb 3V	x16	R1WV6416RSD-5SI#B0	←	Tray	p.19
			R1WV6416RSD-5SI#S0	←	Tape & Reel	

2. Comparison table

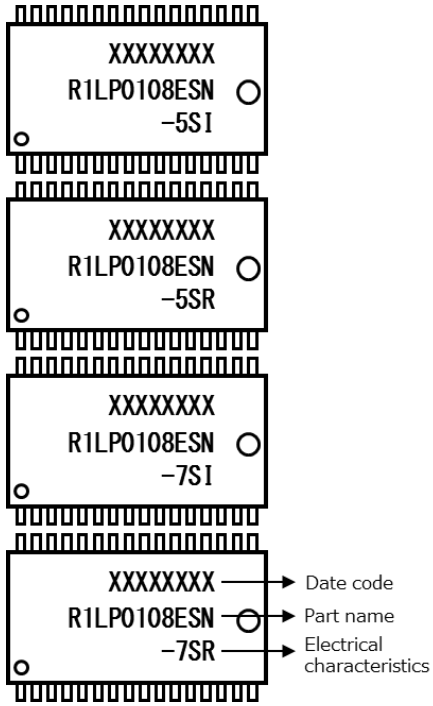
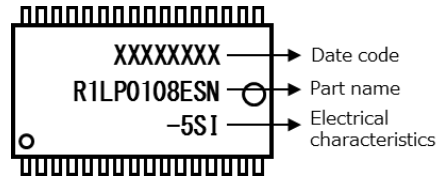
(1) 28pin-SOP 256Kb(5V) Part name : R1LP5256ESP

Item		Pre Change	Post Change
Orderable part name		R1LP5256ESP-5SI/-5SR/-7SI/-7SR#B0 (Magazine packing)	R1LP5256ESP-5SI#B0 (Magazine packing)
		R1LP5256ESP-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LP5256ESP-5SI#S0 (Tape & Reel packing)
Assembly line		Renesas Semiconductor Beijing (China)	←
JEITA Package Code		P-SOP28-8.4x17.5-1.27	←
Package marking specification			
Assembly Material	Lead frame material	42Alloy	←
	Lead plating	Sn-Cu	←
	Die bonding	Epoxy paste	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-included)	←
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Magazine packing	Packing specification	Current specification	New specification
	Magazine	Magagine code : MP024PC	←
	Storage number	30pcs/magazine	←
	Number of magazines (Max.)	40 magazines	←
	Inner box size (LxWxH)	600mm x 172mm x 77mm	595mm x 170mm x 72mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Emboss type name : MTE2416H-28P2W-C	←
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	347mm x 368mm x 54mm	362mm x 340mm x 60mm
Moisture-proof performance		MSL 2	←
Shipping label		Current specification	No change in format (Changes in Renesas internal code)

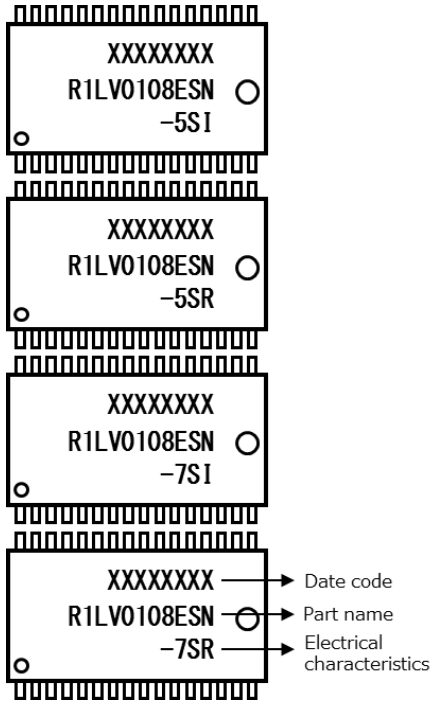
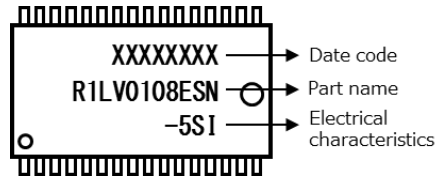
(2) 28pin-SOP 256Kb(3V) Part name : R1LV5256ESP

Item		Pre Change	Post Change
Orderable part name		R1LV5256ESP-5SI/-5SR/-7SI/-7SR#B0 (Magazine packing)	R1LV5256ESP-5SI#B0 (Magazine packing)
		R1LV5256ESP-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LV5256ESP-5SI#S0 (Tape & Reel packing)
Assembly line		Renesas Semiconductor Beijing (China)	←
JEITA Package Code		P-SOP28-8.4x17.5-1.27	←
Package marking specification			
Assembly Material	Lead frame material	42Alloy	←
	Lead plating	Sn-Cu	←
	Die bonding	Epoxy paste	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-included)	←
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Magazine packing	Packing specification	Current specification	New specification
	Magazine	Magagine code : MP024PC	←
	Storage number	30pcs/magazine	←
	Number of magazines (Max.)	40 magazines	←
	Inner box size (LxWxH)	600mm x 172mm x 77mm	595mm x 170mm x 72mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Emboss type name : MTE2416H-28P2W-C	←
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	347mm x 368mm x 54mm	362mm x 340mm x 60mm
Moisture-proof performance		MSL 2	←
Shipping label		Current specification	No change in format (Changes in Renesas internal code)

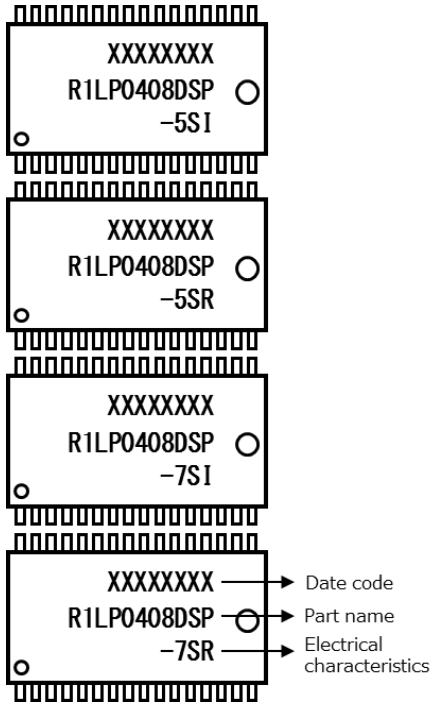
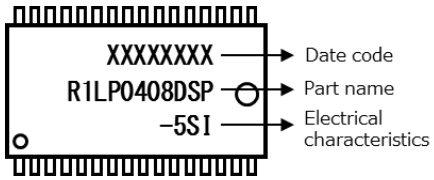
(3) 32pin-SOP 1Mb(5V) Part name : R1LP0108ESN

Item		Pre Change	Post Change
Orderable part name		R1LP0108ESN-5SI/-5SR/-7SI/-7SR#B0 (Magazine packing)	R1LP0108ESN-5SI#B0 (Magazine packing)
		R1LP0108ESN-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LP0108ESN-5SI#S0 (Tape & Reel packing)
Assembly line		Renesas Semiconductor Beijing (China)	←
JEITA Package Code		P-SOP32-11.4x20.75-1.27	←
Package marking specification			
Assembly Material	Lead frame material	Cu	←
	Lead plating	Sn (pure tin)	←
	Die bonding	Epoxy paste	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-free)	←
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Magazine packing	Packing specification	Current specification	New specification
	Magazine	Magagine code : MP525PC	←
	Storage number	25pcs/magazine	←
	Number of magazines (Max.)	36 magazines	←
	Inner box size (LxWxH)	600mm x 172mm x 77mm	595mm x 170mm x 72mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Emboss type name : MTE3216H-32P2M-A	←
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	347mm x 368mm x 54mm	362mm x 340mm x 60mm
Moisture-proof performance		MSL 3	←
Shipping label		Current specification	No change in format (Changes in Renesas internal code)

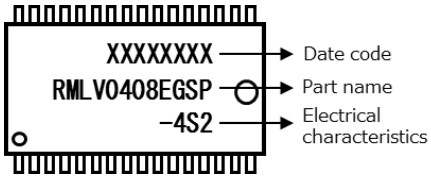
(4) 32pin-SOP 1Mb(3V) Part name : R1LV0108ESN

Item		Pre Change	Post Change
Orderable part name		R1LV0108ESN-5SI/-5SR/-7SI/-7SR#B0 (Magazine packing)	R1LV0108ESN-5SI#B0 (Magazine packing)
		R1LV0108ESN-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LV0108ESN-5SI#S0 (Tape & Reel packing)
Assembly line		Renesas Semiconductor Beijing (China)	←
JEITA Package Code		P-SOP32-11.4x20.75-1.27	←
Package marking specification			
Assembly Material	Lead frame material	Cu	←
	Lead plating	Sn (pure tin)	←
	Die bonding	Epoxy paste	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-free)	←
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Magazine packing	Packing specification	Current specification	New specification
	Magazine	Magagine code : MP525PC	←
	Storage number	25pcs/magazine	←
	Number of magazines (Max.)	36 magazines	←
	Inner box size (LxWxH)	600mm x 172mm x 77mm	595mm x 170mm x 72mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Emboss type name : MTE3216H-32P2M-A	←
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	347mm x 368mm x 54mm	362mm x 340mm x 60mm
Moisture-proof performance		MSL 3	←
Shipping label		Current specification	No change in format (Changes in Renesas internal code)

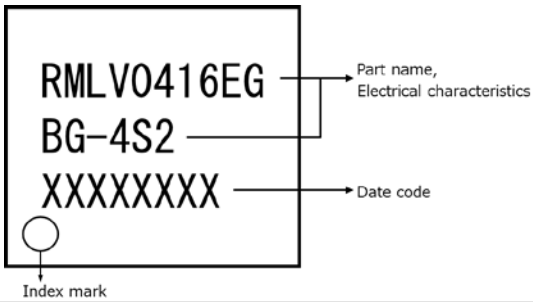
(5) 32pin-SOP 4Mb(5V) Part name : R1LP0408DSP

Item		Pre Change	Post Change
Orderable part name		R1LP0408DSP-5SI/-5SR/-7SI/-7SR#B0 (Magazine packing)	R1LP0408DSP-5SI#B0 (Magazine packing)
		R1LP0408DSP-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LP0408DSP-5SI#S0 (Tape & Reel packing)
Assembly line		Renesas Semiconductor Beijing (China)	←
JEITA Package Code		P-SOP32-11.4x20.75-1.27	←
Package marking specification			
Assembly Material	Lead frame material	Cu	←
	Lead plating	Sn (pure tin)	←
	Die bonding	Epoxy paste	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-free)	←
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Magazine packing	Packing specification	Current specification	New specification
	Magazine	Magagine code : MP525PC	←
	Storage number	25pcs/magazine	←
	Number of magazines (Max.)	36 magazines	←
	Inner box size (LxWxH)	600mm x 172mm x 77mm	595mm x 170mm x 72mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Emboss type name : MTE3216H-32P2M-A	←
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	347mm x 368mm x 54mm	362mm x 340mm x 60mm
Moisture-proof performance		MSL 3	←
Shipping label		Current specification	No change in format (Changes in Renesas internal code)

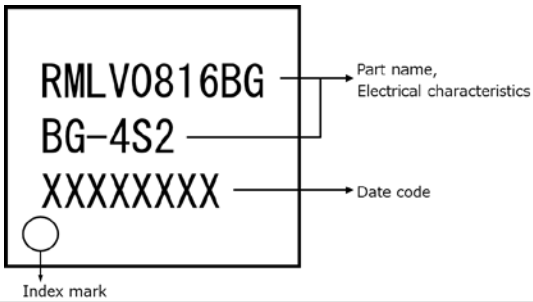
(6) 32pin-SOP 4Mb(3V) Part name : RMLV0408EGSP

Item		Pre Change	Post Change
Orderable part name		RMLV0408EGSP-4S2#CA0 (Magazine packing)	←
		RMLV0408EGSP-4S2#HA0 (Tape & Reel packing)	←
Assembly line		Renesas Semiconductor Beijing (China)	←
JEITA Package Code		P-SOP32-11.4x20.75-1.27	←
Package marking specification			No change
Assembly Material	Lead frame material	Cu	←
	Lead plating	Sn (pure tin)	←
	Die bonding	Epoxy paste	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-free)	←
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Magazine packing	Packing specification	Current specification	New specification
	Magazine	Magagine code : MP525PC	←
	Storage number	25pcs/magazine	←
	Number of magazines (Max.)	36 magazines	←
	Inner box size (LxWxH)	600mm x 172mm x 77mm	595mm x 170mm x 72mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Emboss type name : MTE3216H-32P2M-A	←
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	347mm x 368mm x 54mm	362mm x 340mm x 60mm
Moisture-proof performance		MSL 3	←
Shipping label		Current specification	No change in format (Changes in Renesas internal code)

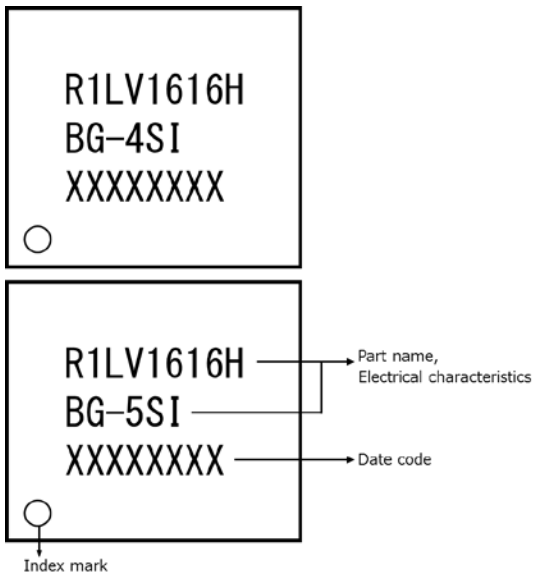
(7) 48ball-FBGA 4Mb(3V) Part name : RMLV0416EGBG

Item		Pre Change	Post Change
Orderable part name		RMLV0416EGBG-4S2#AC0 (Tray packing)	←
		RMLV0416EGBG-4S2#KC0 (Tape & Reel packing)	←
Assembly line		J-Devices Kumamoto District (Japan)	←
JEITA Package Code		P-TFBGA48-7.5x8.5-0.75	←
Package marking specification			No change
Assembly Material	Substrate material	Glass epoxy	←
	Solder ball	Sn-Ag-Cu	←
	Die bonding	Epoxy paste	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-free)	←
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (Tray type name : L196-45)	←
	Storage number	253pcs/tray	←
	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←
	Number of trays (Max.)	9 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	No change
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 3	←
Shipping label		Current specification	No change in format (Changes in Renesas internal code)

(8) 48ball-FBGA 8Mb(3V) Part name : RMLV0816BGBG

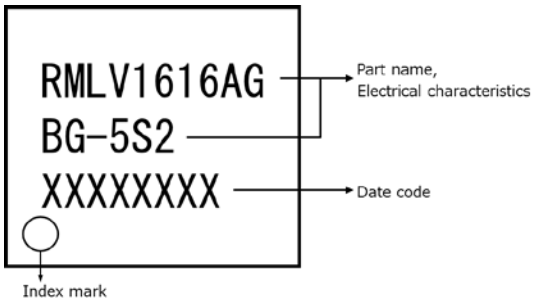
Item		Pre Change	Post Change
Orderable part name		RMLV0816BGBG-4S2#AC0 (Tray packing)	←
		RMLV0816BGBG-4S2#KC0 (Tape & Reel packing)	←
Assembly line		J-Devices Kumamoto District (Japan)	←
JEITA Package Code		P-TFBGA48-7.5x8.5-0.75	←
Package marking specification			No change
Assembly Material	Substrate material	Glass epoxy	←
	Solder ball	Sn-Ag-Cu	←
	Die bonding	Epoxy paste	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-free)	←
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (Tray type name : L196-45)	←
	Storage number	253pcs/tray	←
	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←
	Number of trays (Max.)	9 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	No change
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 3	←
Shipping label		Current specification	No change in format (Changes in Renesas internal code)

(9) 48ball-FBGA 16Mb(3V) Part name : R1LV1616HBG

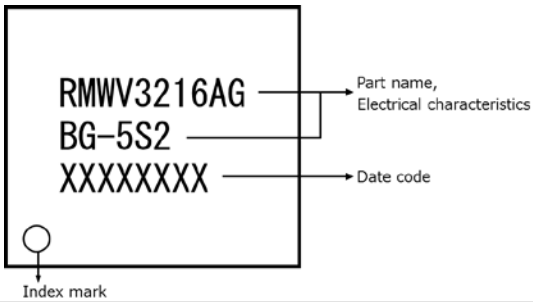
Item		Pre Change	Post Change
Orderable part name		R1LV1616HBG-4SI/-5SI#B0 (Tray packing)	←
		R1LV1616HBG-4SI/-5SI#S0 (Tape & Reel packing)	←
Assembly line		J-Devices Kumamoto District (Japan)	←
JEITA Package Code		P-TFBGA48-8x9.5-0.75	←
Package marking specification			No change
Assembly Material	Substrate material	Glass epoxy	←
	Solder ball	Sn-Ag-Cu	←
	Die bonding	Epoxy film	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-included)	←
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (Tray type name : PTA71C)	←
	Storage number	264pcs/tray	←
	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←
	Number of trays (Max.)	9 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	No change
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 3	←
Shipping label		Current specification	No change in format (Changes in Renesas internal code)

- Regarding R1LV1616HBG, laser marking on the package's surface is processed at final test site.

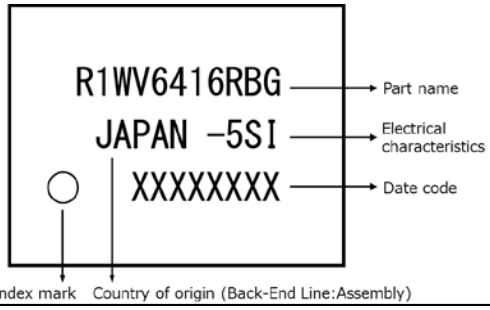
(10) 48ball-FBGA 16Mb(3V) Part name : RMLV1616AGBG

Item		Pre Change	Post Change
Orderable part name		RMLV1616AGBG-5S2#AC0 (Tray packing)	←
		RMLV1616AGBG-5S2#KC0 (Tape & Reel packing)	←
Assembly line		J-Devices Kumamoto District (Japan)	←
JEITA Package Code		P-TFBGA48-7.5x8.5-0.75	←
Package marking specification			No change
Assembly Material	Substrate material	Glass epoxy	←
	Solder ball	Sn-Ag-Cu	←
	Die bonding	Epoxy paste	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-free)	←
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (Tray type name : L196-45)	←
	Storage number	253pcs/tray	←
	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←
	Number of trays (Max.)	9 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	No change
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 3	←
Shipping label		Current specification	No change in format (Changes in Renesas internal code)

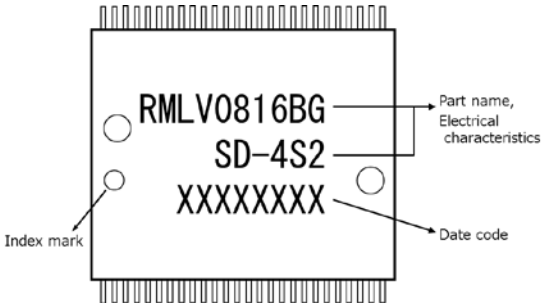
(11) 48ball-FBGA 32Mb(3V) Part name : RMWV3216AGBG

Item		Pre Change	Post Change
Orderable part name		RMWV3216AGBG-5S2#AC0 (Tray packing)	←
		RMWV3216AGBG-5S2#KC0 (Tape & Reel packing)	←
Assembly line		J-Devices Kumamoto District (Japan)	←
JEITA Package Code		P-TFBGA48-7.5x8.5-0.75	←
Package marking specification			No change
Assembly Material	Substrate material	Glass epoxy	←
	Solder ball	Sn-Ag-Cu	←
	Die bonding	Epoxy film	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-free)	←
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (Tray type name : L196-45)	←
	Storage number	253pcs/tray	←
	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←
	Number of trays (Max.)	9 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	No change
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 3	←
Shipping label		Current specification	No change in format (Changes in Renesas internal code)

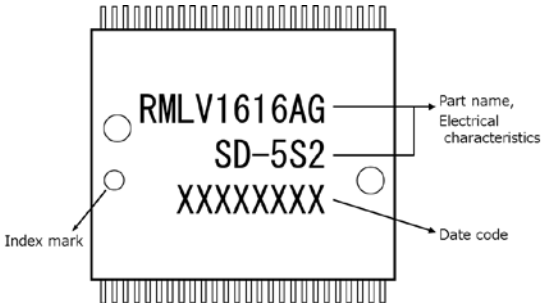
(12) 48ball-FBGA 64Mb(3V) Part name : R1WV6416RBG

Item		Pre Change	Post Change
Orderable part name		R1WV6416RBG-5SI#B0 (Tray packing)	←
		R1WV6416RBG-5SI#S0 (Tape & Reel packing)	←
Assembly line		J-Devices Kumamoto District (Japan)	←
JEITA Package Code		P-TFBGA48-8.5x11-0.75	←
Package marking specification			No change
Assembly Material	Substrate material	Glass epoxy	←
	Solder ball	Sn-Ag-Cu	←
	Die bonding	Epoxy film	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-included)	←
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (Tray type name : L196-121)	←
	Storage number	242pcs/tray	←
	Laying direction of Ics on a tray	Direction from the bottm right position to the up side (when the position of chamfer in tray's corner is bottom left.)	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	No change
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 3	←
Shipping label		Current specification	No change in format (Changes in Renesas internal code)

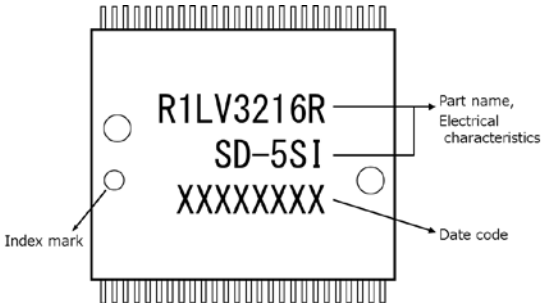
(13) 52pin-µTSOP 8Mb(3V) Part name : RMLV0816BGSD

Item		Pre Change	Post Change
Orderable part name		RMLV0816BGSD-4S2#AC0 (Tray packing)	←
		RMLV0816BGSD-4S2#HC0 (Tape & Reel packing)	←
Assembly line		Renesas Semiconductor Beijing (China)	←
JEITA Package Code		P-TSOP(2)52-8.89x10.79-0.40	←
Package marking specification			No change
Assembly Material	Lead frame material	42Alloy	←
	Lead plating	Sn-Cu	←
	Die bonding	Epoxy film	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-included)	←
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (Tray type name : L196-24)	←
	Storage number	230pcs/tray	←
	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	No change
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 2	←
Shipping label		Current specification	No change in format (Changes in Renesas internal code)

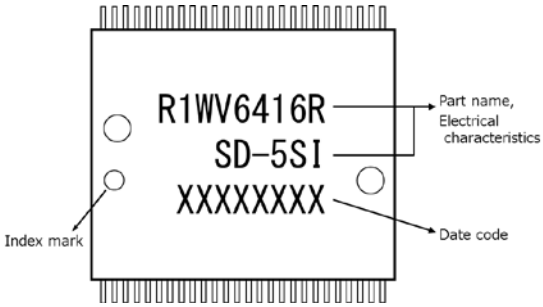
(14) 52pin-µTSOP 16Mb(3V) Part name : RMLV1616AGSD

Item		Pre Change	Post Change
Orderable part name		RMLV1616AGSD-5S2#AC0 (Tray packing)	←
		RMLV1616AGSD-5S2#HC0 (Tape & Reel packing)	←
Assembly line		Renesas Semiconductor Beijing (China)	←
JEITA Package Code		P-TSOP(2)52-8.89x10.79-0.40	←
Package marking specification			No change
Assembly Material	Lead frame material	42Alloy	←
	Lead plating	Sn-Cu	←
	Die bonding	Epoxy film	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-included)	←
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (Tray type name : L196-24)	←
	Storage number	230pcs/tray	←
	Laying direction of Ics on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	No change
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 2	←
Shipping label		Current specification	No change in format (Changes in Renesas internal code)

(15) 52pin-µTSOP 32Mb(3V) Part name : R1LV3216RSD

Item		Pre Change	Post Change
Orderable part name		R1LV3216RSD-5SI#B0 (Tray packing)	←
		R1LV3216RSD-5SI#S0 (Tape & Reel packing)	←
Assembly line		Renesas Semiconductor Beijing (China)	←
JEITA Package Code		P-TSOP(2)52-8.89x10.79-0.40	←
Package marking specification			No change
Assembly Material	Lead frame material	42Alloy	←
	Lead plating	Sn-Cu	←
	Die bonding	Epoxy film	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-included)	←
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (Tray type name : L196-24)	←
	Storage number	230pcs/tray	←
	Laying direction of Ics on a tray	Direction from the bottm right position to the up side (when the position of chamfer in tray's corner is bottom left.)	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	No change
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 2	←
Shipping label		Current specification	No change in format (Changes in Renesas internal code)

(16) 52pin-µTSOP 64Mb(3V) Part name : R1WV6416RSD

Item		Pre Change	Post Change
Orderable part name		R1WV6416RSD-5SI#B0 (Tray packing)	←
		R1WV6416RSD-5SI#S0 (Tape & Reel packing)	←
Assembly line		Renesas Semiconductor Beijing (China)	←
JEITA Package Code		P-TSOP(2)52-8.89x10.79-0.40	←
Package marking specification			No change
Assembly Material	Lead frame material	42Alloy	←
	Lead plating	Sn-Cu	←
	Die bonding	Epoxy film	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-included)	←
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (Tray type name : L196-24)	←
	Storage number	230pcs/tray	←
	Laying direction of Ics on a tray	Direction from the bottm right position to the up side (when the position of chamfer in tray's corner is bottom left.)	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification	No change
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	288mm x 273mm x 48mm	289mm x 264mm x 60mm
Moisture-proof performance		MSL 2	←
Shipping label		Current specification	No change in format (Changes in Renesas internal code)

3. Product integration by EOL of “-5SR, -7SI, -7SR” products (for 256Kb ~ 4Mb Low Power SRAM)

■ Regarding the EOL of “-5SR, -7SI, -7SR” products, these "Access and Temperature grades" are unified to "-5SI" (see below).

Package Type	Memory Cap., Supply Voltage	bit	Pre Change			Post Change		
			Orderable Part Name	Access time	Operation Temp.	Orderable Part Name	Access time	Operation Temp.
28pin-SOP	256Kb 5V	x8	R1LP5256ESP-5SI#B0 R1LP5256ESP-5SI#S0	55ns	-40℃ ～85℃	R1LP5256ESP-5SI#B0 R1LP5256ESP-5SI#S0	55ns	-40℃ ～85℃
			R1LP5256ESP-5SR#B0 R1LP5256ESP-5SR#S0		-0℃ ～70℃			
			R1LP5256ESP-7SI#B0 R1LP5256ESP-7SI#S0	70ns	-40℃ ～85℃			
			R1LP5256ESP-7SR#B0 R1LP5256ESP-7SR#S0		0℃ ～70℃			
	256Kb 3V	x8	R1LV5256ESP-5SI#B0 R1LV5256ESP-5SI#S0	55ns	-40℃ ～85℃	R1LV5256ESP-5SI#B0 R1LV5256ESP-5SI#S0	55ns	-40℃ ～85℃
			R1LV5256ESP-5SR#B0 R1LV5256ESP-5SR#S0		-0℃ ～70℃			
			R1LV5256ESP-7SI#B0 R1LV5256ESP-7SI#S0	70ns	-40℃ ～85℃			
			R1LV5256ESP-7SR#B0 R1LV5256ESP-7SR#S0		0℃ ～70℃			
32pin-SOP	1Mb 5V	x8	R1LP0108ESN-5SI#B0 R1LP0108ESN-5SI#S0	55ns	-40℃ ～85℃	R1LP0108ESN-5SI#B0 R1LP0108ESN-5SI#S0	55ns	-40℃ ～85℃
			R1LP0108ESN-5SR#B0 R1LP0108ESN-5SR#S0		-0℃ ～70℃			
			R1LP0108ESN-7SI#B0 R1LP0108ESN-7SI#S0	70ns	-40℃ ～85℃			
			R1LP0108ESN-7SR#B0 R1LP0108ESN-7SR#S0		0℃ ～70℃			
	1Mb 3V	x8	R1LV0108ESN-5SI#B0 R1LV0108ESN-5SI#S0	55ns	-40℃ ～85℃	R1LV0108ESN-5SI#B0 R1LV0108ESN-5SI#S0	55ns	-40℃ ～85℃
			R1LV0108ESN-5SR#B0 R1LV0108ESN-5SR#S0		-0℃ ～70℃			
			R1LV0108ESN-7SI#B0 R1LV0108ESN-7SI#S0	70ns	-40℃ ～85℃			
			R1LV0108ESN-7SR#B0 R1LV0108ESN-7SR#S0		0℃ ～70℃			
	4Mb 5V	x8	R1LP0408DSP-5SI#B0 R1LP0408DSP-5SI#S0	55ns	-40℃ ～85℃	R1LP0408DSP-5SI#B0 R1LP0408DSP-5SI#S0	55ns	-40℃ ～85℃
			R1LP0408DSP-5SR#B0 R1LP0408DSP-5SR#S0		-0℃ ～70℃			
			R1LP0408DSP-7SI#B0 R1LP0408DSP-7SI#S0	70ns	-40℃ ～85℃			
			R1LP0408DSP-7SR#B0 R1LP0408DSP-7SR#S0		0℃ ～70℃			

- #B0: Magazine packing, #S0: Tape & Reel packing

4. Electrical characteristics (DC/AC) (for 256Kb ~ 4Mb Low Power SRAM)

- Regarding the EOL of "-5SR, -7SI, -7SR" products, electrical characteristics (DC/AC) of unified "-5SI" product is completely upper-compatible with "- "-5SR, -7SI, -7SR" product (see below).

(1)–a. Electrical characteristics (DC) : 256Kb(5V) R1LP5256ESP

Products

Item	**Pre Change**	**Post Change**
Orderable part name	R1LP5256ESP-5SI, -5SR, -7SI, -7SR#B0	R1LP5256ESP-5SI#B0
	R1LP5256ESP-5SI, -5SR, -7SI, -7SR#S0	R1LP5256ESP-5SI#S0

DC conditions

Item	Symbol	**Pre Change**		Symbol	**Post Change**
Supply voltage	Vcc	4.5V～5.5V		Vcc	←
Operating temperature range	Ta	5SR, 7SR	0℃ to 70℃	Ta	-40℃ to 85℃
		5SI, 7SI	-40℃ to 85℃		
Input high voltage	VIH	2.2V(min.) / Vcc+0.3V(max.)		VIH	←
Input low voltage	VIL	-0.3V(min.) / 0.8V(max.)		VIL	←

DC characteristics

Item	Symbol	**Pre Change**		Symbol	**Post Change**	
Operating Current	Icc1(TTL, Min.Cycle)	35mA(max.) / 25mA(typ.)		Icc1(TTL, Min.Cycle)	←	
	Icc2(MOS, Cycle=1us)	4mA(max.) / 2mA(typ.)		Icc2(MOS, Cycle=1us)	←	
Standby current	ISB(TTL)	3mA(max.)		ISB(TTL)	←	
	ISB1(MOS)	～25℃	2uA(max.) / 0.6uA(typ.)	ISB1(MOS)	～25℃	←
		～40℃	3uA(max.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃ (for 5SI, 7SI)	10uA(max.)		～85℃	←
Output high voltage	VOH	IOH=-1mA	2.4V(min.)	VOH	IOH=-1mA	←
	VOH2	IOH=-0.1mA	Vcc-0.5V(min.)	VOH2	IOH=-0.1mA	←
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	IOL=2mA	←

Capacitance

Item	Symbol	**Pre Change**	Symbol	**Post Change**
Input capacitance	C in	6pF(max.)	C in	←
Input/Output capacitance	C I/O	8pF(max.)	C I/O	←

Data retention characteristics

Item	Symbol	**Pre Change**		Symbol	**Post Change**	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
Data retention current	IccDR(Vcc=3.0V)	～25℃	2uA(max.) / 0.6uA(typ.)	IccDR(Vcc=3.0V)	～25℃	←
		～40℃	3uA(max.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃ (for 5SI, 7SI)	10uA(max.)		～85℃	←
Chip deselect time to data retention	tCDR	0ns(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	

(1)–b. Electrical characteristics (AC) : 256Kb(5V) R1LP5256ESP

Products

Item	Pre Change	Post Change
Orderable part name	R1LP5256ESP-5SI, -5SR, -7SI, -7SR#B0	R1LP5256ESP-5SI#B0
	R1LP5256ESP-5SI, -5SR, -7SI, -7SR#S0	R1LP5256ESP-5SI#S0

AC characteristics

Read Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Read cycle time	tRC	5SI, 5SR	55ns(min.)	tRC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Address access time	tAA	5SI, 5SR	55ns(max.)	tAA	55ns(max.)
		7SI, 7SR	70ns(max.)		
Chip select access time	tACS	5SI, 5SR	55ns(max.)	tACS	55ns(max.)
		7SI, 7SR	70ns(max.)		
Output enable to output valid	tOE	5SI, 5SR	30ns(max.)	tOE	30ns(max.)
		7SI, 7SR	35ns(max.)		
Output hold from address change	tOH	5SI, 5SR	10ns(min.)	tOH	←
		7SI, 7SR	10ns(min.)		
Chip select to output in low-Z	tCLZ	5SI, 5SR	5ns(min.)	tCLZ	←
		7SI, 7SR	5ns(min.)		
Output enable to output in low-Z	tOLZ	5SI, 5SR	5ns(min.)	tOLZ	←
		7SI, 7SR	5ns(min.)		
Chip deselect to output in high-Z	tCHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tCHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		

Write Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Write cycle time	tWC	5SI, 5SR	55ns(min.)	tWC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Address valid to end of write	tAW	5SI, 5SR	50ns(min.)	tAW	50ns(min.)
		7SI, 7SR	65ns(min.)		
Chip select to end of write	tCW	5SI, 5SR	50ns(min.)	tCW	50ns(min.)
		7SI, 7SR	65ns(min.)		
Write pulse width	tWP	5SI, 5SR	40ns(min.)	tWP	40ns(min.)
		7SI, 7SR	50ns(min.)		
Address setup time	tAS	5SI, 5SR	0ns(min.)	tAS	←
		7SI, 7SR	0ns(min.)		
Write recovery time	tWR	5SI, 5SR	0ns(min.)	tWR	←
		7SI, 7SR	0ns(min.)		
Data to write time overlap	tDW	5SI, 5SR	25ns(min.)	tDW	25ns(min.)
		7SI, 7SR	30ns(min.)		
Data hold from write time	tDH	5SI, 5SR	0ns(min.)	tDH	←
		7SI, 7SR	0ns(min.)		
Output enable from end of write	tOW	5SI, 5SR	5ns(min.)	tOW	←
		7SI, 7SR	5ns(min.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Write to output in high-Z	tWHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tWHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		

(2)–a. Electrical characteristics (DC) : 256Kb(3V) R1LV5256ESP

Products

Item	Pre Change	Post Change
Orderable part name	R1LV5256ESP-5SI, -5SR, -7SI, -7SR#B0	R1LV5256ESP-5SI#B0
	R1LV5256ESP-5SI, -5SR, -7SI, -7SR#S0	R1LV5256ESP-5SI#S0

DC conditions

Item	Symbol	Pre Change		Symbol	Post Change
Supply voltage	Vcc	2.7V～3.6V		Vcc	←
Operating temperature range	Ta	5SR, 7SR	0°C to 70°C	Ta	-40°C to 85°C
		5SI, 7SI	-40°C to 85°C		
Input high voltage	VIH	2.0V(min.) / Vcc+0.3V(max.)		VIH	←
Input low voltage	VIL	-0.3V(min.) / 0.6V(max.)		VIL	←

DC characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Operating Current	Icc1(TTL, Min.Cycle)	25mA(max.) / 14mA(typ.)		Icc1(TTL, Min.Cycle)	←	
	Icc2(MOS, Cycle=1us)	5mA(max.) / 2mA(typ.)		Icc2(MOS, Cycle=1us)	←	
Standby current	ISB(TTL)	0.33mA(max.)		ISB(TTL)	←	
	ISB1(MOS)	～25℃	2uA(max.) / 0.6uA(typ.)	ISB1(MOS)	～25℃	←
		～40℃	3uA(max.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃ (for 5SI, 7SI)	10uA(max.)		～85℃	←
Output high voltage	VOH	IOH=-0.5mA	2.4V(min.)	VOH	IOH=-0.5mA	←
	VOH2	IOH=-0.05mA	Vcc-0.5V(min.)	VOH2	IOH=-0.05mA	←
Output low voltage	VOL	IOL=1mA	0.4V(max.)	VOL	IOL=1mA	←

Capacitance

Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	C in	6pF(max.)	C in	←
Input/Output capacitance	C I/O	8pF(max.)	C I/O	←

Data retention characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
Data retention current	IccDR(Vcc=3.0V)	～25℃	2uA(max.) / 0.6uA(typ.)	IccDR(Vcc=3.0V)	～25℃	←
		～40℃	3uA(max.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃ (for 5SI, 7SI)	10uA(max.)		～85℃	←
Chip deselect time to data retention	tCDR	0ns(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	

(2)–b. Electrical characteristics (AC) : 256Kb(3V) R1LV5256ESP

Products

Item	Pre Change	Post Change
Orderable part name	R1LV5256ESP-5SI, -5SR, -7SI, -7SR#B0	R1LV5256ESP-5SI#B0
	R1LV5256ESP-5SI, -5SR, -7SI, -7SR#S0	R1LV5256ESP-5SI#S0

AC characteristics
Read Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Read cycle time	tRC	5SI, 5SR	55ns(min.)	tRC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Address access time	tAA	5SI, 5SR	55ns(max.)	tAA	55ns(max.)
		7SI, 7SR	70ns(max.)		
Chip select access time	tACS	5SI, 5SR	55ns(max.)	tACS	55ns(max.)
		7SI, 7SR	70ns(max.)		
Output enable to output valid	tOE	5SI, 5SR	30ns(max.)	tOE	30ns(max.)
		7SI, 7SR	35ns(max.)		
Output hold from address change	tOH	5SI, 5SR	10ns(min.)	tOH	←
		7SI, 7SR	10ns(min.)		
Chip select to output in low-Z	tCLZ	5SI, 5SR	5ns(min.)	tCLZ	←
		7SI, 7SR	5ns(min.)		
Output enable to output in low-Z	tOLZ	5SI, 5SR	5ns(min.)	tOLZ	←
		7SI, 7SR	5ns(min.)		
Chip deselect to output in high-Z	tCHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tCHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		

Write Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Write cycle time	tWC	5SI, 5SR	55ns(min.)	tWC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Address valid to end of write	tAW	5SI, 5SR	50ns(min.)	tAW	50ns(min.)
		7SI, 7SR	65ns(min.)		
Chip select to end of write	tCW	5SI, 5SR	50ns(min.)	tCW	50ns(min.)
		7SI, 7SR	65ns(min.)		
Write pulse width	tWP	5SI, 5SR	40ns(min.)	tWP	40ns(min.)
		7SI, 7SR	50ns(min.)		
Address setup time	tAS	5SI, 5SR	0ns(min.)	tAS	←
		7SI, 7SR	0ns(min.)		
Write recovery time	tWR	5SI, 5SR	0ns(min.)	tWR	←
		7SI, 7SR	0ns(min.)		
Data to write time overlap	tDW	5SI, 5SR	25ns(min.)	tDW	25ns(min.)
		7SI, 7SR	30ns(min.)		
Data hold from write time	tDH	5SI, 5SR	0ns(min.)	tDH	←
		7SI, 7SR	0ns(min.)		
Output enable from end of write	tOW	5SI, 5SR	5ns(min.)	tOW	←
		7SI, 7SR	5ns(min.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Write to output in high-Z	tWHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tWHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		

(3)–a. Electrical characteristics (DC) : 1Mb(5V) R1LP0108ESN

Products

Item	Pre Change	Post Change
Orderable part name	R1LP0108ESN-5SI, -5SR, -7SI, -7SR#B0	R1LP0108ESN-5SI#B0
	R1LP0108ESN-5SI, -5SR, -7SI, -7SR#S0	R1LP0108ESN-5SI#S0

DC conditions

Item	Symbol	Pre Change		Symbol	Post Change
Supply voltage	Vcc	4.5V～5.5V		Vcc	←
Operating temperature range	Ta	5SR, 7SR	0°C to 70°C	Ta	-40°C to 85°C
		5SI, 7SI	-40°C to 85°C		
Input high voltage	VIH	2.2V(min.) / Vcc+0.3V(max.)		VIH	←
Input low voltage	VIL	-0.3V(min.) / 0.8V(max.)		VIL	←

DC characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Operating Current	Icc1(TTL, Min.Cycle)	35mA(max.) / 25mA(typ.)		Icc1(TTL, Min.Cycle)	←	
	Icc2(MOS, Cycle=1us)	5mA(max.) / 2mA(typ.)		Icc2(MOS, Cycle=1us)	←	
Standby current	ISB(TTL)	3mA(max.)		ISB(TTL)	←	
	ISB1(MOS)	～25℃	2uA(max.) / 0.6uA(typ.)	ISB1(MOS)	～25℃	←
		～40℃	3uA(max.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃ (for 5SI, 7SI)	10uA(max.)		～85℃	←
Output high voltage	VOH	IOH=-1mA	2.4V(min.)	VOH	IOH=-1mA	←
	VOH2	IOH=-0.1mA	Vcc-0.5V(min.)	VOH2	IOH=-0.1mA	←
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	IOL=2mA	←

Capacitance

Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	C in	8pF(max.)	C in	←
Input/Output capacitance	C I/O	10pF(max.)	C I/O	←

Data retention characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
Data retention current	IccDR(Vcc=3.0V)	～25℃	2uA(max.) / 0.6uA(typ.)	IccDR(Vcc=3.0V)	～25℃	←
		～40℃	3uA(max.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃ (for 5SI, 7SI)	10uA(max.)		～85℃	←
Chip deselect time to data retention	tCDR	0ns(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	

(3)–b. Electrical characteristics (AC) : 1Mb(5V) R1LP0108ESN

Products

Item	Pre Change	Post Change
Orderable part name	R1LP0108ESN-5SI, -5SR, -7SI, -7SR#B0	R1LP0108ESN-5SI#B0
	R1LP0108ESN-5SI, -5SR, -7SI, -7SR#S0	R1LP0108ESN-5SI#S0

AC characteristics

Read Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Read cycle time	tRC	5SI, 5SR	55ns(min.)	tRC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Address access time	tAA	5SI, 5SR	55ns(max.)	tAA	55ns(max.)
		7SI, 7SR	70ns(max.)		
Chip select access time	tACS1 / tACS2	5SI, 5SR	55ns(max.)	tACS1 / tACS2	55ns(max.)
		7SI, 7SR	70ns(max.)		
Output enable to output valid	tOE	5SI, 5SR	30ns(max.)	tOE	30ns(max.)
		7SI, 7SR	35ns(max.)		
Output hold from address change	tOH	5SI, 5SR	5ns(min.)	tOH	5ns(min.)
		7SI, 7SR	10ns(min.)		
Chip select to output in low-Z	tCLZ1 / tCLZ2	5SI, 5SR	5ns(min.)	tCLZ1 / tCLZ2	5ns(min.)
		7SI, 7SR	10ns(min.)		
Output enable to output in low-Z	tOLZ	5SI, 5SR	5ns(min.)	tOLZ	←
		7SI, 7SR	5ns(min.)		
Chip deselect to output in high-Z	tCHZ1 / tCHZ2	5SI, 5SR	0ns(min.) / 20ns(max.)	tCHZ1 / tCHZ2	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		

Write Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Write cycle time	tWC	5SI, 5SR	55ns(min.)	tWC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Address valid to end of write	tAW	5SI, 5SR	50ns(min.)	tAW	50ns(min.)
		7SI, 7SR	55ns(min.)		
Chip select to end of write	tCW	5SI, 5SR	50ns(min.)	tCW	50ns(min.)
		7SI, 7SR	55ns(min.)		
Write pulse width	tWP	5SI, 5SR	45ns(min.)	tWP	45ns(min.)
		7SI, 7SR	50ns(min.)		
Address setup time	tAS	5SI, 5SR	0ns(min.)	tAS	←
		7SI, 7SR	0ns(min.)		
Write recovery time	tWR	5SI, 5SR	0ns(min.)	tWR	←
		7SI, 7SR	0ns(min.)		
Data to write time overlap	tDW	5SI, 5SR	25ns(min.)	tDW	25ns(min.)
		7SI, 7SR	30ns(min.)		
Data hold from write time	tDH	5SI, 5SR	0ns(min.)	tDH	←
		7SI, 7SR	0ns(min.)		
Output enable from end of write	tOW	5SI, 5SR	5ns(min.)	tOW	←
		7SI, 7SR	5ns(min.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Write to output in high-Z	tWHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tWHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		

(4)–a. Electrical characteristics (DC) : 1Mb(3V) R1LV0108ESN

Products

Item	Pre Change	Post Change
Orderable part name	R1LV0108ESN-5SI, -5SR, -7SI, -7SR#B0	R1LV0108ESN-5SI#B0
	R1LV0108ESN-5SI, -5SR, -7SI, -7SR#S0	R1LV0108ESN-5SI#S0

DC conditions

Item	Symbol	Pre Change		Symbol	Post Change
Supply voltage	Vcc	2.7V～3.6V		Vcc	←
Operating temperature range	Ta	5SR, 7SR	0°C to 70°C	Ta	-40°C to 85°C
		5SI, 7SI	-40°C to 85°C		
Input high voltage	VIH	2.0V(min.) / Vcc+0.3V(max.)		VIH	←
Input low voltage	VIL	-0.3V(min.) / 0.6V(max.)		VIL	←

DC characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Operating Current	Icc1(TTL, Min.Cycle)	25mA(max.) / 15mA(typ.)		Icc1(TTL, Min.Cycle)	←	
	Icc2(MOS, Cycle=1us)	5mA(max.) / 2mA(typ.)		Icc2(MOS, Cycle=1us)	←	
Standby current	ISB(TTL)	0.33mA(max.)		ISB(TTL)	←	
	ISB1(MOS)	～25℃	2uA(max.) / 0.6uA(typ.)	ISB1(MOS)	～25℃	←
		～40℃	3uA(max.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃ (for 5SI, 7SI)	10uA(max.)		～85℃	←
Output high voltage	VOH	IOH=-0.5mA	2.4V(min.)	VOH	IOH=-0.5mA	←
	VOH2	IOH=-0.05mA	Vcc-0.5V(min.)	VOH2	IOH=-0.05mA	←
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	IOL=2mA	←

Capacitance

Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	C in	8pF(max.)	C in	←
Input/Output capacitance	C I/O	10pF(max.)	C I/O	←

Data retention characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
Data retention current	IccDR(Vcc=3.0V)	～25℃	2uA(max.) / 0.6uA(typ.)	IccDR(Vcc=3.0V)	～25℃	←
		～40℃	3uA(max.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃ (for 5SI, 7SI)	10uA(max.)		～85℃	←
Chip deselect time to data retention	tCDR	0ns(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	

(4)–b. Electrical characteristics (AC) : 1Mb(3V) R1LV0108ESN

Products

Item	Pre Change	Post Change
Orderable part name	R1LV0108ESN-5SI, -5SR, -7SI, -7SR#B0	R1LV0108ESN-5SI#B0
	R1LV0108ESN-5SI, -5SR, -7SI, -7SR#S0	R1LV0108ESN-5SI#S0

AC characteristics

Read Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Read cycle time	tRC	5SI, 5SR	55ns(min.)	tRC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Address access time	tAA	5SI, 5SR	55ns(max.)	tAA	55ns(max.)
		7SI, 7SR	70ns(max.)		
Chip select access time	tACS1 / tACS2	5SI, 5SR	55ns(max.)	tACS1 / tACS2	55ns(max.)
		7SI, 7SR	70ns(max.)		
Output enable to output valid	tOE	5SI, 5SR	30ns(max.)	tOE	30ns(max.)
		7SI, 7SR	35ns(max.)		
Output hold from address change	tOH	5SI, 5SR	5ns(min.)	tOH	5ns(min.)
		7SI, 7SR	10ns(min.)		
Chip select to output in low-Z	tCLZ1 / tCLZ2	5SI, 5SR	5ns(min.)	tCLZ1 / tCLZ2	5ns(min.)
		7SI, 7SR	10ns(min.)		
Output enable to output in low-Z	tOLZ	5SI, 5SR	5ns(min.)	tOLZ	←
		7SI, 7SR	5ns(min.)		
Chip deselect to output in high-Z	tCHZ1 / tCHZ2	5SI, 5SR	0ns(min.) / 20ns(max.)	tCHZ1 / tCHZ2	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		

Write Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Write cycle time	tWC	5SI, 5SR	55ns(min.)	tWC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Address valid to end of write	tAW	5SI, 5SR	50ns(min.)	tAW	50ns(min.)
		7SI, 7SR	55ns(min.)		
Chip select to end of write	tCW	5SI, 5SR	50ns(min.)	tCW	50ns(min.)
		7SI, 7SR	55ns(min.)		
Write pulse width	tWP	5SI, 5SR	45ns(min.)	tWP	45ns(min.)
		7SI, 7SR	50ns(min.)		
Address setup time	tAS	5SI, 5SR	0ns(min.)	tAS	←
		7SI, 7SR	0ns(min.)		
Write recovery time	tWR	5SI, 5SR	0ns(min.)	tWR	←
		7SI, 7SR	0ns(min.)		
Data to write time overlap	tDW	5SI, 5SR	25ns(min.)	tDW	25ns(min.)
		7SI, 7SR	30ns(min.)		
Data hold from write time	tDH	5SI, 5SR	0ns(min.)	tDH	←
		7SI, 7SR	0ns(min.)		
Output enable from end of write	tOW	5SI, 5SR	5ns(min.)	tOW	←
		7SI, 7SR	5ns(min.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Write to output in high-Z	tWHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tWHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		

(5)–a. Electrical characteristics (DC) : 4Mb(5V) x8 R1LP0408DSP

Products

Item	Pre Change	Post Change
Orderable part name	R1LP0408DSP-5SI, -5SR, -7SI, -7SR#B0	R1LP0408DSP-5SI#B0
	R1LP0408DSP-5SI, -5SR, -7SI, -7SR#S0	R1LP0408DSP-5SI#S0

DC conditions

Item	Symbol	Pre Change		Symbol	Post Change
Supply voltage	Vcc	4.5V～5.5V		Vcc	←
Operating temperature range	Ta	5SR, 7SR	0°C to 70°C	Ta	-40°C to 85°C
		5SI, 7SI	-40°C to 85°C		
Input high voltage	VIH	2.2V(min.) / Vcc+0.3V(max.)		VIH	←
Input low voltage	VIL	-0.3V(min.) / 0.8V(max.)		VIL	←

DC characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Operating Current	Icc(TTL)	10mA(max.) / 5mA(typ.)		Icc(TTL)	←	
	Icc1(TTL, Min.Cycle)	25mA(max.) / 15mA(typ.)		Icc1(TTL, Min.Cycle)	←	
	Icc2(MOS, Cycle=1us)	5mA(max.) / 3mA(typ.)		Icc2(MOS, Cycle=1us)	←	
Standby current	ISB(TTL)	0.5mA(max.) / 0.1mA(typ.)		ISB(TTL)	←	
	ISB1(MOS)	～25℃	2.5uA(max.) / 0.8uA(typ.)	ISB1(MOS)	～25℃	←
		～40℃	3uA(max.) / 1uA(typ.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃ (for 5SI, 7SI)	10uA(max.)		～85℃	←
Output high voltage	VOH	IOH=-1mA	2.4V(min.)	VOH	IOH=-1mA	←
	VOH2	IOH=-0.1mA	Vcc-0.5V(min.)	VOH2	IOH=-0.1mA	←
Output low voltage	VOL	IOL=2.1mA	0.4V(max.)	VOL	IOL=2.1mA	←

Capacitance

Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	C in	8pF(max.)	C in	←
Input/Output capacitance	C I/O	10pF(max.)	C I/O	←

Data retention characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
Data retention current	IccDR(Vcc=3.0V)	～25℃	2.5uA(max.) / 0.8uA(typ.)	IccDR(Vcc=3.0V)	～25℃	←
		～40℃	3uA(max.) / 1uA(typ.)		～40℃	←
		～70℃	8uA(max.)		～70℃	←
		～85℃ (for 5SI, 7SI)	10uA(max.)		～85℃	←
Chip deselect time to data retention	tCDR	0ns(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	

(5)–b. Electrical characteristics (AC) : 4Mb(5V) x8 R1LP0408DSP

Products

Item	Pre Change	Post Change
Orderable part name	R1LP0408DSP-5SI, -5SR, -7SI, -7SR#B0	R1LP0408DSP-5SI#B0
	R1LP0408DSP-5SI, -5SR, -7SI, -7SR#S0	R1LP0408DSP-5SI#S0

AC characteristics
Read Cycle

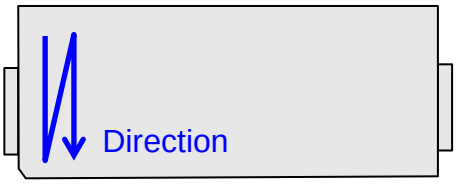
Item	Symbol	Pre Change		Symbol	Post Change
Read cycle time	tRC	5SI, 5SR	55ns(min.)	tRC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Address access time	tAA	5SI, 5SR	55ns(max.)	tAA	55ns(max.)
		7SI, 7SR	70ns(max.)		
Chip select access time	tACS	5SI, 5SR	55ns(max.)	tACS	55ns(max.)
		7SI, 7SR	70ns(max.)		
Output enable to output valid	tOE	5SI, 5SR	25ns(max.)	tOE	25ns(max.)
		7SI, 7SR	35ns(max.)		
Chip select to output in low-Z	tCLZ	5SI, 5SR	10ns(min.)	tCLZ	←
		7SI, 7SR	10ns(min.)		
Output enable to output in low-Z	tOLZ	5SI, 5SR	5ns(min.)	tOLZ	←
		7SI, 7SR	5ns(min.)		
Chip deselect to output in high-Z	tCHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tCHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Output hold from address change	tOH	5SI, 5SR	10ns(min.)	tOH	←
		7SI, 7SR	10ns(min.)		

Write Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Write cycle time	tWC	5SI, 5SR	55ns(min.)	tWC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Chip select to end of write	tCW	5SI, 5SR	50ns(min.)	tCW	50ns(min.)
		7SI, 7SR	60ns(min.)		
Address setup time	tAS	5SI, 5SR	0ns(min.)	tAS	←
		7SI, 7SR	0ns(min.)		
Address valid to end of write	tAW	5SI, 5SR	50ns(min.)	tAW	50ns(min.)
		7SI, 7SR	60ns(min.)		
Write pulse width	tWP	5SI, 5SR	40ns(min.)	tWP	40ns(min.)
		7SI, 7SR	50ns(min.)		
Write recovery time	tWR	5SI, 5SR	0ns(min.)	tWR	←
		7SI, 7SR	0ns(min.)		
Write to output in high-Z	tWHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tWHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Data to write time overlap	tDW	5SI, 5SR	25ns(min.)	tDW	25ns(min.)
		7SI, 7SR	30ns(min.)		
Data hold from write time	tDH	5SI, 5SR	0ns(min.)	tDH	←
		7SI, 7SR	0ns(min.)		
Output enable from end of write	tOW	5SI, 5SR	5ns(min.)	tOW	←
		7SI, 7SR	5ns(min.)		
Output disable to output in high-Z	tOHZ	5SI, 5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		

5. Packing specification (Laying direction of ICs on a tray)

- Regarding R1LV3216RSD-5SI, R1WV6416RSD-5SI and R1WV6416RBG-5SI, laying direction of ICs on a tray is to be changed (see below).
- No change in other products, because the direction is already same as the "Post Change“ as shown below.

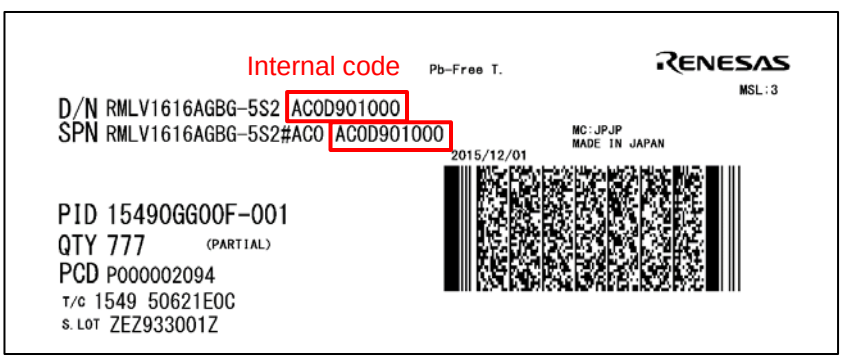
	Pre Change	Post Change
Laying direction of ICs on a tray		
Orderable part name	R1LV3216RSD-5SI#B0 R1WV6416RSD-5SI#B0 R1WV6416RBG-5SI#B0	R1LV3216RSD-5SI#B0 R1WV6416RSD-5SI#B0 R1WV6416RBG-5SI#B0

6. Shipping label

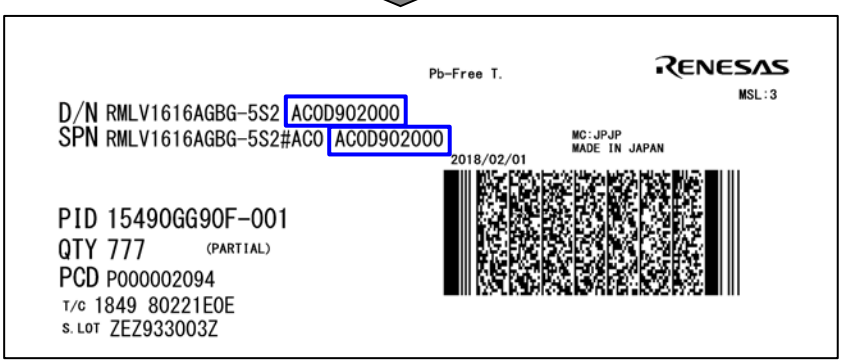
- Label format itself is not changed.
- Written specifications: “Internal code“ is changed. See below for example.

(1) Example of
Internal code = 10-digit

Pre Change

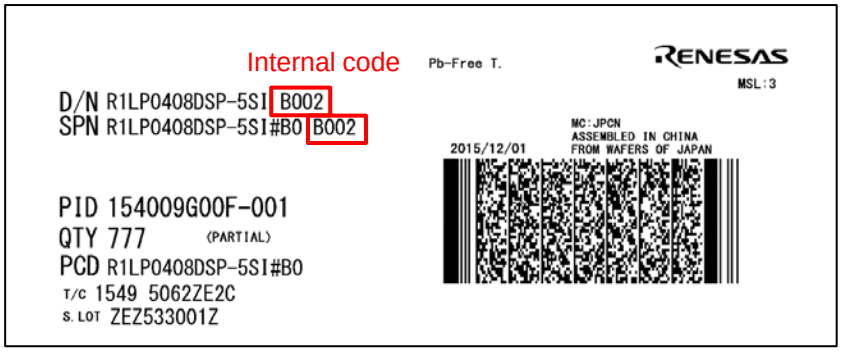


Post Change



(2) Example of
Internal code = 4-digit

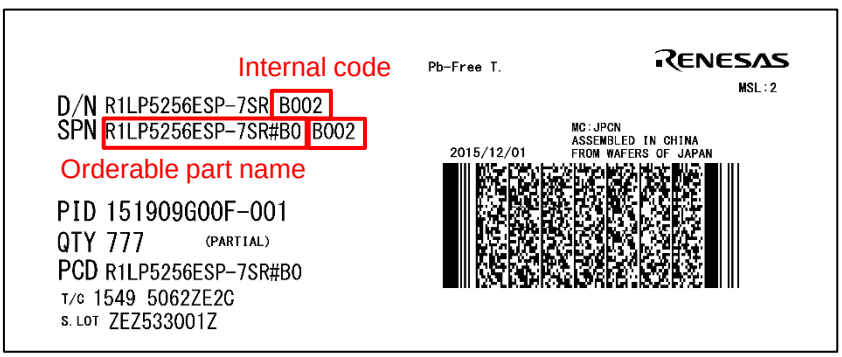
Pre Change



Post Change

(3) Example of
EOL product
(-5SR, -7SI, -7SR)

Pre Change



Note: Orderable part name
is changed to “-5SI”.

Post Change

7. Site information

<Final Test Site>

■Company Name : Powertech Technology Inc.

■Country Name : Taiwan

■Company Address : No.10, Datong Rd., Hsinchu Industrial Park, Hukou, Hsinchu 30352, Taiwan