Product Advisory (PA)

Subject: Die Thickness Change and Add Additional Manufacturing Locations for DDR5 RCD
Publication Date: 4/30/2021
Effective Date: Follow Implementation Date per below Table.
Revision Description:
Initial Release

Description of Change:
Renesas is changing the die thickness from 8mil to 10mil for better warpage performance. Internal qualification on the first lot has been successfully completed. Refer attach Qualification report. A follow up PA notice will be issued as when the qualification is fully completed successfully.

Refer attachment for more details on die thickness changes.

In addition, we are adding few manufacturing locations for this product as shown below to allow manufacturing flexibility and achieve minimal dual source. No change to foundry location.

There will be no change in the moisture sensitive level.

Assembly Location	Test Location	Die Thickness	Remark	Estimated Qual Completion Date	Implementation Date
ASEC, Taiwan	REPG, Malaysia	8 mil	Existing	Passed	Implemented
ASEC, Taiwan	REPG, Malaysia	10 mil	New	May 16, 2021	Jun 16, 2021
ASEC, Taiwan	ASEK, Taiwan	10 mil	New	May 16, 2021	June 16, 2021
SCK, Korea	REPG, Malaysia	10 mil	New	June 22, 2021	July 22, 2021
SCK, Korea	ASEK, Taiwan	10 mil	New	June 22, 2021	July 22, 2021
ATK, Korea	REPG, Malaysia	10 mil	New	Sep 2, 2021	Oct 2, 2021
ATK, Korea	ASEK, Taiwan	10 mil	New	Sep 2, 2021	Oct 2, 2021

Material Sets	Existing Assembly ASEC, Taiwan	Existing Assembly SCK, Korea	Alternate Assembly Amkor, Korea
Die Bump	Copper Pillar 37Cu/3Ni/27SnAg	Copper Pillar 37Cu/3Ni/27SnAg	Copper Pillar 37Cu/3Ni/27SnAg
Mold Compound	EME-G311A Type C	KE-G1250FC-K	EME-G355
Substrate/Supplier	GHPL830NS+SR1 (UMTC)	GHPL830NS+SR1 (SIMMTECH)	GHPL830NS+SR1 (UMTC)
Solder Balls	0.3mm LF35	0.3mm LF35	0.3mm LF35

Affected Product List: 5RCD0148HC3AVG, 5RCD0148HC3AVGI, 5RCD0148HC3AVG8, 5RCD0148HC3AVGI8

Reason for Change:
To provide manufacturing flexibility and warpage improvement.

Impact on Fit, Form, Function, Quality & Reliability:
The change will have no impact on the fit, function, quality and reliability.

Product Identification:
The cutoff datecode for ASEC with 10mil die thickness material is 2120 onwards.
Traceable through assembly lot# prefix for assembly location where:

RC denote ASEC
B denote SCK
D denote Amkor Korea

Test location traceable from assembly lot#

Qualification Status: Completed for 1st lot. Refer Appendix A
Sample Availability Date: 5/3/2021
Device Material Declaration: Available upon request

Questions or requests pertaining to this change notice, including additional data or samples, must be sent to Renesas within 30 days of the publication date.

For additional information regarding this notice, please contact idt-pcn@lm.renesas.com

Package Qualification Report

Date: 4/12/2021

Product : 5RCD0148			
Fab Base:	AD903T	Process Technology:	CLN28HPC, 1P8M
Package Types:	FCCSP 240	Fab Location:	TSMC
Qual Plan:	P21-01-013	Assembly Location:	ASEC - Taiwan

Test Description	**Conditions**	**Sample Size**	**Results (rej/SS)**	**Comments**
Temperature Cycling [1]	JESD22-A104, -55°C to +125°C, 1000 cycles	77 x 3 lots	0/77, 3 lots	Pass
Highly Accelerated Temperature and Humidity stress (Biased) [1]	JESD22-A110, +130°C, 85% R.H., Vcc_{max},96 hrs	77 x 3 lots	0/77, 1 lot	Pass 2nd & 3rd lots ECD: May 2021
Unbiased Highly Accelerated Temperature and Humidity stress (Unbiased) [1]	JESD22-A118, +130°C, 85% R.H., 96 hrs	77 x 3 lots	0/77, 3 lots	Pass
High Temperature Storage Life	JESD22-A103, +150°C, 1000 hrs	77 x 3 lots	0/77, 3 lots	Pass
Physical Dimension	JESD22-B100 (Per applicable Renesas Package Outline Drawing)	30 x 3 lots	0/30, 3 lots	Pass
Solder Ball Shear	JESD22-B117	5 x 3 lots	0/5, 3 lots	Pass
Moisture Classification	J-STD-020	77 x 3 lots	0/77, 3 lots	Pass

Note:

1. With preconditioning per JESD22-A113, MSL3 (260°C)

DDR5 RCD PACKAGE OPTIMIZATION UPDATE

2/28/2021
PACKAGE DEVELOPMENT

BIG IDEAS
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BACKGROUND

- Package warpage is a key index impacting DIMM level SMT quality
- Package warpage is also important parameter for component level and board level reliability
- Renesas defined package warpage spec with 20% safety margin
- Renesas completed package stack-up optimizations to minimize the warpage
- This report aims to provide package optimization summary to the customer to assess DIMM and System level reliability implications.

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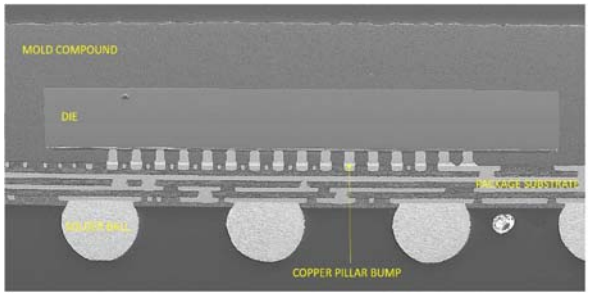
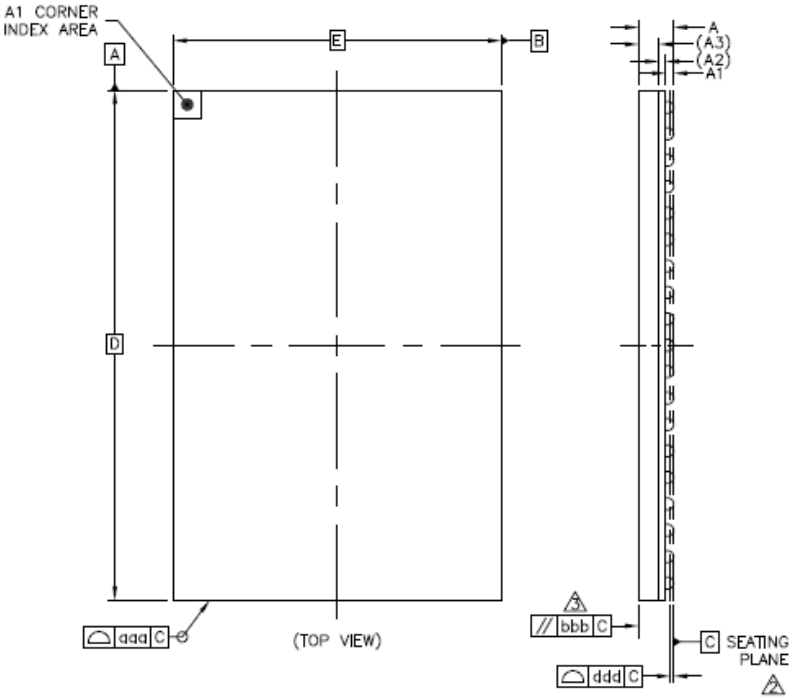
POD & DIE VOLUME

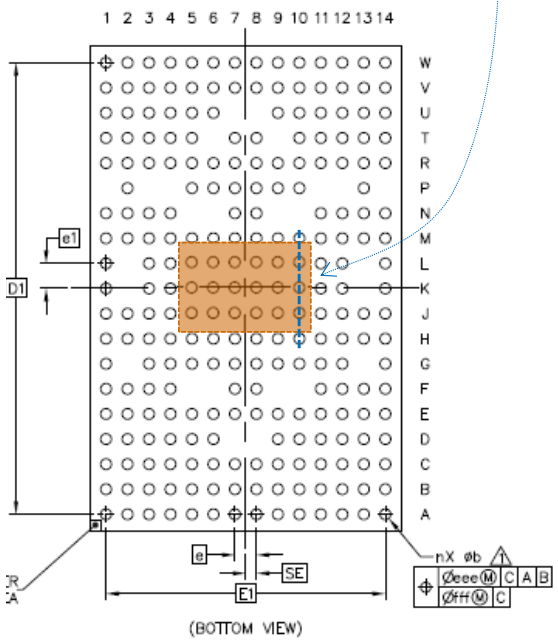


X-sectional view

Package Volume:
8.7 x 13.5 x 0.717 = 84.212 mm^3

Die Volume:
3.36 x 2.16 x 0.20 = 1.452 mm^3 (8 mil), 1.7%
3.36 x 2.16 x 0.25 = 1.814 mm^3 (10 mil), 2.2%
Δ = 1.814 – 1.452 = 0.362 mm^3, 0.4% volume change





	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1
STAND OFF	A1	0.16	---	0.26
SUBSTRATE THICKNESS	A2		0.187	REF
MOLD THICKNESS	A3		0.53	REF
BODY SIZE	D		13.5	BSC
	E		8.7	BSC
BALL DIAMETER			0.3	
BALL OPENING			0.275	
BALL WIDTH	b	0.25	---	0.35
BALL PITCH	e		0.6	BSC
BALL PITCH	e1		0.7	BSC
BALL COUNT	n		240	
EDGE BALL CENTER TO CENTER	D1		12.6	BSC
	E1		7.8	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		0.3	BSC
PACKAGE EDGE TOLERANCE	aaa		0.15	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.05	

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PACKAGE WARPAGE CONTROL, KEEP 20% MARGIN

- JEITA Spec, 100 um max
  - ϕ0.3 mm solder ball
  - 0.6 x 0.7 mm ball pitch

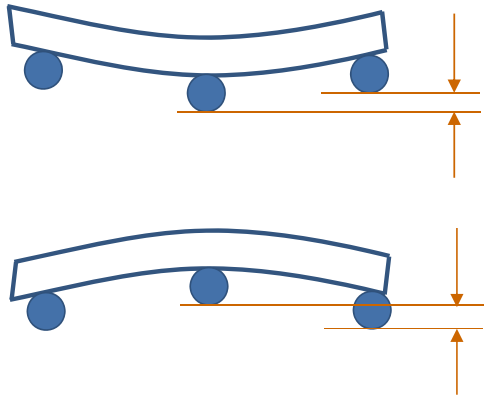
- Renesas Engineering Control, 80 um max
  - Shadow Moiré (room → reflow → room)
  - Highest number from 3 dry & 3 wet units

- Production Control, 80 um max
  - Ball coplanarity check at room (ICOS)
  - Sample size (100%)

- Quarterly Production Monitoring, 80 um max (TBD)
  - Shadow Moiré (room → reflow → room)
  - Highest number from 3 dry & 3 wet units

Table 1 — Flatness requirements (mm) during reflow for components less than or equal to 15mm on any side, applies to temperature range from flux activation to reflow peak. Follows JEITA ED-7306.

		b - Ball Diameter(mm)[III]												
		0.20	0.25	0.30	0.35	0.40	0.45	0.50	0.55	0.60	0.65	0.80	0.90	1.00
Ball Pitch (mm)	0.40	±0.10	±0.10	±0.10										
	0.50		±0.10	±0.10	±0.10									
	0.65		±0.10	±0.10	±0.10	±0.11	±0.12							
	0.80		±0.10	±0.10	±0.10	±0.11	±0.12	±0.13	±0.14					
	1.00					±0.11	±0.12	±0.13	±0.14	±0.17	±0.17			
	1.27									±0.17	±0.17	±0.21	±0.23	±0.25



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PACKAGE WARPAGE REDUCTION

- Checked 3 parameters to reduce package warpage level with extensive DOEs.
- Tested 3 EMC types at early stage of the development
  - Picked best material having the lowest strip level warpage
- Tested two substrate PP thickness options
  - 25 um vs. 35 um
  - 35 um PP showed meaningful warpage reduction
  - However, we picked 25 um PP for higher electrical performance with minimal package parasitic
- Tested two die thickness options
  - 8 mil vs. 10 mil
  - 10 mil die shows significant improvement (Dry 80.3 → 65.4 um), (Wet 92.9 → 60.2 um)

Die thickness increase is a safe parameter to improve warpage without impacting performance.
Achieved about 15 um and 33 um improvement from dry and wet samples, respectively.

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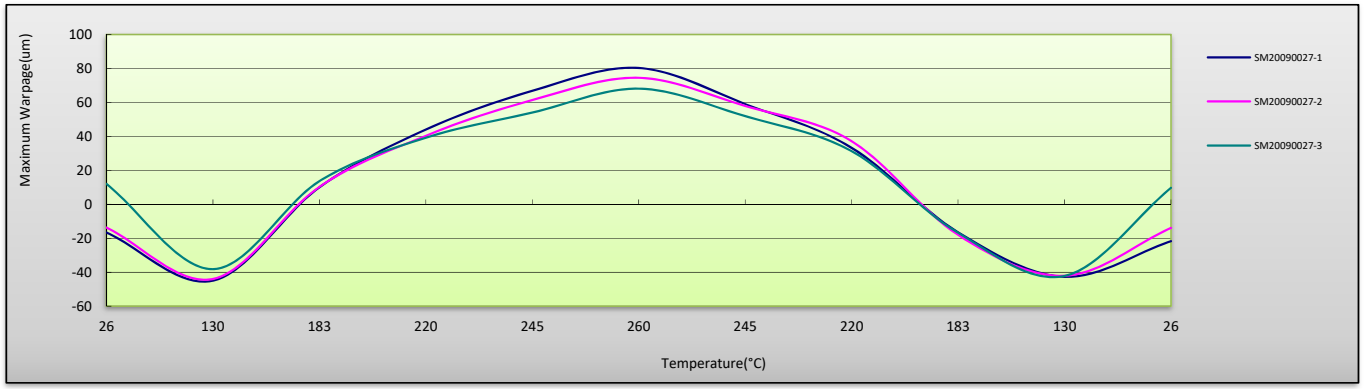
8 MIL DIE, DRY WARPAGE DATA (1/4)

Temp. (‘C)	Bake-1	Bake-2	Bake-3	Avg.
26	-16.6	-13.7	12	-6.1
130	-45	-44	-38.2	-42.4
183	10	10.3	13.6	11.3
220	44	40.4	39.2	41.2
245	66.8	61.4	54	60.7
260	80.3	74.5	68.1	74.3
245	59.1	57.9	51.9	56.3
220	33.3	37.2	31.3	33.9
183	-16.5	-18	-16.8	-17.1
130	-42.7	-42.1	-42.2	-42.3
26	-21.7	-13.9	9.7	-8.6

- Shadow Moiré
- Sample size, 3 dry units
- Bake at 125°C for 24hrs
- Max warpage, 80.3 um at reflow > 80 um spec



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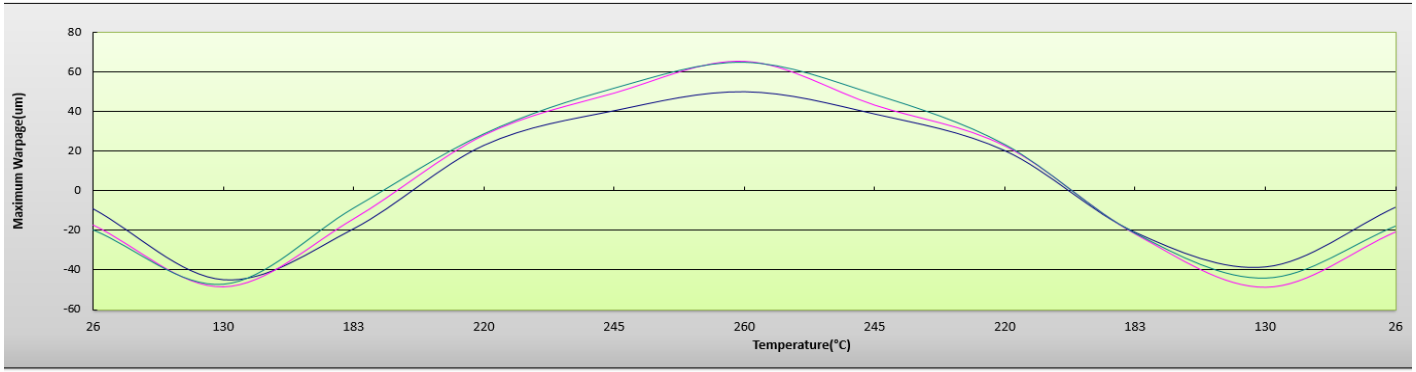
8 MIL DIE, WET WARPAGE DATA (2/4)

Temp. (‘C)	MSL3+Bake-1	MSL3+Bake-2	MSL3+Bake-3	Avg.
25	-13.3	-18.4	-16.6	-16.1
130	-43.8	-48.6	-44.8	-45.7
183	-16.2	-15	-8.7	-13.3
220	20.4	28.2	29	25.9
245	41.6	55	59.2	51.9
260	47.5	63.6	68.3	59.8
245	38.7	56.3	56.8	50.6
220	15.6	27.6	24	22.4
183	-24.6	-22.4	-16.9	-21.3
130	-48	-48.4	-51.9	-49.4
25	-11.7	-17.9	-22.2	-17.3

- Shadow Moiré
- Sample size, 3 wet units
- Bake at 125°C for 24hrs + MSL3 soak
- Max warpage, 68.3 um at reflow < 80 um spec
- 92.9 um from prior qual data > 80 um spec



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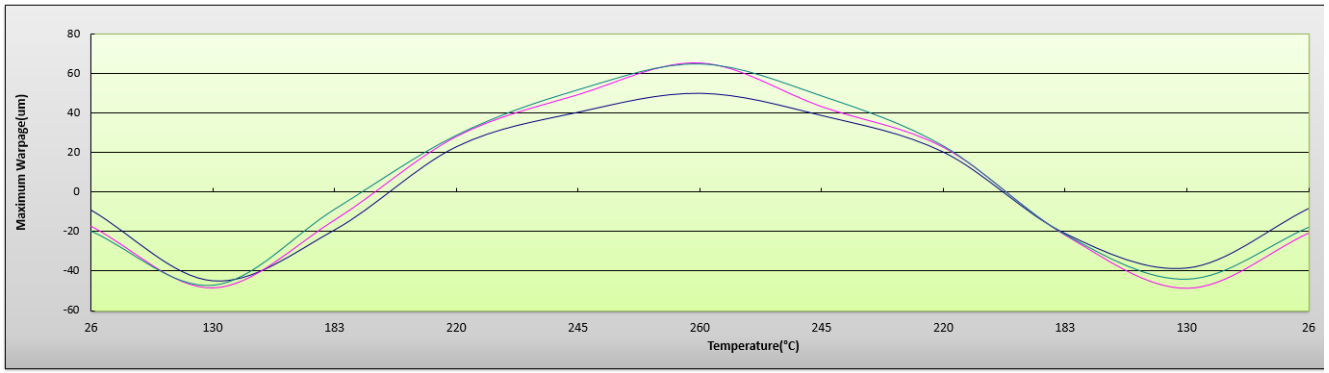
10 MIL DIE, DRY WARPAGE DATA (3/4)

Temp. (‘C)	Bake-1	Bake-2	Bake-3
26	-9.1	-17.1	-19.6
130	-45	-48.3	-47
183	-19.2	-14	-8.6
220	23	28.2	28.8
245	40.5	49.4	51.8
260	50.1	65.4	64.8
245	38.8	43.3	48.6
220	20.2	22.7	23.3
183	-21.1	-21.7	-21.4
130	-38.5	-48.5	-43.9
26	-8.2	-20.5	-17.6

- Shadow Moiré
- Sample size, 3 dry units
- Bake at 125°C for 24hrs
- Max warpage, 65.4 um at reflow < 80 um spec



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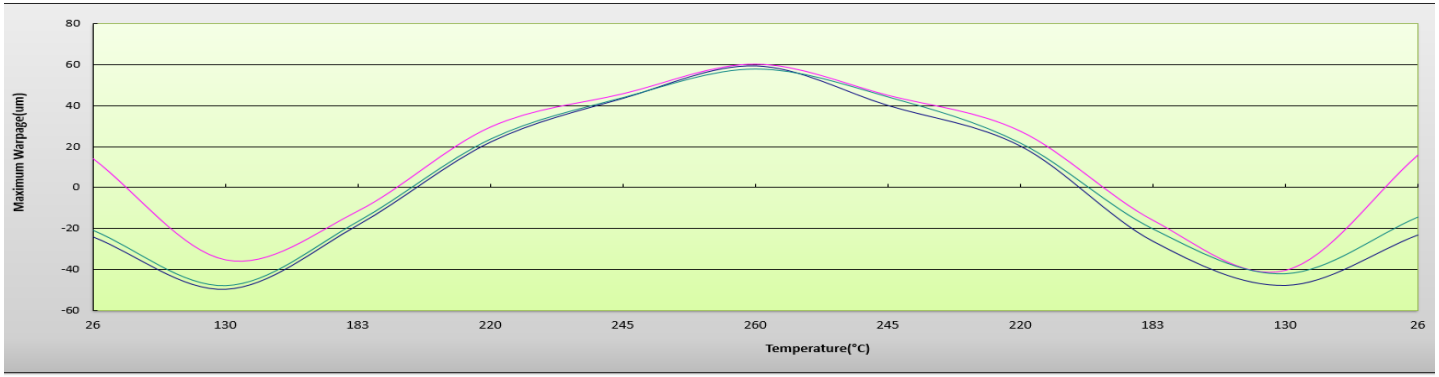
10 MIL DIE, WET WARPAGE DATA (4/4)

Temp. (‘C)	Bake+ MSL3-1	Bake + MSL3-2	Bake + MSL3-3	Avg.
26	-24	14.1	-20.8	-10.2
130	-49.5	-35.2	-47.7	-44.1
183	-18.1	-11.3	-16.4	-15.3
220	22.3	29.6	23.7	25.2
245	43.6	45.8	43.9	44.4
260	59.4	60.2	57.8	59.1
245	40.1	45	44.2	43.1
220	20.3	27.5	21.7	23.2
183	-26.1	-15.9	-20.1	-20.7
130	-47.6	-40.3	-41.9	-43.3
26	-23	15.9	-14.3	-7.1

- Shadow Moiré
- Sample size, 3 wet units
- Bake at 125°C for 24hrs + MSL3 soak
- Max warpage, 60.2 um at reflow < 80 um spec



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ATE VALIDATION

- Assembled two wafers from the same wafer fab-lot to compare device performance

Lot	Step	In	Out	Yield
QERC23917 (8mil)	FT1	80	73	91.25%
QERC24292 (10 mil)	FT1	90	87	96.67%

- ATE Yield
  - ATE yield improved from 91 to 97%
- Failure modes
  - Total 10 unit fail from the table above
  - All these failure are contained in 3 failure modes
- CPK trend review on tested parameters
  - CPK min & max distribution reduced
  - Lower CPK items also reduced

Die thickness increase does not impact ATE yield or device performance.
DDR5 RCD die backside is floating, not for grounding. Die thickness does not impact device performance.

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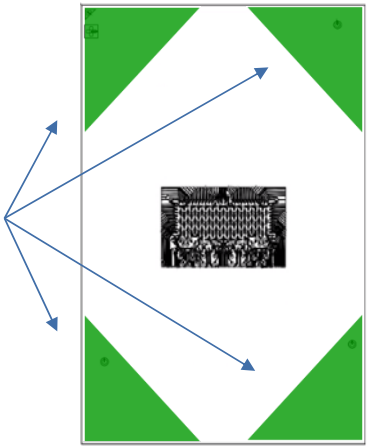
DIMM BLR ASSESSMENT, QUALITATIVE ANALYSIS (1/2)

Samples			X	Y
1	Lot 1	Unit 1	14.79	16.56
		Unit 2	18.73	17.44
		Unit 3	19.31	20.12
2	Lot 2	Unit 1	17.25	15.21
		Unit 2	19.60	13.58
		Unit 3	19.89	13.44
3	Lot 3	Unit 1	17.13	24.22
		Unit 2	18.75	22.09
		Unit 3	15.17	19.18
		Average	**17.85**	**17.98**

- Measured CTE of the DDR5 RCD package
  - X-direction CTE & Y-direction CTE measurement
  - Temperature change from 25 to 100C
  - Effective CTE is about 18 ppm/C

- Die area is less than 6% of total package area!
  - CTE under the die area will be reduced by thicker die
  - However, change in effective CTE between the two corner balls with maximum DNP will be negligible (4 corners with green shades)
  - Hence, DIMM level BLR should be equal or better with lower package warpage (higher SMT quality)



Effective CTE between two corner BGA balls with maximum DNP stays the same.
DIMM level TC performance will be equal or better. Lower warpage provides higher SMT quality.

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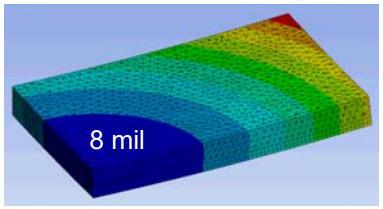
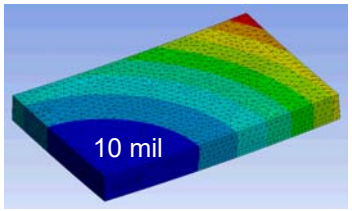
DIMM BLR ASSESSMENT, FEM VALIDATION (2/2)

- FEM Model
  - Simplified quarter-model with 3 layers (substrate, die, and EMC)
  - Temperature change from 25 to 100C to match with CTE measurement condition in previous page
  - Extract XY deformation at package corner with maximum DNP

- XY Deformation analysis
  - ΔX 0.0056834 mm → 0.0056781 mm
  - ΔY 0.0087355 mm → 0.0087257 mm





  - This confirms XY CTE at maximum DNP area does not change with die thickness increase

ΔX and ΔY of solder ball with maximum DNP stays the same.
ΔZ of 10 mil die case will be smaller with lower package warpage. It means equal or higher DIMM level BLR.

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SUMMARY & RECOMMENDATIONS

- Package with 10 mil die thickness improves warpage level significantly, 15 and 33 um for dry and wet cases.
- Less package warpage means lower interfacial stress and higher component level reliability.
- Less warpage at reflow provides higher DIMM assembly yield with higher SMT quality.
- DDR5 RCD package body (13.5 x 8.7 mm) is much bigger than die size (3.36 x 2.16 mm). Die volume increase is 0.4% of the total package body volume. Hence, thicker die driven CTE reduction does not impact effective CTE between two diagonal balls with maximum DNP.
- We are not using DDR5 RCD die back side for grounding. Hence, die thickness does not impact product performance. We confirmed with ATE data from wafers coming from the same fab-lot.
- Based on above data collected, DIMM level performance and component level reliability should be equal or better than previous engineering samples with 8 mil die. This change does not require full system qual and customer may consider QBS or mini-qual with TC only.
- In summary, Renesas intends to ship all DDR5 RCD products with the optimized package stack up, 10 mil die thickness, from March 2021.

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