PRODUCT ADVISORY

Data Sheet Specification Change for Intersil Product ISL9305*

Refer to:
PA11079

Date: August 15, 2011

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To: Our Valued Intersil Customers

Subject: **Data Sheet Specification Change for Intersil Product ISL9305***

This advisory is to inform you that Intersil has updated the data sheet specification for the listed ISL9305* products. The update to the *DCD Output Voltage Slew Rate Control Register* table adds information regarding the potential for damage to the device if the register is set to 111. The old and new versions of the *DCD Output Voltage Slew Rate Control Register* tables are included on the next sheet with the changes shaded in yellow. The updated data sheet is available on the Intersil web site at http://www.intersil.com/data/fn/fn7605.pdf.

Products Affected:

ISL9305IRTAANLZ-T	ISL9305IRTHWBNLZ-T	ISL9305IRTWCLBZ-T
ISL9305IRTBCNLZ-T	ISL9305IRTHWCLBZ-T	ISL9305IRTWCNLZ-T
ISL9305IRTBFNCZ-T	ISL9305IRTHWCNLZ-T	ISL9305IRTWCNYZ-T
ISL9305IRTHAANLZ-T	ISL9305IRTHWCNYZ-T	ISL9305IRTWLNCZ-T
ISL9305IRTHBCNLZ-T	ISL9305IRTHWLNCZ-T	
ISL9305IRTHBFNCZ-T	ISL9305IRTWBNLZ-T	

Intersil will take all necessary actions to conform to agreed upon customer requirements and to ensure the continued high quality and reliability of Intersil products being supplied. Customers may expect to continue receiving product processed to the same established conditions and systems used for manufacturing of material supplied today.

If you have concerns with this advisory, Intersil must hear from you promptly. Please contact the nearest Intersil Sales Office or call the Intersil Corporate line at 1-888-468-3774, in the United States, or 1-321-724-7143 outside of the United States.

Regards,

Jon Brewster

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DCD Output Voltage Slew Rate Control Register – PA11079

Old Table

DCD_SRCTL, address 0x06h

TABLE 8.

BIT	NAME	ACCESS	RESET	DESCRIPTION
B7	DCD2SR_2	R/W	0	DCD2 Slew Rate Setting. DCD2SR[2:0]: 000 to 0.225mV/µs 001 to 0.45mV/µs 010 to 0.90mV/µs 011 to 1.8mV/µs 100 to 3.6mV/µs 101 to 7.2mV/µs 110 to 14.4mV/µs 111 to immediate
B6	DCD2SR_1	R/W	0	
B5	DCD2SR_0	R/W	1	
B4	Reserve	-	0	Reserved
B3	DCD1SR_2	R/W	0	DCD1 Slew Rate Setting. DCD1SR[2:0]: 000 to 0.225mV/µs 001 to 0.45mV/µs 010 to 0.90mV/µs 011 to 1.8mV/µs 100 to 3.6mV/µs 101 to 7.2mV/µs 110 to 14.4mV/µs 111 to immediate
B2	DCD1SR_1	R/W	0	
B1	DCD1SR_0	R/W	1	
B0	Reserve	-	0	Reserved

New Table

DCD_SRCTL, address 0x06h

TABLE 8.

BIT	NAME	ACCESS	RESET	DESCRIPTION
B7	DCD2SR_2	R/W	0	DCD2 Slew Rate Setting. DCD2SR[2:0]: 000 to 0.225mV/µs 001 to 0.45mV/µs 010 to 0.90mV/µs 011 to 1.8mV/µs 100 to 3.6mV/µs 101 to 7.2mV/µs 110 to 14.4mV/µs 111 reserved for system use (Note 7)
B6	DCD2SR_1	R/W	0	
B5	DCD2SR_0	R/W	1	
B4	Reserve	-	0	Reserved
B3	DCD1SR_2	R/W	0	DCD1 Slew Rate Setting. DCD1SR[2:0]: 000 to 0.225mV/µs 001 to 0.45mV/µs 010 to 0.90mV/µs 011 to 1.8mV/µs 100 to 3.6mV/µs 101 to 7.2mV/µs 110 to 14.4mV/µs 111 reserved for system use (Note 7)
B2	DCD1SR_1	R/W	0	
B1	DCD1SR_0	R/W	1	
B0	Reserve	-	0	Reserved

NOTE:

7. The IC can be damaged when output is programmed from high to low and the slew rate register is set to 111.