# PRODUCT ADVISORY

# Data Sheet Specification Change for Intersil ISL89163*, ISL89164*, and ISL89165* Products

**Refer to:**
**PA11087**

**Date: August 29, 2011**

August 29, 2011

To: Our Valued Intersil Customers

Subject: **Data Sheet Specification Change for Intersil ISL89163*, ISL89164*, and ISL89165* Products**

This advisory is to inform you that Intersil has updated the data sheet specification for the listed ISL89163*, ISL89164*, and ISL89165* products. The update is to note 12 referenced in the *Under Voltage* section of the DC Electrical Specifications table. The new note highlights that a *400µs* delay will inhibit the release of the output state when the UV positive going threshold is crossed. The previous revision of the datasheet showed a *200µs* delay. The old and new versions of the note are included on the next sheet with the changes shaded in yellow. The updated data sheet is available on the Intersil web site at http://www.intersil.com/data/fn/fn7707.pdf.

Products affected:

| | | | |
|---|---|---|---|
| ISL89163FBEAZ | ISL89163FRTBZ | ISL89164FRTAZ | ISL89165FBEBZ |
| ISL89163FBEAZ-T | ISL89163FRTBZ-T | ISL89164FRTAZ-T | ISL89165FBEBZ-T |
| ISL89163FBEBZ | ISL89164FBEAZ | ISL89164FRTBZ | ISL89165FRTAZ |
| ISL89163FBEBZ-T | ISL89164FBEAZ-T | ISL89164FRTBZ-T | ISL89165FRTAZ-T |
| ISL89163FRTAZ | ISL89164FBEBZ | ISL89165FBEAZ | ISL89165FRTBZ |
| ISL89163FRTAZ-T | ISL89164FBEBZ-T | ISL89165FBEAZ-T | ISL89165FRTBZ-T |

Intersil will take all necessary actions to conform to agreed upon customer requirements and to ensure the continued high quality and reliability of Intersil products being supplied. Customers may expect to continue receiving product processed to the same established conditions and systems used for manufacturing of material supplied today.

If you have concerns with this advisory, Intersil must hear from you promptly. Please contact the nearest Intersil Sales Office or call the Intersil Corporate line at 1-888-468-3774, in the United States, or 1-321-724-7143 outside of the United States.

Regards,

Jon Brewster

Jon Brewster
Intersil Corporation

PA11087

CC: J. Touvell G. Parker R. Garcia L. Cormie

# Change in Delay Time – PA11087

## Old Note

NOTES:

8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
9. The nominal 20% and 80% thresholds for option C are valid for any value of VDD.
10. This parameter is taken from the simulation models for the input FET. The actual capacitance on this input will be dominated by the PCB parasitic capacitance.
11. The true state input voltage for the non-inverted inputs is greater than the Logic 1 threshold voltage. The true state input voltage for the inverted inputs is less than the logic 0 threshold voltage.
12. A 200µs delay further inhibits the release of the output state when the UV positive going threshold is crossed.

## New Note

NOTES:

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12. **A 400µs delay further inhibits the release of the output state when the UV positive going threshold is crossed.**