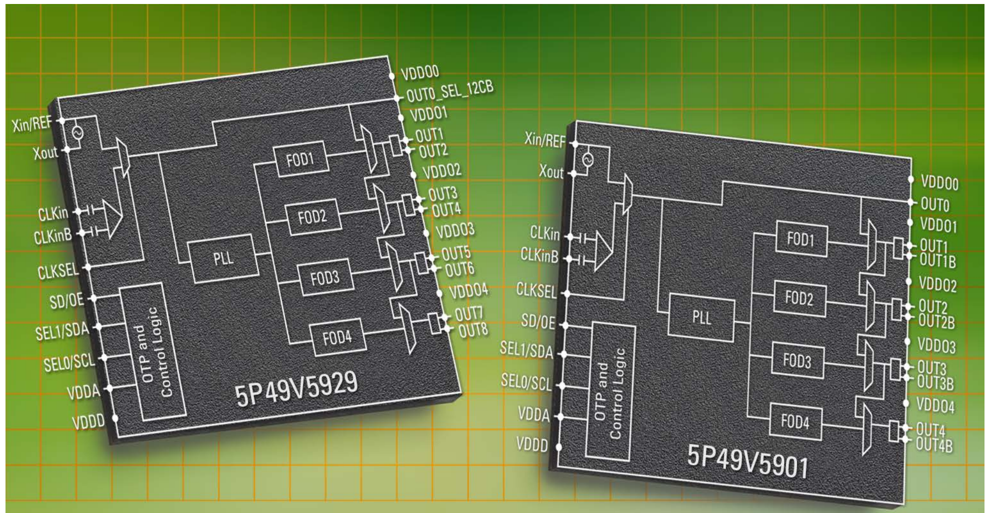
Integrated Device Technology

VersaClock® 5 Programmable Clock Family

ANALOG AND RF | INTERFACE AND CONNECTIVITY | MEMORY AND LOGIC | POWER MANAGEMENT | **TIMING AND SYNCHRONIZATION**



- 50% lower power than competing devices
- Xtal or Clock-in Selection
- Up to 4 single OTP programming operations or store 4 configurations
- Up to 4 Fractional Output Dividers (FOD) allow programming of 4 independent frequencies
- Up to 4 pairs of individually configurable outputs

KEY FEATURES

- High performance, low phase noise PLL, <0.7 ps RMS typical phase jitter on outputs:
  - PCIe® Gen1, 2, 3 compliant clock capability
  - USB 3.0 compliant clock capability
  - Gigabit Ethernet clock capability (1 GbE, 10 GbE)
- Generates up to four independent output frequencies with four fractional output dividers (FODs)
- Four banks of internal non-volatile in-system programmable or factory programmable OTP EPROM
- I²C serial programming interface
- Up to four universal output pairs:
  - Each configurable as one differential output pair or two LVCMOS outputs
  - Up to 9 LVCMOS outputs
- I/O Standards:
  - Single-ended I/Os: 1.8V to 3.3V LVCMOS
  - Differential I/Os: LVPECL, LVDS and HCSL
- Input frequency ranges:
  - LVCMOS Reference Clock Input (XIN/REF): 1 MHz to 200 MHz
  - LVDS, LVPECL, HCSL Differential Clock Input (CLKIN, CLKINB): 1 MHz to 350 MHz
  - Crystal frequency range: 8 MHz to 40 MHz
- Output frequency ranges:
  - LVCMOS Clock Outputs: 1 MHz to 200 MHz
  - LVDS, LVPECL, HCSL Differential Clock Outputs: 1 MHz to 350 MHz
- One reference LVCMOS output clock
- Independent Spread Spectrum capability on each output pair

APPLICATIONS

- Ethernet switch/router
- PCI Express® 1.0/2.0/3.0
- Broadcast video/audio timing
- Processor and FPGA clocking
- Any-frequency clock conversion
- MSAN/DSLAM/PON
- Fibre Channel, SAN
- Telecom line cards
- 1 GbE and 10 GbE

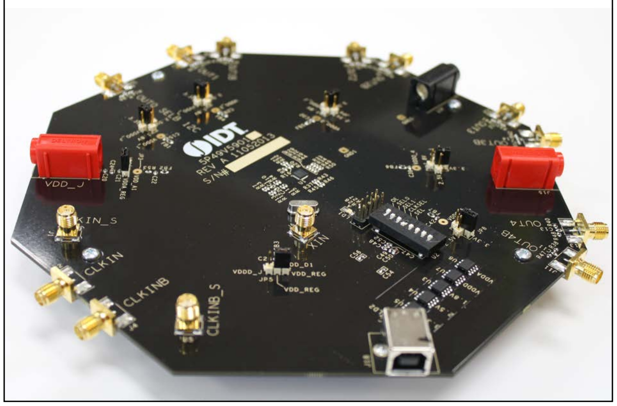
IDT VersaClock 5 are programmable clock generators intended for high-performance consumer, networking, industrial, computing, and data-communications applications.

The VersaClock 5 family is an in-system programmable clock generator featuring up to four universal output pairs capable of producing independent frequencies up to 350 MHz configurable as HCSL, LVPECL, LVDS, or dual LVCMOS outputs. The highly-integrated device consolidates four differential or eight single-ended clock generators, and can store up to four different configuration settings, helping to minimize board space and bill-of-materials. Upon request, devices may be factory-programmed to the customer's desired configuration.

With RMS phase jitter less than 0.7 picoseconds over the full 12 kHz to 20 MHz integration range, the new device meets the stringent jitter requirements of PCI Express® Gen 1/2/3, USB 3.0, and 1G/10G Ethernet. The high-performance clock generator operates at less than 100 mW core power (50 percent lower than competing devices), helping to ease system thermal constraints, reduce operating power expenses, and maximize battery life. The 5P49V5913 and 5P49V5914 devices have a reduced number of universal outputs, enabling customers to get the exact functionality they need on their systems in the most cost-effective manner. Four other devices—5P49V5923, 5P49V5925, 5P49V5927, 5P49V5929—also have reduced functionality, with only LVCMOS outputs (3, 5, 7 or 9) that enable extremely low cost replacement solutions for LVCMOS crystal oscillators.

Part Number	Functionality	Output Type
5P49V5901	PLL with 4 Fractional Output Dividers	4 Configurable Output Pairs + Reference Output
5P49V5913	PLL with 2 Fractional Output Dividers	2 Configurable Output Pairs + Reference Output
5P49V5914	PLL with 3 Fractional Output Dividers	3 Configurable Output Pairs + Reference Output
5P49V5923	PLL with 2 Fractional Output Dividers	2 LVCMOS Outputs + Reference Output
5P49V5925	PLL with 4 Fractional Output Dividers	4 LVCMOS Outputs + Reference Output
5P49V5927	PLL with 3 Fractional Output Dividers	6 LVCMOS Outputs + Reference Output
5P49V5929	PLL with 4 Fractional Output Dividers	8 LVCMOS Outputs + Reference Output

VERSACLOCK 5 FAMILY EVALUATION BOARD



Orderable Part ID	Output Signaling
EVKVC5-5901ALL	LVPECL, LVCMOS, LVDS, HCSL
EVKVC5-5901HCSL	HCSL
EVKVC5-5901LVDS	LVDS
EVKVC5-5901CMOS	LVCMOS
EVKVC5-5901LPECL	LVPECL

FEATURES

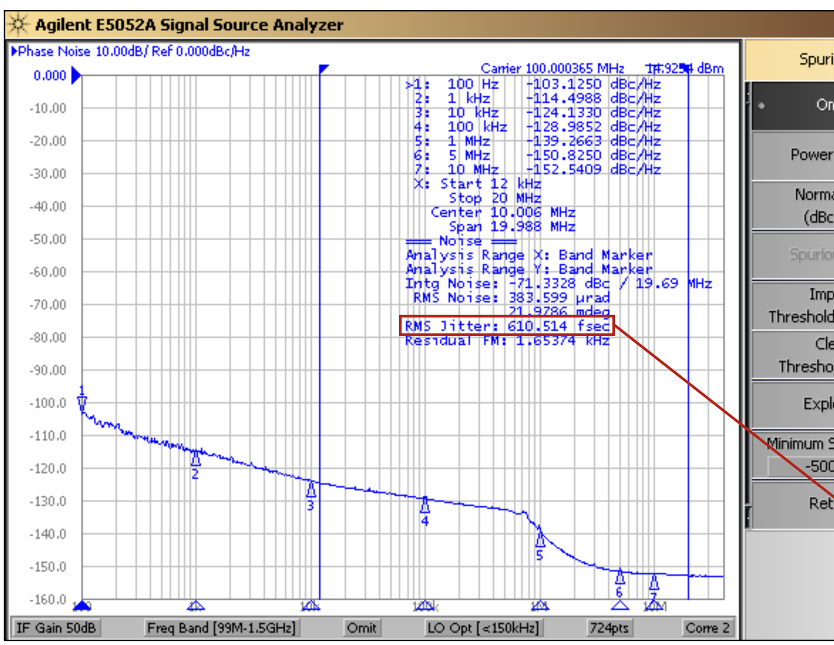
- 4 Differential Outputs or 8 LVCMOS Outputs capable of generating any output frequency using IDT Timing Commander™ software
- SMA connectors for outputs
- When the board is connected to a PC running IDT Timing Commander Software through USB, the device can be configured and programmed to generate frequencies with best-in-class performances
- The 25 MHz crystal installed on the board can source a reference frequency to the device when CLKIN/CLKINB is not used

DEVELOPMENT TOOLS

IDT TIMING COMMANDER™

Making Complex Configurations Simple

IDT Timing Commander is an easy-to-use Windows®-based software platform enabling system design engineers to configure, program and monitor sophisticated timing devices with an intuitive and flexible GUI.



Excellent Phase Noise Over The Entire Frequency Range

Capable of generating up to four independent output frequencies (0 ppm error) with:

- <0.7 ps typ RMS phase jitter (12 KHz to 20 MHz)
- PCIe® Gen 1/2/3 compliant clocks
- USB 3.0, Thunderbolt™ compliant clocks
- 1G/10G Gigabit Ethernet compliant clocks

610 fsec RMS Phase Jitter (12 KHz to 20 MHz)

To request samples, download documentation, or to use the custom Timing Commander tool to program your own devices go to **www.IDT.com/go/versaclock5**

PB_VERSACLOCK5_REVB1114