August 4, 2011

Product Specifications of the M16C/6S1 Group of Microcontrollers

Items	Specification			
Product	M16C/6S1 Group			
Part No.	R5F36S1ENFB	R5F36S1EDFB	R5F36S16NFB	R5F36S16DFB
CPU	M16C/60 Series core			
Supply Voltage	VCC1 = VCC2 = 3.0 V to 3.6 V			
Minimum Instruction Execution time	32.6 nsec (f(BCLK) = 30.72 MHz, VCC1 = VCC2 = 3.0 to 3.6 V)			
Number of basic instructions	91 instructions			
Operating Temperature	−20 to 85℃	−40 to 85℃	−20 to 85℃	−40 to 85℃
Memory Capacity ROM/RAM	256 KB/31 KB		128 KB/20 KB	
Data Flash memory	4 KB × 2 block			
Peripheral Function	Watchdog timer (15-bit × 1 channel with prescaler)			
	DMA controller × 4 channels			
	Timer A: 16-bit × 5 channels			
	Timer B: 16-bit × 6 channels			
	Serial Interface (UART0-UART2), (UART5-UART7) • Clock synchronous/asynchronous × 5 channels • PLC connection × 1 channel • I^2C-bus, IE Bus, special mode 2, SIM(UART2)			
	Multi-master I^2C-bus interface x 1 channel			
	I/O Ports			

Items	Specification
	• Programmable I/O ports: CMOS I/O ports 53 (selectable pull-up resistors) • N-channel open drain ports: 3
	A/D Converter • 10-bit resolution × 18 channels, including sample and hold function • Conversion time: 2.8 µS
PLC Block DCSK mode	Modulation technique: DCSK (Differential Code Shift Keying) Error correction: Short-block error correction, CRC-16 Compliant worldwide regulation: FCC, ARIB, EN50065-1-CELENEC Data transfer rate and Frequency band • FCC and ARIB o Frequency band: 120 to 400 KHz o 7.5 Kbps: Standard mode (SM) o 5.0 Kbps: Robust mode (RM) o 1.25 Kbps: Extremely Robust mode (ERM) • CENELEC o Frequency band: A-band 20 to 80 KHz : B-band 95 to 125 KHz o 2.5 Kbps: Robust mode (RM) o 0.625 Kbps: Extremely Robust mode (ERM) Internal AFE • 10-bit D/A convertor, LPF, line driver amplifier, • 13-bit A/D convertor, VGA, BGR, VDC
PLC Block DCSK-Turbo mode	Modulation technique: DCSK (Differential Code Shift Keying)-Turbo Error correction: Short-block error correction, CRC-16

Items	Specification

	Compliant worldwide regulation: FCC, ARIB, EN50065-1-CELENEC
	Data transfer rate and Frequency band
	
	• FCC and ARIB
	  o Frequency band: 120 to 400 KHz
	  o Up to 500 Kbps @ PHY
	  o Up to 300 Kbps @ MAC payload rate (Communication packet length: 1760-byte)
	• CENELEC-A band
	  o Frequency band: 20 to 80 KHz
	  o Up to 150 Kbps @ PHY
	  o Up to 90 Kbps @ MAC payload rate (Communication packet length: 1760-byte)
	• CENELEC-B band
	  o Frequency band: 95 to 125 KHz
	  o Up to 50 Kbps @ PHY
	  o Up to 30 Kbps @ MAC payload rate (Communication packet length: 1760-byte)
	
	Internal AFE
	
	• 10-bit D/A convertor, LPF, line driver amplifier,
	• 13 bit A/D convertor, VGA, BGR, VDC

Clock generator	4 circuits: • Main clock, sub clock, low-speed on-chip oscillator (125 KHz), PLL frequency synthesizer Oscillation stop detection: • Main clock oscillation stop/re-oscillation detection function Frequency divider circuit: Divide ratio selectable from 1, 2, 4, 8, and 16 Power saving features: Wait mode, stop mode Real-time clock

Items	Specification
Encryption	AES Encryption (Key length: 128-bit)
Package	100 pins, HTQFP (14.0 mm × 14.0 mm × 1.0 mm)

(Remarks)

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