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Product Specifications of the R-Car H1 SoC

Function	Specification	
Product number	R-Car H1 (R8A77790)	
Power supply voltage	3.3 V (IO), 1.5 V (DDR3), 1.2 V (Core), 2.5 V (PCIe, MLB), 1.8 V (SDIF UHS-I)	
CPU core	ARM® Cortex™-A9 Quad (with NEON™)	SH-4A core
Maximum operating frequency	1000 MHz	800 MHz
Processing performance	10000 DMIPS	1760 DMIPS (Effective), 5600 MFLOPS
Cache memory	Instruction cache: 32 KB Operand cache: 32 KB L2 cache: 1 MB	Instruction cache: 32 KB Operand cache: 32 KB
External memory	DDR3-SDRAM (DDR) Maximum operating frequency: 500 MHz Data bus width: 32 bits × 2 channel (4 GB/s × 2 ch)	
Expansion bus	Flash ROM and SRAM, Data bus width: 8 or 16 bits	
	PCI Express 2.0 (1 lane)	
Graphics	PowerVR SGX543MP2 (3D)	
	Renesas graphics processor (2D)	
Video	Display out × 2 ch (RGB888)	
	Video input x 2 ch	
	Video decode processor (H.264/AVC, MPEG-4, VC-1)	
	Media RAM	
	JPEG acceralator	

Function	Specification
	TS interface
	Video image processing (color conversion, image expansion, reduction, filter processing)
	Distortion compensation module (image renderer) × 4 ch
	Image recognition processor
Audio	Sound processing unit × 2 ch
	Sampling rate converter × 10 ch
	Sound serial interface × 10 ch
	MOST DTCP
Storage interfaces	USB 2.0 host interface × 3 ports (w/ PHY)
	SD host interface × 4 ch
	Multimedia card interface
	Serial ATA interface
In-car network automotive peripherals	Media local bus (MLB) interface × 1 ch (6-pin / 3-pin interface selectable)
	CAN Interface × 2 ch
	IEBus interface
	GPS baseband module
Security	Crypto engine (AES, DES, Hash, RSA)
	Secure RAM
Other peripherals	DMA controller LBSC DMAC: 3 ch / SuperHyway-DMAC: 4 ch / HPB DMAC: 39 ch
	32-bit timer × 9 ch
	PWM timer × 7ch
	I2C bus interface × 4 ch
	Serial communication interface (SCIF) × 8 ch
	Serial peripheral interface (HSPI) × 3 ch
	Ethernet controller (IEEE802.3u, RMII, without PHY)
	Interrupt controller (INTC)

Function	Specification
	Clock generator (CPG) with built-in PLL
	On-chip debugger interface
Low power mode	DPS/VS (CPU core, PowerVR SGX543MP2, VPU, IMP) AVS (adaptive voltage scaling) function DDR-SDRAM power supply backup mode
Package	832-pin FCBGA (27 × 27 mm)
Development environment	ICE for ARM CPU available from different vendors
Evaluation board	A user system development reference platform offering the following features is also available, enabling the users to carry out efficient system development. (1) Includes car information system-oriented peripheral circuits, providing users with an actual device verification environment. (2) Can be used as a software development tool for application software, etc. (3) Allows easy implementation of custom user functions.
Middleware	Wide variety of middleware such as H.264, MPEG-4 and VC-1 for video is available to realize complete system concept.