Separate Sheet

Product Specifications of the RAA604S00

Product No.	RAA604S00
Operating frequency band	863 MHz – 928 MHz
Modulation /Data rate (kbps)	2FSK/GFSK：10/20/40/50/100/150/200/300 4FSK/GFSK：200/400
Current consumption (RF portion)	Vcc = 3.3 V, typ. RX: 6.3 mA, RX wait: 5.8 mA / TX：20 mA (+10 dBm)
Receiving sensitivity	-114 dBm（GFSK 10 Kbps、BER<0.1%） -104 dBm（GFSK 100 Kbps、BER<0.1%）
IEEE802.15.4g/4e -compliant H/W function	Filtering for Dual Sub-GHz Communication Transmit frame automatic generating function *Preamble length: 4 to 1000 bytes setting possible Automatic ACK reply/receiving function support
Package	32-pin 5 mm x 5 mm QFN

RL78/G1H main specifications

Item		R5F11FLJ	R5F11FLK	R5F11FLL
Code flash memory (KB)		256 KB	384 KB	512 KB
Data flash memory (KB)		8 KB	8 KB	8 KB
RAM (KB)		24 KB	32 KB	48 KB
Address space		1 MB		
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillator, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz (VDD = 2.7 to 3.6 V) HS (high-speed main) mode: 1 to 16 MHz (VDD = 2.4 to 3.6 V) LS (low-speed main) mode: 1 to 8 MHz (VDD = 1.8 to 3.6 V)		
	High-speed on-chip	HS (high-speed main) mode: 1 to 32 MHz (VDD = 2.7 to 3.6 V), HS (high-speed main) mode: 1 to 16 MHz (VDD = 2.4 to 3.6		

	oscillator clock (fIH)	V), LS (low-speed main) mode: 1 to 8 MHz (VDD = 1.8 to 3.6 V),
Subsystem clock		XT1 (crystal) oscillator, external subsystem clock input (EXCLKS) 32.768 kHz (TYP.)
Low-speed on-chip oscillator clock		15 kHz (TYP.)
RF base clock		48 MHz (TYP.)
RF slow clock		External clock input for RF unit (EXCLKS) 32.768 kHz (TYP.)
General-purpose register		8 bit x 32 registers (8 bit x 8 registers x 4 banks)
Minimum instruction execution time		0.03125 us (High-speed on-chip oscillator clock: fIH = 32 MHz operation)
		0.05 us (High-speed system clock: fMX = 20 MHz operation)
		30.5 us (Subsystem clock: fSUB = 32.768 kHz operation)
Instruction set		·instruction set (8/16 bit) · Adder and subtractor/ logical operation (8/16 bit) · Multiplication (8 bit x 8 bit, 16 bit x 16 bit), Division (16 bit ÷ 16 bit, 3 bit ÷ 32 bit) · Multiplication and Accumulation (16 bit x 16 bit + 32 bit) · Rotate, barrel shift, and bit manipulation (set, reset, test, and boolean operation), etc.
I/O port	Total	41
	CMOS I/O	26
	CMOS input	5
	CMOS output	1
	N-ch open-drain I/O (6 V tolerance)	4
	GPIO (RF unit)	5
SubGHz RF	Operating frequency band	863 MHz - 928 MHz

transceiver	Modulation /Data rate (kbps)	2FSK/ GFSK ： 10/ 20/ 40/ 50/ 100/ 150/ 200/ 300 4FSK/ GFSK ： 200/ 400
	Current consumption (RF portion)	Vcc = 3.3 V, typ. RX:6.3 mA, RX wait: 5.8 mA / TX: 20 mA (+10 dBm)
	Receiving sensitivity	-114 bdBm（GFSK 10 bKbps、BER <0.1%） -104 bdBm（GFSK 100 bKbps、BER <0.1%）
	IEEE802.15.4g/ 4e -compliant H/W function	Filtering for Dual Sub-GHz Communication Transmit frame automatic generating function *Preamble length: 4 to 1000 byte setting possible Automatic ACK reply/ receiving function support
Timer	16-bit timer	9 channels
	Watchdog timer	1 channel
	Real-time clock (RTC)	1 channel
	12-bit interval timer	1 channel
	Timer Output	1 channel
Clock output/buzzer output		2
		· 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: fMAIN = 20 MHz operation) = 20 MHz operation).024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: fSUB = 32.768 kHz operation)
10-bit resolution A/D converter		6 channels
Serial interface		CSI/UART: 2 channels OSI: 1 channel
	I2C bus	2 channels

Multiplier and divider/multiply-accumulator		Multiplication: 16 bit x 16 bit = 32 bit (Unsigned or signed) Division: 32 bit x 32 bit = 32 bit (Unsigned) Multiply-accumulate: 16 bit x 16 bit + 32 bit = 32 bit (Unsigned or signed)
Data transfer controller (DTC)		21 sources
Vectored interrupt sources	Internal	26
	External	7
Reset		• Reset by RESET pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution（Note 3） • Internal reset by RAM parity error • Internal reset by illegal-memory access
Power-on-reset circuit		·ower-on-reset circuit 1.51 (TYP.) (TYP.)r-down-reset: 1.50 (TYP.)
Voltage detector		·voltage detector: 1.88 V to 3.13 V (10 stages) voltage detector: 1.84 V to 3.05 V (10 stages)
On-chip debug function		Provided
Power supply voltage		VDD = 1.8 - 3.6 V
Operating ambient temperature		TA = -40 ºC - +85 ºC (A: Consumer applications, D: Industrial applications)
Package		64-pin 9 mm x 9 mm VQFN (0.5 mm pitch)