

September 8, 2011

Product Specifications of the SH726A and SH726B MCUs

1. SH726A

Item		Specification		
Product Classification		SH726A		
Product Code*	16 mm square, 0.5 mm pitch	Industrial usage, etc.	R5S726A0D216FP	R5S726A1D216FP
		Car accessories	R5S726A0P216FP	R5S726A1P216FP
	14 mm square, 0.4 mm pitch	Industrial usage, etc.	R5S726A2D216FP	R5S726A3D216FP
		Car accessories	R5S726A2P216FP	R5S726A3P216FP
Power Supply Voltage		3.3 V / 1.25 V		
Operating Temperature		-40 to +85°C		
CPU Core		SH2A-FPU		
CPU Instruction Number		112 (Including FPU related instructions)		
Built-In RAM		Large Capacity Memory: 1.25 MB (with data retention area)		
		High Speed Memory: 64 KB		
Cache Memory		16 KB (Instruction 8 K / Operand 8 K Separated, 4-way set associative)		
External Memory		Bus Clock Maximum 72 MHz		
		Direct Connect to SRAM and SDRAM by Bus State Controller		
		Address Space 8 MB × 2		
		Data Bus Width: 8- / 16-bit		
Built-In Peripheral Function		SPI Multi I/O Bus Controller		
		Multi-Function Timer Pulse Unit 2 (MTU2) × 5		
		16-bit Compare Match Timer (CMT) × 2		

Item	Specification	
	A/D Converter (10-bit resolution) × 6 Channels	
	USB 2.0 Host/Function Module	
	Serial communication interface with FIFO (SCIF) × 5 Channels	
	(Clocked synchronous or asynchronous mode selectable)	
	I ² C Bus Interface × 4 Channels	
	Serial Sound Interface × 4 Channels	
	Renesas Serial Peripheral Interface × 2 Channels	
	Serial I/O with FIFO	
	Renesas SPDIF Interface	
	SD Host Interface (It requires SD Card License)	
	Real Time Clock	
	CD-ROM Decoder	
	Sampling Rate Convertor × 3 Channels	
	IEBus Interface	
	-	CAN Interface × 2 Channels
	On-chip Debug Function <ul style="list-style-type: none"> • Advanced User Debugger-II • User Debug Interface • User Break Controller × 2 Channels 	
	Direct Memory Access Controller × 16 Channels	
	Interrupt Controller	
Watch Dog Timer		

Item	Specification
	Clock Pulse Generator (CPG): Input clock can be multiplied by 18 (max.) by the internal PLL circuit
Boot Modes	Boot mode 0: Boots the LSI from the memory connected to the CS0 space
	Boot mode 1: Boots the LSI, through low-speed communication, from the serial flash memory connected to channel 0 of the Renesas serial peripheral interface
Power-down modes	Sleep mode
	Software standby mode
	Deep standby mode
	Module standby mode
Package	120-pin QFP (16 mm × 16 mm) 0.5 mm pitch / 120-pin QFP (14 mm × 14 mm) 0.4 mm pitch

2. SH726B

Item	Specification							
Product Classification	SH726B							
Product Code*	<table border="1"> <tr> <td rowspan="2">20 mm square, 0.5 mm pitch</td> <td>Industrial usage, etc.</td> <td>R5S726B0D216FP</td> <td>R5S726B1D216FP</td> </tr> <tr> <td>Car accessories</td> <td>R5S726B0P216FP</td> <td>R5S726B1P216FP</td> </tr> </table>	20 mm square, 0.5 mm pitch	Industrial usage, etc.	R5S726B0D216FP	R5S726B1D216FP	Car accessories	R5S726B0P216FP	R5S726B1P216FP
20 mm square, 0.5 mm pitch	Industrial usage, etc.		R5S726B0D216FP	R5S726B1D216FP				
	Car accessories	R5S726B0P216FP	R5S726B1P216FP					
Power Supply Voltage	3.3 V / 1.25 V							
Operating Temperature	-40 - +85°C							
CPU Core	SH2A-FPU							
CPU Instruction Number	112 (Including FPU related instructions)							
Built-In RAM	Large Capacity Memory: 1.25 MB (with data retention area)							
	High Speed Memory: 64 KB							

Item	Specification		
Cache Memory	16 KB (Instruction 8 K / Operand 8 K Separated, 4-way set associative)		
External Memory	Bus Clock Maximum 72 MHz		
	Direct Connect to SRAM and SDRAM by Bus State Controller		
	Address Space 64 MB × 5		
	Data Bus Width: 8- / 16-bit		
Built-In Peripheral Function	SPI Multi I/O Bus Controller		
	Multi-Function Timer Pulse Unit 2 (MTU2) × 5		
	16-bit Compare Match Timer (CMT) × 2		
	A/D Converter (10-bit resolution) × 8 Channels		
	USB 2.0 Host/Function Module × 2 Channels		
	Serial communication interface with FIFO (SCIF) × 5 Channels (Clocked synchronous or asynchronous mode selectable)		
	I ² C Bus Interface × 4 Channels		
	Serial Sound Interface × 4 Channels		
	Renesas Serial Peripheral Interface × 3 Channels		
	Serial I/O with FIFO		
	Renesas SPDIF Interface		
	SD Host Interface (It requires SD Card License)		
	Real Time Clock		
	CD-ROM Decoder		
	Sampling Rate Convertor × 3 Channels		
	IEBus Interface		
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%; text-align: center;">-</td> <td style="width: 30%;">CAN Interface × 2 Channels</td> </tr> </table>	-	CAN Interface × 2 Channels
	-	CAN Interface × 2 Channels	
On-chip Debug Function			

Item	Specification
	<ul style="list-style-type: none"> • Advanced User Debugger-II • User Debug Interface • User Break Controller × 2 Channels <p>Direct Memory Access Controller × 16 Channels</p> <p>Interrupt Controller</p> <p>Watch Dog Timer</p> <p>Clock Pulse Generator (CPG): Input clock can be multiplied by 18 (max.) by the internal PLL circuit</p>
Boot Modes	<p>Boot mode 0: Boots the LSI from the memory connected to the CS0 space</p> <p>Boot mode 1: Boots the LSI, through low-speed communication, from the serial flash memory connected to channel 0 of the Renesas serial peripheral interface</p>
Power-down modes	<p>Sleep mode</p> <p>Software standby mode</p> <p>Deep standby mode</p> <p>Module standby mode</p>
Package	144-pin QFP (20 mm × 20 mm) 0.5 mm pitch

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