November 5, 2010

Specifications of New 16-Bit IO-Link Microcontrollers

Item		μPD78F8040F1	μPD78F8041F1	μPD78F8042F1	μPD78F8043F1
Internal memory	Flash memory	32 KB	64 KB	96 KB	128 KB
	RAM	4 KB	4 KB	6 KB	7 KB
Memory space		1 MB			
Main system clock (Oscillation frequency)	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 2 to 20 MHz: V_{DD} = 3.0 to 5.5 V			
	Internal high-speed oscillation clock	Internal oscillation 1 MHz (Typ.), 8 MHz (Typ.): V_{DD} = 3.0 to 5.5 V			
	20 MHz internal high-speed oscillation clock	Internal oscillation 20 MHz (Typ.): V_{DD} = 3.0 to 5.5 V			
Internal low-speed oscillation clock (dedicated to WDT)		Internal oscillation 30 kHz (Typ.): V_{DD} = 3.0 to 5.5 V			
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)			
		0.125 μs (Internal high-speed oscillation clock: f_{IH} = 8 MHz operation)			
Instruction set		• 8-bit operation, 16-bit operation • Multiplication (8 bits × 8 bits) • Bit manipulation (Set, reset, test, and Boolean operation), etc.			

I/O port (MCU)		CMOS I/O: 23Note 1 CMOS input: 1 N-ch open-drain I/O (6 V tolerance): 2
I/O port (IO-Link transceiver)		IO-Link I/O: 1 (CQ)
Timer		• 16-bit timer: 12 channels (Timer input: 6 channels, Timer output: 6 channels) • Watchdog timer: 1 channel
	Timer output	6 (PWM outputs: timer array unit 0: 4Note 2, timer array unit 1: 2Note 2)
A/D converter		10-bit resolution × 6 channels (AV_{REF} = 1.8 to 5.5 V)

Notes:

1. Three of these pins (P11/RxD0, P50/INTP1, and P51/INTP2) are used for IO-Link communication. They must be connected to the IO-Link transceiver. The user connects P11/RxD0, P50/INTP1, and P51/INTP2 to RXD, ILIM, and WAKE respectively on the PCB.
2. The number of outputs varies depending on the setting.

Item		μPD78F8040F1	μPD78F8041F1	μPD78F8042F1	μPD78F8043F1
Serial interface		• IO-Link (use UART0): 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • UART supporting LIN-bus: 1 channel • I^2C bus: 1 channel			
Multiplier/divider		• 16 bits × 16 bits = 32 bits (multiplication) • 32 bits ÷ 32 bits = 32 bits (division)			
DMA controller		2 channels			
Vectored interrupt sources	Internal	28			
	External	5 Note 1			
Reset		• Reset by RESET pin • Internal reset by watchdog timer • Internal reset by power-on-clear			

	• Internal reset by low-voltage detector • Internal reset by illegal instruction execution Note 2 • Internal reset by a reset processing check error
Power-on-clear circuit	• Power-on-reset:1.61 ±0.09 V • Power-down-reset:1.59 ±0.09 V
Low-voltage detector	3.15 V to 4.22 V (8 stages)
On-chip debug function	Provided
Power supply voltage	V_{DD} = 3.0 to 5.5 V
Operating ambient temperature	TA = −40 to +85°C
Package	• 56-pin plastic FBGA (4 × 7)

Notes:

1. The user connects P11/RxD0, P50/INTP1, and P51/INTP2 to RXD, ILIM, and WAKE respectively on the PCB.
2. An illegal instruction is generated when instruction code FFH is executed. Reset by illegal instruction execution is not issued during emulation by the in-circuit emulator or on-chip debug emulator.