

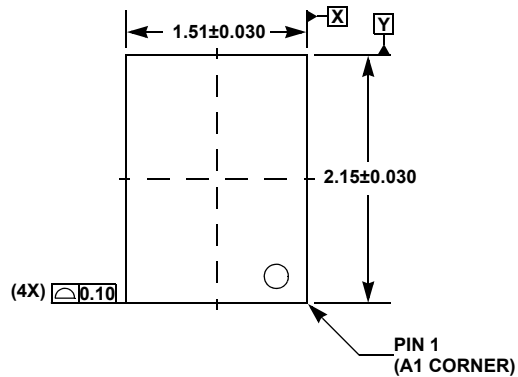
# Plastic Packages for Integrated Circuits

## Package Outline Drawing

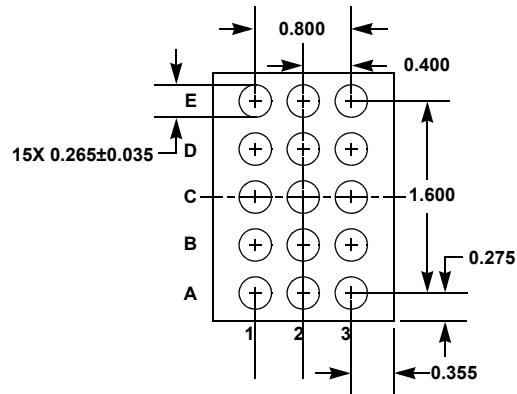
### W3x5.15

15 BALL WAFER LEVEL CHIP SCALE PACKAGE (WLCSP 0.4mm pitch)

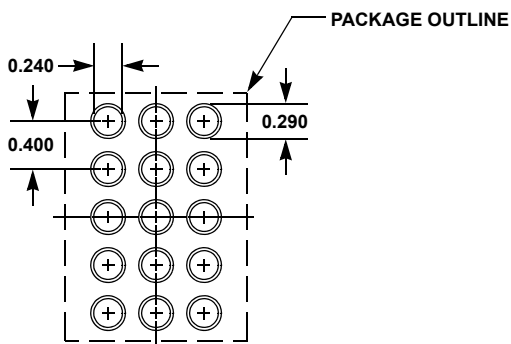
Rev 1, 6/14



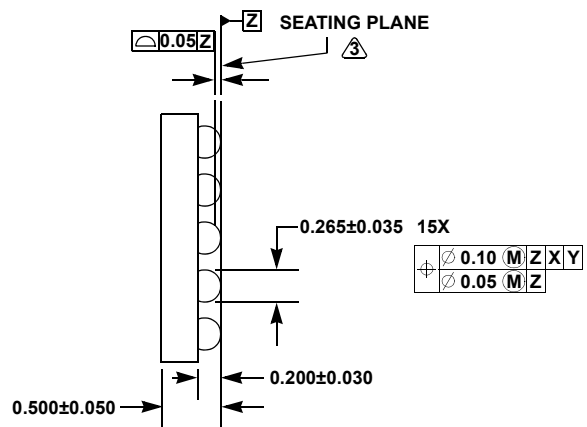
TOP VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

#### NOTES:

1. Dimensions and tolerance per ASME Y 14.5M - 1994.
2. Dimension is measured at the maximum bump diameter parallel to primary datum **Z**.
3. Primary datum **Z** and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.
5. There shall be a minimum clearance of 0.10mm between the edge of the bump and the body edge.