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Renesas Electronics Corporation

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Renesas Starter Kit 2+ for SH/7670

User's Manual

Renesas Single-Chip Microcomputer
SH Family

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Precautions

This Renesas Starter Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures;

- ensure attached cables do not lie across the equipment
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that which the receiver is connected
- power down the equipment when not in use
- consult the dealer or an experienced radio/TV technician for help NOTE: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken;

- The user is advised that mobile phones should not be used within 10m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Renesas Starter Kit does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

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Chapter 1. Preface

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Glossary

CPLD	CMOS Programmable Logic Device	PC	Program Counter
CPU	Central Processing Unit	RSK+	Renesas Starter Kit+
E10A-FSK	On-chip debugger module	SSI	Serial sound interface
HEW	High-performance Embedded Workshop	STI	Stream interface
LCD	Liquid crystal Display	USB	Universal Serial Bus
LED	Light Emitting Diode	RAM	Random Access memory
ROM	Read only memory	TFT	Thin film transistor Display

Chapter 2.Purpose

This RSK is an evaluation tool for Renesas microcontrollers.

This manual describes the technical details of the RSK hardware. The Quick Start Guide and Tutorial Manual provide details of the software installation and debugging environment.

Features include:

- Renesas Microcontroller Programming.
- User Code Debugging.
- User Circuitry such as Buttons, Switches and LEDs.
- User or Example Application.
- Sample peripheral device initialisation code.

The RSK2+ board contains all the circuitry required for microcontroller operation.

Chapter 3. Power Supply

3.1. Requirements

This RSK2+ operates from an external 12V (centre positive) power supply unit.

A diode provides reverse polarity protection only if a current limiting power supply is used.

All RSK2+ boards are supplied with an E10A debugger.

All RSK2+ boards have an optional centre positive supply connector using a 2.0mm barrel power jack. Following table describes about jumper settings for power supply section. Default settings are in **BOLD**.

Option Link Settings				
Reference	Function	Fitted	Removed	Related To
5V_SEL_1	Power supply configuration	Enables 5V supply to the board	Disables 5V supply to the board Enables 12V supply connection to the board	5V_SEL_2
5V_SEL_2	Power supply Configuration	Enables 5V supply to the board	Disables 5V supply to the board. Enables 12V supply connection to the board.	5V_SEL_1

Table 3-3-1: Jumper settings-Power supply

Warning

The RSK2+ is neither under nor over voltage protected. Use a centre positive supply for this board.

3.2. Power up Behaviour

When the RSK is purchased the RSK2+ board has the 'Release' or stand alone code from the example tutorial code pre-programmed into the Renesas microcontroller. On powering up the board the user LEDs will start to flash.

4.2. Board Dimensions

The following diagram gives the board dimensions and connector positions. All through hole connectors are on a common 0.1" grid for easy interfacing.

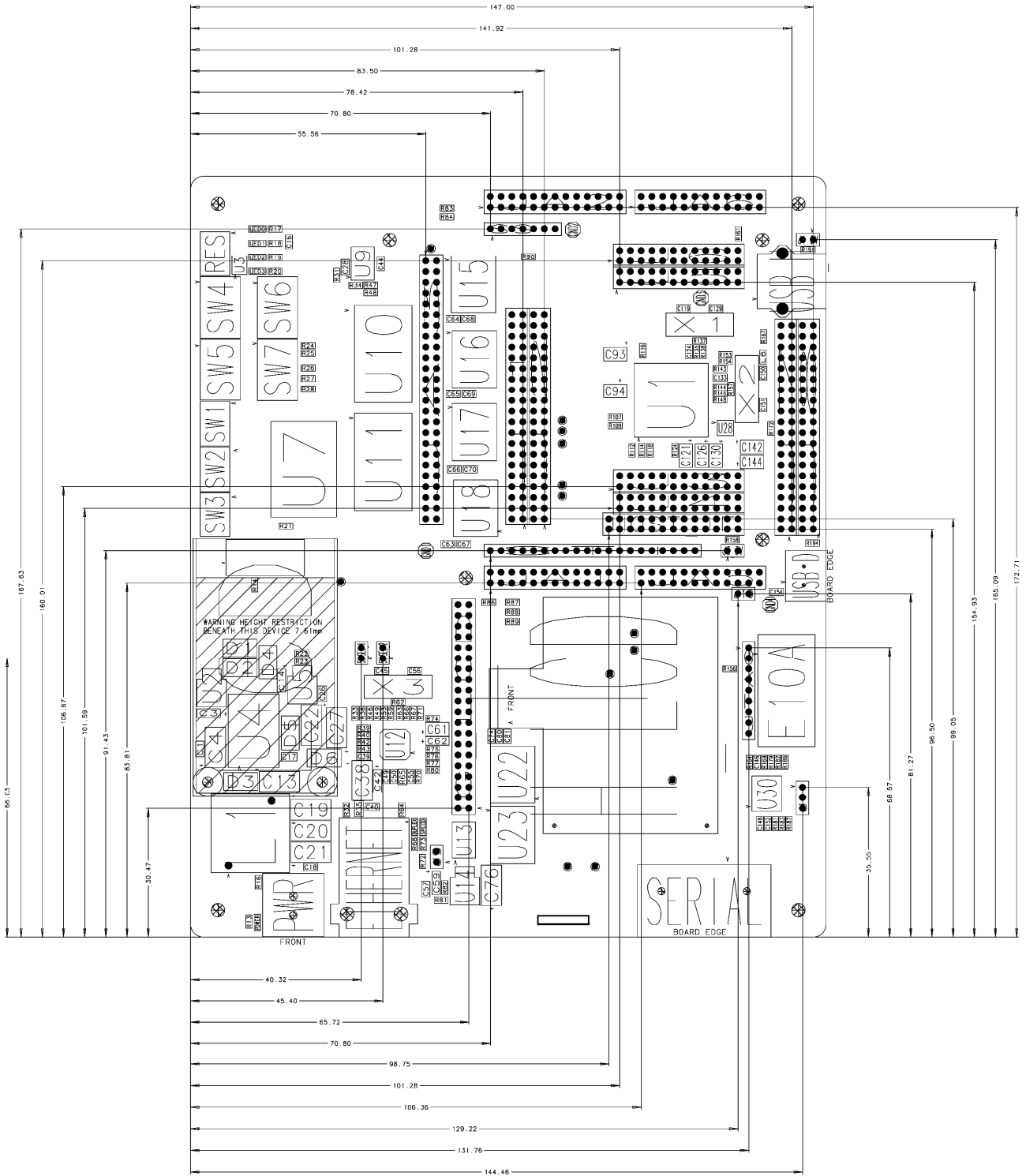


Figure 4-2: Board Dimensions

Chapter 5. Block Diagram

Figure 5-1 shows the CPU board components and their connectivity.

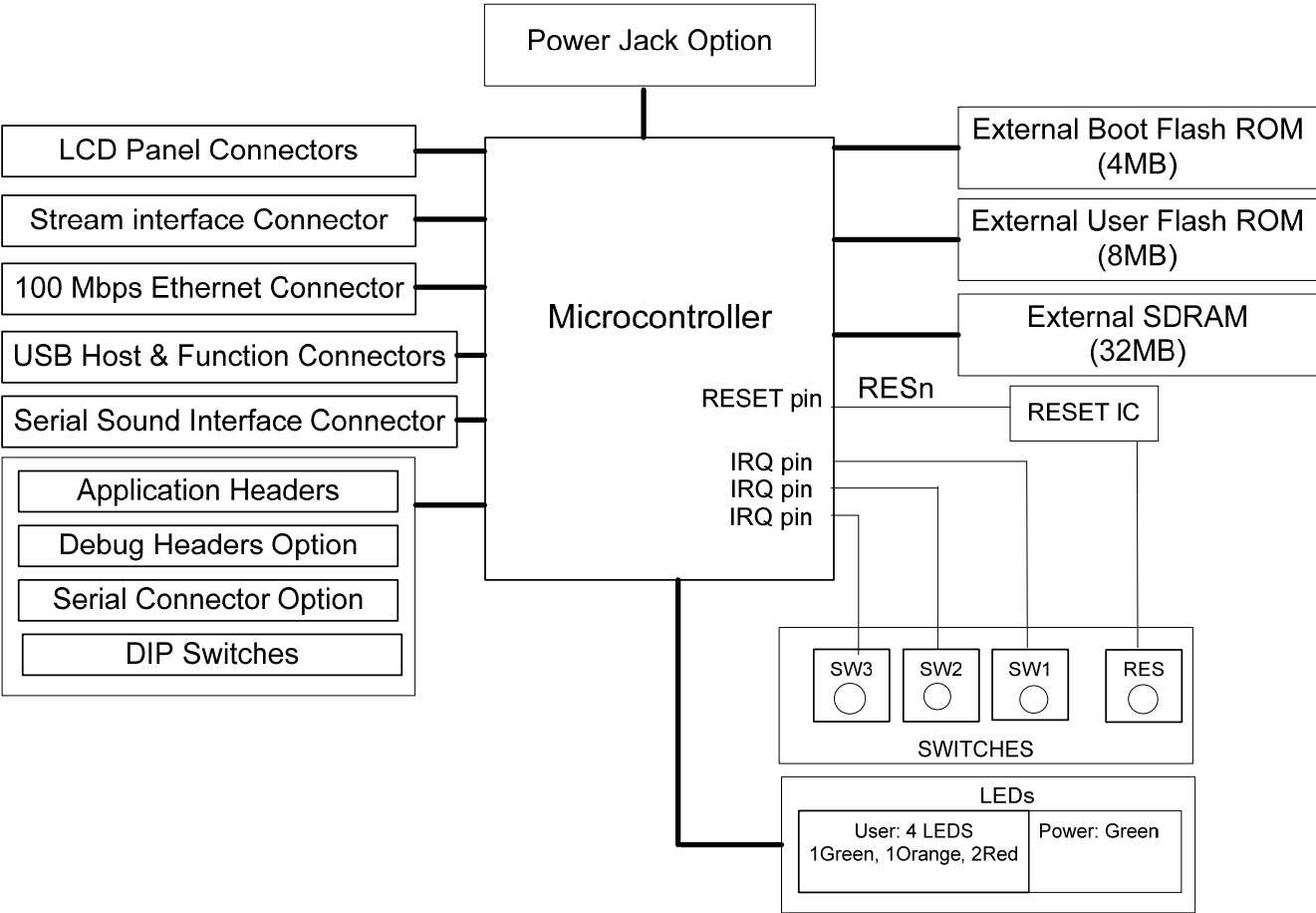


Figure 5-1: Block Diagram

Figure 5-2 shows the E10A connections to the RSK2+.

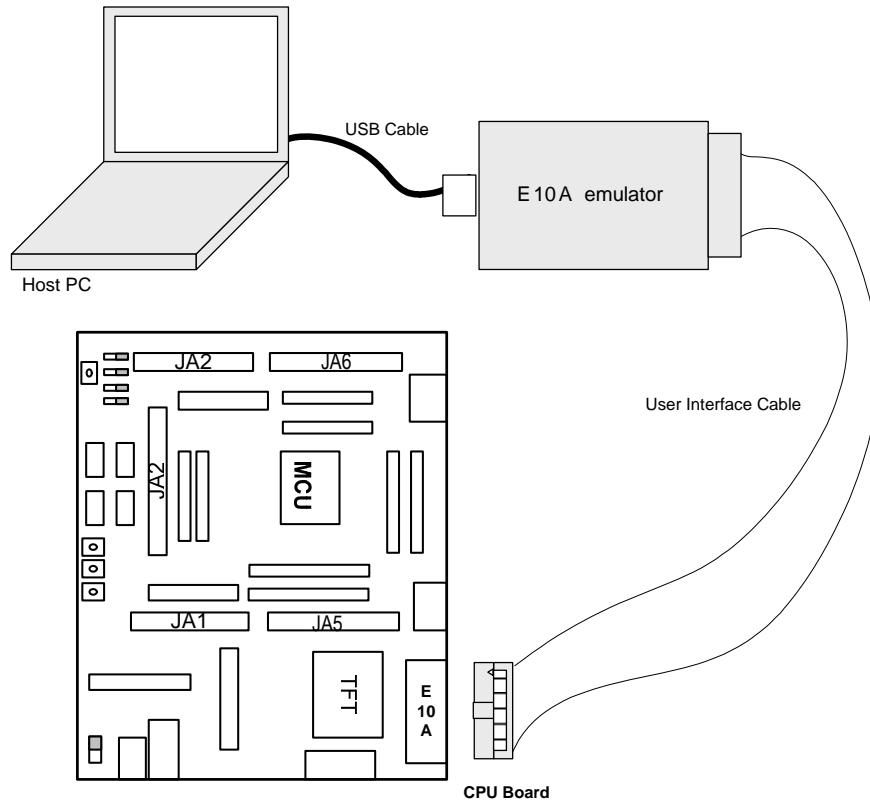


Figure 5-2: RSK2+ E10A Connections

Chapter 6. User Circuitry

6.1. User Switches

There are four user switches located on the CPU board. The function of each button and its connection are shown in Table 6-1
Switch Functions

Switch	Function	Microcontroller
RES	When pressed, the RSK2+ microcontroller is reset.	RESn, Pin W18
SW1*	Connects to an IRQ input for user controls. Note: to connect this button to the CPU please check that dip-switch SW5.1 is in the 'On' position (for details refer to schematic).	IRQ4n, Pin N1 (Port D pin 4)
SW2*	Connects to an IRQ line for user controls. Note: to connect this button to the CPU please check that dip-switch SW5.3 is in the 'On' position (for details refer to schematic).	IRQ5n, Pin N2 (Port D, pin 5)
SW3*	Connects to an IRQ line for user controls. Note: to connect this button to the CPU please check that dip-switch SW5.5 is in the 'On' position (for details refer to schematic).	IRQ6n, Pin N3 (Port D, pin 6)

Table 6-1 Switch Functions

*Refer to schematic for detailed connectivity information.

6.2. LEDs

There are seven LEDs on the RSK2+ board. The green 'POWER' LED lights when the board is powered. The four user LEDs are connected to an IO port and will light when their corresponding port pin is set low. Two green LEDs (placed near Ethernet PHY LAN8700i device) light when Ethernet connection is established, for details refer to Chapter 6.5

Table 6-2, below, shows the User LED pin references and their corresponding microcontroller port pin connections.

LED Reference (As shown on silkscreen)	Colour	Microcontroller Port Pin	Microcontroller Pin Number
LED0	Green	Port E4	Y13
LED1	Orange	Port E5	W13
LED2	Red	Port E10	W15
LED3	Red	Port E11	W16

Table 6-2 LED Ports

6.3. Serial port

Serial port SCIF2 is connected to the standard on-board RS232 header (Male). Serial port SCIF1 can optionally be connected to the same RS232 header, for details please refer to schematic. Please use standard serial RS232 null-modem cable to connect RSK2+ board to a PC.

The default serial port connections are listed in Table 6-3.

Description	Function	Microcontroller Port Pin	Fit for RS232	Default State
SCI1 Rx	Spare Serial Port	W14	R187	Not fitted
SCI1 Tx	Spare Serial Port	V14	R186	Not Fitted
SCI2 Rx	Default serial port	Y15	R169	Fitted
SCI2 Tx	Default serial port	Y16	R180	Fitted

Table 6-3 Serial Port settings

The SCI1 port pins are also available on JA2 header. The SCI2 port pins are available on JA6 header. For details please refer to schematic.

6.4. USB

The USB module can be used either for USB host or function (device) modes. For the USB host mode the on-board 'USB_H' connector must be used. For the USB function mode please use on-board 'USB_D' connector.

Table 6-4 contains details of the signal descriptions and pin connections.

Description	Function	Microcontroller Pin Number	Header Pins
VBUS	Function mode: External USB connection monitor pin. Host mode: On-board USB power supply pin.	W9	J8-17
USB_D+	USB data I/O pin	Y9	Not available
USB_D-	USB data I/O pin	Y8	Not available
USB_X1	USB clock pin	W12	J8-23*
USB_X2	USB clock pin	Y12	J8-24*
REFIN	Reference input	Y11	-

Table 6-4 USB module settings

*SW4.1 and SW4.3 must be in the 'On' position while SW4.2 in OFF position for USB_H mode. SW4.1 and SW4.3 must be in the 'OFF' position while SW4.2 in ON position for USB_D (function) mode. For details please refer to Table 6-16.

The host power is supplied by a controlled 500mA MOSFET switch with overload protection. IRQ7n is connected to this device to provide overload sensing for devices connected to the host USB port. The device is self resetting when the overload is removed.

When this board is connected as a function device the VBUS signal is connected to a logic device input. To protect this device from having a voltage applied when the main power is turned off on the PCB a diode is fitted in the power supply. This will try to power the board from the connected host device. It is likely that this will shut down the connected host unless it is in high power mode. Please ensure that when developing USB function applications that the USB cable is removed when removing power from this product. Operation is not expected when the product is powered from the function USB port.

The single USB channel is split between the Host and Function connectors using a USB Mux Switch. Care is required when routing Hi-Speed USB signals on your applications. On switching SW4-3 the USB signals are routed to the other connector and disconnected from the current selection.

6.5. Ethernet

The Ethernet module conforms to the Ethernet or IEEE802.3 media access control (MAC) standard. Ethernet controller is connected to the direct memory access controller for Ethernet controller (E-DMAC) and carries out high-speed data transfer to and from the memory. In addition the Ethernet controller is connected to on-board SMSC LAN8700i physical layer (PHY) chip enabling it to perform transmission and reception of Ethernet frames. The hardware address of the LAN8700i is predefined as '0x1F'.

There are two Ethernet LEDs on the RSK2+ board and two LEDs on the on-board Ethernet RJ-45 connector. The on-board green SPEED LED lights when 100 Mbit connection is established between the PHY device and any other connected Ethernet device. The green DUPLEX LED lights when Full-Duplex connection is established between the PHY device and any other connected Ethernet device. The embedded Ethernet connector green LED lights when there is a link with the other devices. The yellow LED lights when there is a network activity.

Table 6-5 contains details of the signal descriptions and pin connections.

LED Reference (As shown on silkscreen)	Colour	LAN8700i Port Pin	LAN8700i Pin Number
SPEED	Green	SPEED100_PHYAD0	9
DUPLEX	Green	FDUPLEX_PHYAD3	12
Ethernet connector: Yellow LED	Yellow	ACTIVITY_PHYAD2	11
Ethernet connector: Green LED	Green	LINK_PHYAD1	10

Table 6-5 Ethernet module settings

6.5.1. Ethernet MAC Address

This board contains an SPI EEPROM device (U29). This device has been pre-programmed with an individual MAC address for the board. The first six locations in the device contain the MAC address in hexadecimal numbers starting with the most significant byte. The rest of this EEPROM device is available for customer use. However care must be taken to store the existing value in the device before it is erased.

6.6. Debug LCD Module

A debug LCD module is embedded on the RSK2+ board. The debug LCD module uses a 4 bit interface to reduce the CPU pin allocation. The contrast control is set by a resistor on the supplied display module. The LCD module must be connected to the CPU pins by turning ON SW6 dip-switches: 7 and 9. SW6 switches 8 and 10 must be turned off. For more details please refer to schematic.

Table 6-6 shows the LCD pin allocation and CPU signal names used to handle the LCD.

LCD					
LCD Pin	LCD pin name / CPU port	CPU pin	LCD Pin	LCD pin name / CPU port	CPU pin
1	Ground	Ground	2	5V Only	
3	No Connection		4	DLCDRS / PA24	D2
5	R/W (Wired to Write only)	Pulled down to Ground	6	DLCDE + 100k pull down to ground / PB4	A3
7	No Connection		8	No connection	
9	No Connection		10	No connection	
11	DLCDD4 / PD0DLCD4	R3	12	DLCDD5 / PD2	P1
13	DLCDD6 / PD2DLCD6	P2	14	DLCDD7 / PD3	P3

Table 6-6 Debug LCD Module Connections

The Debug LCD module can only be used when A24 and DACK1 are not used.

6.7. Graphic Colour TFT LCD Module.

The RSK2+ board is equipped with a SSD1906R TFT LCD module controller and two headers for TFT LCD modules. The SSD1906R controller has 256K Embedded Display SRAM and can support colour and monochrome TFT displays. TFT modules can be inserted in the H_LCD connector (for the Hitachi LCD modules) or G_LCD connector (for other TFT modules). An adaptor board may be required for other TFT modules.

The TFT controller fitted can support driving panels up to 18 bits in colour depth. When using panels of 18 bit depth with 16 bit data it is necessary to connect Red0 and Blue0 to ground. To support these panels we have provided jumper J9 which will connect these signals to Logic 0 when fitted.

Connections are provided to support an alternate TFT LCD driver IC (Epson S1D13A04) these connections are not verified and information is provided for reference only. Customers may use this alternate device at their own risk.

By default the on-board backlight voltage generator (U24) is enabled and it is configured to drive a string of up to 6 series LEDs with a current of 16.2mA. If the User needs to dim a LCD backlight or disable it, R92 resistor may be fitted. For an appropriate value of the resistor please refer to datasheet of backlight voltage generator (MAX1599).

The connections for the TFT LCD Modules are listed in Table 6-7 and Table 6-8.

H_LCD (For Hitachi LCD)					
Pin	CPU board Signal Name	Device Pin	Pin	CPU board Signal Name	Device Pin
1	GROUND		2	GROUND	
3	GROUND		4	LCD_VCC	
5	LCD_VCC		6	LCD_VCC	
7	BLCD_DATA0		8	BLCD_DATA1	
9	BLCD_DATA2		10	BLCD_DATA3	
11	BLCD_DATA4		12	BLCD_DATA5	
13	BLCD_DATA6		14	BLCD_DATA7	
15	BLCD_DATA8		16	BLCD_DATA9	
17	BLCD_DATA10		18	BLCD_DATA11	
19	BLCD_DATA12		20	BLCD_DATA13	
21	BLCD_DATA14		22	BLCD_DATA15	
23	BLCD_DATA16		24	BLCD_DATA17	
25	BLCD_DOTCLK		26	BLCD_HSYNC	
27	BLCD_VSYNC		28	BSSCS	B4
29	BSSCK	V15	30	BSSO	V14
31	RXD1	W14	32	BLCD_RESn	W18
33	GROUND		34	VLED +	
35	VLED +		36	VLED -	
37	VLED -		38	GROUND	
39	GROUND				

Table 6-7 Hitachi LCD Module Connections

G_LCD (For Generic LCD)					
Pin	CPU board Signal Name	Device Pin	Pin	CPU board Signal Name	Device Pin
1	BOARD_5V		2	BOARD_5V	
3	LCD_VCC		4	LCD_VCC	
5	VLED+		6	VLED-	
7	BLCD_DATA1		8	BLCD_DATA2	
9	BLCD_DATA3		10	BLCD_DATA4	
11	BLCD_DATA5		12	BLCD_DATA6	
13	BLCD_DATA7		14	BLCD_DATA8	
15	BLCD_DATA9		16	BLCD_DATA10	
17	BLCD_DATA11		18	BLCD_DATA13	
19	BLCD_DATA14		20	BLCD_DATA15	
21	BLCD_DATA16		22	BLCD_DATA17	
23	BLCD_DON		24	BLCD_HSYNC	
25	BLCD_DOTCLK		26	BLCD_MDISP	
27	BLCD_VSYNC		28	BCLD_CLK (LCD CLK)	
29	BSSCK	V15	30	RXD1	W14
31	BSSO		32	BSSCS	B4
33	BLCD_RESn	W18	34	GROUND	
35	BLCD_VCPWC		36	BLCD_VEPWC	145
37	GROUND		38	GROUND	
39	GROUND		40	GROUND	

Table 6-8 Generic LCD Module Connections

6.8. Serial Sound Interface (SSI).

The RSK2+ board is equipped with Serial Sound Interface (SSI). The SSI is a module designed to send or receive an audio data stream with various devices. The 'SSI' header is accessible on the RSK2+ board. Please see the microcontroller hardware manual for more details.

J2					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	Board_5V		2	Board_VCC	
3	SSI_SCK1	W17	4	SSI_WS1	V12
5	SSI_DATA1	V13	6	AUDIOCLK	V16
7	GROUND				

Table 6-9 Serial sound interface Connections

6.9. Video Stream Interface

The RSK2+ board is equipped with Video Stream Interface header 'STI'. For details please refer to the SH/7670 hardware manual.

STI connector					
Pin	CPU board Signal Name	Device Pin	Pin	CPU board Signal Name	Device Pin
1	ST0_CLKIN	R19	2	ST_CLKOUT	Y17
3	ST0_D0	N20	4	ST0_D2	M18
5	ST0_D4	M20	6	ST0_D6	L19
7	NC		8	GROUND	
9	GROUND		10	NC	
11	ST0_D7	L20	12	ST0_D5	L18
13	ST0_D3	M19	14	ST0_D1	N18
15	ST0_SYC	N19	16	ST0_VLD	P20
17	ST0_PWM	P18	18	ST0_REQ	P19
19	ST0_VCO_CLKIN	R20	20	GROUND	

Table 6-10 Video stream interface connections

6.10. Option Links

Table 6-11 below describes the function of the option links contained on this RSK2+ board and associated with Serial Port Configuration. The default configuration is indicated by **BOLD** text.

Serial Port Option Link Settings				
Reference	Function	Fitted	Not fitted	Related To
R165	Serial Port configuration	Disables RS232 Serial Transceiver	Enables RS232 Serial Transceiver	
R169	Serial Port Configuration	Connects serial port SCIF2 (Rx) to serial receiver pin.	Disconnects serial port SCIF2 (Rx) from serial receiver pin.	R179, R180, R170
R170	Serial Port Configuration	Connects serial port SCIF2 (Rx) to JA6 pins.	Disconnects serial port SCIF2 (Rx) from JA6 pins.	R179, R180, R169
R180	Serial Port Configuration	Connects serial port SCIF2 (Tx) to serial transmitter pin.	Disconnects serial port SCIF2 (Tx) from serial transmitter pin.	R179, R169, R170
R179	Serial Port Configuration	Connects serial port SCIF2 (Tx) to JA6 pins.	Disconnects serial port SCIF2 (Tx) port from JA6 pins.	R169, R180, R170
R181	Serial Port Configuration	Connects serial port SCIF1 (Tx) to D-type connector secondary channel.	Disconnects port SCIF1 (Tx) from D-type connector secondary channel.	R186
R183	Serial Port Configuration	Connects serial port SCIF1 (Rx) to D-type connector secondary channel.	Disconnects port SCIF1 (Rx) from D-type connector secondary channel.	R187
R186	Serial Port Configuration	Connects serial port SCIF1 (Tx) to secondary serial transmitter pin.	Disconnects serial port SCIF1 (Tx) from secondary serial transmitter pin.	R181
R187	Serial Port Configuration	Connects serial port SCIF1 (Rx) to secondary serial receiver pin.	Disconnects serial port SCIF1 (Rx) from secondary serial receiver pin.	R183

Table 6-11 Serial port configuration links.

Table 6-12 below describes the function of the option links associated with power source. The default configuration is indicated by BOLD text.

Power Supply Option Link Settings				
Reference	Function	Fitted	Not fitted	Related To
5V_SEL_1	RSK2+ board power supply	Both jumper blocks are to be fitted to override the input regulator and allow an external 5V supply to power the board.	Both jumper blocks are to be removed to allow an external 7-12V supply to power the board.	R16, R22, 5V_SEL_2
5V_SEL_2	External power supply			R16, R22, 5V_SEL_1
R191	Power source	Normal operation	J1_2 provides the option to measure the current. *WARNING*	
R158	Power source	Normal operation	J3_3 provides the option to measure the current. *WARNING*	
R86	External power supply	Routes JA1-3 pin to on-board 3V3.	Disable 3V3 output to JA1-3 pin	R171,R172
R22	External power supply	Routes JA1-1 pin to on-board 5V.	Disable 5V output to JA1-1 pin	5V_SEL_1, 5V_SEL_2
R92	LCD backlight	Disables or dims TFT LCD backlight	Enables 16.2mA output for TFT LCD backlight	

Table 6-12 Power configuration links.

***WARNING:** All power connections with provision for current measurement must remain connected while the power is on or damage to the connected devices is highly likely.

Table 6-13 below describes the function of the option links associated with clock configuration. The default configuration is indicated by BOLD text.

Clock Option Link Settings				
Reference	Function	Fitted	Not fitted	Related To
R62	PHY clock source	Load resistor for a crystal	Not fitted	
R63	PHY clock source	Connects on-board oscillator for the PHY device	Can be replaced with damping resistor if required.	
R157	USB clock source	Load resistor for a crystal	Not fitted	
R146	USB clock source	On-board oscillator is used	External clock source is used	R144, R145, R147
R147	USB External clock source	External clock source is used	On-board Clock Source is used	R144, R145, R146
R144	USB clock source	On-board oscillator is used	External clock source is used	R146, R145, R147
R145	USB External clock source	External clock source is used	On-board Clock Source is used	R144, R146, R147
R137	CPU clock source	Load resistor for a crystal	Not fitted	
R139	CPU External clock source	External clock source is used	On-board Clock Source is used	R135, R136, R138
R138	CPU clock source	On-board oscillator is used	External clock source is used	R135, R136, R139
R136	CPU External clock source	External clock source is used	On-board Clock Source is used	R135, R139, R138
R135	CPU clock source	On-board oscillator is used	External clock source is used	R139, R136, R138

Table 6-13 Clock configuration links.

Table 6-14 below describes the function of the option links associated with USB. The default configuration is indicated by BOLD text.

Option Link Settings				
Reference	Function	Fitted	Not fitted	Related To
R184	USB Host connector shield	USB Host connector shield is grounded	USB Host connector shield is unconnected	-
R194	USB Device connector shield	USB Device connector shield is grounded	USB Device connector shield is unconnected	-

Table 6-14 USB links.

6.11.DIP Switch Settings

DIP Switch SW4	State	DIP Switch SW5	State	DIP Switch SW6	State	DIP Switch SW7	State
1	ON	1	OFF	1	OFF	1	OFF
2	OFF	2	ON	2	ON	2	ON
3	ON	3	OFF	3	OFF	3	ON
4	ON	4	ON	4	ON	4	OFF
5	ON	5	OFF	5	OFF	5	ON
6	ON	6	ON	6	ON	6	OFF
7	ON	7	OFF	7	ON	7	ON
8	ON	8	ON	8	OFF	8	OFF
9	OFF	9	OFF	9	ON	9	ON
10	OFF	10	ON	10	OFF	10	OFF

Table 6-15 Default DIP Switch Settings

Switch (SW4)			
ID	Function	Action On	Action Off
1	Selection of USB VBUS Flag	USB Host connector connected to VBUS	USB Host connector VBUS flag disconnected
2		USB Function connector connected to VBUS	USB Function connector VBUS flag disconnected
3	Select between USB Host and Function Connectors.	USB Host connector is selected.	USB Function connector is selected.
4	TFT Controller CF4	Little Endian bus interface	Big Endian bus interface
5	TFT Controller CF6	CF6 = 0 *See Table 6-17	CF6 = 1 *See table Table 6-17
6	TFT Controller CF7	CF7 = 0 *See Table 6-17	CF7 = 1 *See table Table 6-17
7	Chip Select 5 (Expansion Header) Selection 0	CS5_SEL0 = 0 *See Table 10-2	CS5_SEL0 = 1 * See Table 10-2
8	Chip Select 5 (Expansion Header) Selection 1	CS5_SEL1 = 0 *See Table 10-2	CS5_SEL1 = 1 * See Table 10-2
9	Flash Protection (Boot Flash)	Flash protection On	Flash Protection Off
10	Flash Protection (User Flash)	Flash Protection On	Flash Protection Off

Table 6-16 SW4 Functions

CF6	CF7	CLKI to BCLK Divide Ratio
0	0	1:1
0	1	2:1
1	0	3:1
1	1	4:1

Table 6-17 SW4-5+6 Function

Switch (SW5)			
ID	Function	Action On	Action Off
1	Multiplexed Pin: ST0D0 and IO0	ST0_D0 Connected	ST0_D0 Disconnected
2		IO0 Connected	IO0 Disconnected
3	Multiplexed Pin: ST0D1 and IO1	ST0_D1 Connected	ST0_D1 Disconnected
4		IO1 Connected	IO1 Disconnected
5	Multiplexed Pin: ST0D2 and IO2	ST0_D2 Connected	ST0_D2 Disconnected
6		IO2 Connected	IO2 Disconnected
7	Multiplexed Pin: ST0D3 and IO3	ST0_D3 Connected	ST0_D3 Disconnected
8		IO3 Connected	IO3 Disconnected
9	Multiplexed Pin: ST0D4 and IO4	ST0_D4 Connected	ST0_D4 Disconnected
10		IO4 Connected	IO4 Disconnected

Table 6-18 SW5 Functions

Switch (SW6)			
ID	Function	Action On	Action Off
1	Multiplexed Pin: ST0_D5 and IO5	ST0_D5 Connected	ST0_D5 Disconnected
2		IO5 Connected	IO5 Disconnected
3	Multiplexed Pin: ST0_D6 and IO6	ST0_D6 Connected	ST0_D6 Disconnected
4		IO6 Connected	IO6 Disconnected
5	Multiplexed Pin: ST0_D7 and IO7	ST0_D7 Connected	ST0_D7 Disconnected
6		IO7 Connected	IO7 Disconnected
7	Multiplexed Pin: DLCDE and DACK1	DLCDE Connected	DLCDE Disconnected
8		DACK1 Connected	DACK1 Disconnected
9	Multiplexed Pin: DLCDRS and A24	DLCDRS Connected	DLCDRS Disconnected
10		A24 Connected	A24 Disconnected

Table 6-19 SW6 Functions

Switch (SW7)			
ID	Function	Action On	Action Off
1	Multiplexed Pin HIFMD and A25. HIFMD is sampled at reset and determines if this is a host or slave device. If both switches are off operation is not guaranteed.	Pulled high	Disconnected
2		Pulled Low	Disconnected
3	Selection of CS5C	CS5C is connected to signal CS5Cn_CS5Dn on JA3	CS5C is not connected to signal CS5Cn_CS5Dn on JA3
4	Selection of CS5D	CS5C is connected to signal CS5Cn_CS5Dn on JA3	CS5C is not connected to signal CS5Cn_CS5Dn on JA3
5	Multiplexed Pin: WAITn and SDA	WAITn Connected	WAITn Disconnected
6		SDA Connected	SDA Disconnected
7	Multiplexed Pin: CS5n and TEND1	CS5n Connected	CS5n Disconnected
8		TEND1 Connected	TEND1 Disconnected
9	Multiplexed Pin: CS6n and DREQ1	CS6n Connected	CD6n Disconnected
10		DREQ1 Connected	DREQ1 Disconnected

Table 6-20 SW7 Functions

6.12. Oscillator Sources

Crystal oscillators are fitted on the RSK2+ and used to supply the main clock input to the Renesas microcontroller. Please see the table below for details of the oscillators that are fitted and alternative footprints provided on this RSK2+:

Component	
Crystal (X1), Main clock.	25 MHz
Crystal (X2), USB module.	48 MHz
Crystal (X3), Ethernet module.	25 MHz

Table 6-21 Oscillators / Resonators

6.13. Reset Circuit

The CPU Board includes μ P Supervisory Circuit with Manual Reset ability. The reset timeout period is set as 15 ms.

Please check the reset requirements carefully to ensure the reset circuit on the user's board meets all the reset timing requirements.

Chapter 7. Modes

This CPU incorporates a host interface (HIF) for use in high-speed transfer of data between external devices which cannot utilize the system bus. The HIF allows external devices to read from and write to 4 Kbytes (2 Kbytes x 2 banks) of the on-chip RAM exclusively for HIF use (HIFRAM) within this CPU, in 32-bit units.

Using HIFRAM, the HIF also supports HIF boot mode allowing this CPU to be booted. In HIF boot mode, this CPU can be booted from HIFRAM by an external device storing the instruction code in HIFRAM. The HIF's 'HOST Interface' header is accessible on the RSK2+ board.

For the details please refer to the SH/7670 Group Hardware Manual.

Chapter 8. Programming Methods

The RSK2+SH7670 board can be programmed using E10A-FSK supplied with the kit. Following header is provided to download and debug the user code – H-UDI.

8.1. H-UDI Header for E10A

This is a 14 pin header used to download and debug the user program. This header provides H-UDI interface for user debugging. Limited Event conditions in ROM and unlimited Breakpoints in RAM are supported. The AUD trace function is not supported on this interface.

Chapter 9. Headers

9.1. Microcontroller Headers

Table 9-1 to Table 9-8 show the microcontroller pin headers and their corresponding microcontroller connections. The header pins connect directly to the microcontroller pin unless otherwise stated.

J1					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	A(17)	A1	2	A(19)	B1
3	A(0)	A2	4	A(18)	B2
5	DLCDE_DACK1	A3	6	CS5n_TEND1	B3
7	WAITn_SDA	A4	8	IOCS	B4
9	CS4n	A5	10	RDn	B5
11	DQM1	A6	12	BSn	B6
13	D(9)	A7	14	D(8)	B7
15	D(12)	A8	16	D(10)	B8
17	D(15)	A9	18	D(14)	B9
19	D(5)	A10	20	D(6)	B10
21	D(2)	A11	22	D(3)	B11
23	A(16)	A12	24	D(0)	B12
25	A(13)	A13	26	A(14)	B13
27	A(10)	A14	28	A(11)	B14
29	A(7)	A15	30	A(8)	B15
31	A(4)	A16	32	A(5)	B16
33	A(1)	A17	34	A(2)	B17
35	SDRASn	A18	36	CS3n	B18
37	SDCASn	A19	38	GROUND	B19
39	GROUND	A20	40	SDCKE	B20

Table 9-1: J1

J2					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	A(22)	C1	2	HIFMD_A25	D1
3	A(21)	C2	4	DLCDRS_A24	D2
5	A(20)	C3	6	A(23)	D3
7	CS6n_DREQ1	C4	8	GROUND	D4
9	SCL	C5	10	GROUND	D5
11	CS0n	C6	12	UC_VCCQ	D6
13	DQM0	C7	14	UC_VCC	D7
15	D(11)	C8	16	GROUND	D8
17	D(13)	C9	18	UC_VCCQ	D9
19	D(7)	C10	20	UC_VCCQ	D10
21	D(4)	C11	22	GROUND	D11
23	D(1)	C12	24	GROUND	D12
25	A(15)	C13	26	UC_VCC	D13
27	A(12)	C14	28	GROUND	D14
29	A(9)	C15	30	UC_VCCQ	D15
31	A(6)	C16	32	GROUND	D16
33	A(3)	C17	34	GROUND	D17
35	GROUND	C18	36	DQM3	D18
37	WE _n	C19	38	DQM2	D19
39	CKIO	C20	40	D(25)	D20

Table 9-2: J2

J3					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	LNKSTA	E1	2	PIN_E2	E2
3	TX-CLK	F1	4	MDIO	F2
5	MII_TXD3	G1	6	TX-ER	G2
7	MII_TXD0	H1	8	MII_TXD1	H2
9	RX-CLK	J1	10	COL	J2
11	MII_RXD3	K1	12	RX-DV	K2
13	MII_RXD0	L1	14	MII_RXD1	L2
15	NC	-	16	ASEMDn	M2
17	IRQ4n	N1	18	IRQ5n	N2
19	DLCD5	P1	20	DLCD6	P2
21	HIF_D14	R1	22	HIF_D15	R2
23	HIF_D11	T1	24	HIF_D12	T2

Table 9-3: J3

J4					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	PIN_E3	E3	2	GROUND	E4
3	MDC	F3	4	UC_VCCQ	F4
5	TX-EN	G3	6	GROUND	G4
7	MII_TXD2	H3	8	UC_VCC	H4
9	CRS	J3	10	GROUND	J4
11	RX-ER	K3	12	UC_VCCQ	K4
13	MII_RXD2	L3	14	UC_VCCQ	L4
15	IRQ7n	M3	16	GROUND	M4
17	IRQ6n	N3	18	GROUND	N4
19	DLCD7	P3	20	UC_VCC	P4
21	DLCD4	R3	22	UC_VCC	R4
23	HIF_D13	T3	24	GROUND	T4

Table 9-4: J4

J5					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	GROUND	E17	2	D(24)	E18
3	UC_VCCQ	F17	4	D(27)	F18
5	UC_VCCQ	G17	6	D(31)	G18
7	UC_VCCQ	H17	8	UC_VCCQ	H18
9	GROUND	J17	10	GROUND	J18
11	UC_VCC	K17	12	GROUND	K18
13	GROUND	L17	14	ST0D5_IO5	L18
15	GROUND	M17	16	ST0D2_IO2	M18
17	UC_VCCQ	N17	18	ST0D1_IO1	N18
19	GROUND	P17	20	ST0_PWM	P18
21	UC_VCC	R17	22	WDTOVFn	R18
23	GROUND	T17	24	GROUND	T18

Table 9-5: J5

J6					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	D(26)	E19	2	D(28)	E20
3	D(29)	F19	4	D(30)	F20
5	D(23)	G19	6	D(22)	G20
7	D(21)	H19	8	D(20)	H20
9	D(19)	J19	10	D(18)	J20
11	D(17)	K19	12	D(16)	K20
13	ST0D6_IO6	L19	14	ST0D7_IO7	L20
15	ST0D3_IO3	M19	16	ST0D4_IO4	M20
17	ST0_SYC	N19	18	ST0D0_IO0	N20
19	ST0_REQ	P19	20	ST0_VLD	P20
21	ST0_CLKIN	R19	22	ST0_VCO_CLKIN	R20
23	MD_BW	T19	24	ASEBRKn	T20

Table 9-6: J6

J7					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	HIF_D9	U1	2	HIF_D7	V1
3	HIF_D10	U2	4	GROUND	V2
5	GROUND	U3	6	HIF_D4	V3
7	GROUND	U4	8	HIF_D1	V4
9	GROUND	U5	10	HIF_RS	V5
11	UC_VCCQ	U6	12	HIF_RDY	V6
13	GROUND	U7	14	GROUND	V7
15	GROUND	U8	16	GROUND	V8
17	DV12	U9	18	GROUND	V9
19	UV12	U10	20	GROUND	V10
21	AV12	U11	22	AGND	V11
23	UC_VCC	U12	24	SSI_WS1	V12
25	GROUND	U13	26	SSI_DATA1	V13
27	UC_VCCQ	U14	28	TXD1	V14
29	UC_VCCQ	U15	30	SCK1	V15
31	GROUND	U16	32	AUDIOCLK	V16
33	GROUND	U17	34	TCK	V17
35	MD_CLK1	U18	36	TDI	V18
37	NMI	U19	38	MD_CLK0	V19
39	NC	-	40	CON_EXTAL	V20

Table 9-7: J7

J8					
Pin	Circuit Net Name	Device Pin	Pin	Circuit Net Name	Device Pin
1	GROUND	W1	2	HIF_D8	Y1
3	HIF_D6	W2	4	HIF_D5	Y2
5	HIF_D3	W3	6	HIF_D2	Y3
7	HIF_D0	W4	8	HIF_CS _n	Y4
9	HIF_WR _n	W5	10	HIF_RD _n	Y5
11	HIF_DREQ	W6	12	HIF_INT _n	Y6
13	HIF_EBL	W7	14	DV33	Y7
15	GROUND	W8	16	NC (USB D-)	
17	VBUS_IN	W9	18	NC (USB D+)	
19	AGND	V11	20	AV33	Y10
21	GROUND	W11	22	NC	
23	CON_USB_X1	W12	24	CON_USB_X2	Y12
25	LED1	W13	26	LED0	Y13
27	RXD1	W14	28	SCK2	Y14
29	LED2	W15	30	RXD2	Y15
31	LED3	W16	32	TXD2	Y16
33	SSI_SCK1	W17	34	ST_CLKOUT	Y17
35	RES _n	W18	36	TRST _n	Y18
37	TDO	W19	38	TMS	Y19
39	CON_XTAL	W20	40	NC	

Table 9-8: J8

9.2. Application Headers

Table 9-9 and Table 9-13 below show the standard application header connections.

JA1							
Pin	Generic Header Name	CPU board Signal Name	Device Pin	Pin	Generic Header Name	CPU board Signal Name	Device Pin
1	5V	CON_5V		2	0V	GROUND	
3	3V3	CON_3V3		4	0V	GROUND	
5	AVcc	NC		6	AVss	CON_AVSS	
7	AVref	NC		8	ADTRG	NC	
9	AD0	NC		10	AD1	NC	
11	AD2	NC		12	AD3	NC	
13	DAC0	NC		14	DAC1	NC	
15	IO_0	IO_0	N20	16	IO_1	IO_1	N18
17	IO_2	IO_2	M18	18	IO_3	IO_3	M19
19	IO_4	IO_4	M20	20	IO_5	IO_5	L18
21	IO_6	IO_6	L19	22	IO_7	IO_7	L20
23	IRQ3	IRQ7n	M3	24	IIC_EX	NC	
25	IIC_SDA	SDA	A4	26	IIC_SCL	SCL	C5

* Shared pins. Please refer to schematic.

Table 9-9: JA1 Standard Generic Header

JA2							
Pin	Generic Header Name	CPU board Signal Name	Device Pin	Pin	Generic Header Name	CPU board Signal Name	Device Pin
1	RESn	RESn	W18	2	EXTAL	CON_EXTAL	V20**
3	NMIIn	NMI	U19	4	Vss1	GROUND	
5	WDT_OVF	WDTOVFn	R18	6	SClaTX	TxD1	V14
7	IRQ0	IRQ4n	R3*	8	SClaRX	RxD1	W14
9	IRQ1	IRQ5n	P1*	10	SClaCK	SCK1	V15
11	UD	NC		12	CTSRTS	NC	
13	Up	NC		14	Un	NC	
15	Vp	NC		16	Vn	NC	
17	Wp	NC		18	Wn	NC	
19	TMR0	NC		20	TMR1	NC	
21	TRIGa	NC		22	TRIGb	NC	
23	IRQ2	IRQ6n	P2*	24	TRISTn	NC	
25	-	NC		26	-	NC	

* Shared pins. Please refer to schematic.

** Option link.

Table 9-10: JA2 Standard Generic Header

JA5							
Pin	Generic Header Name	CPU board Signal Name	Device Pin	Pin	Generic Header Name	CPU board Signal Name	Device Pin
1	AD4	NC		2	AD5	NC	
3	AD6	NC		4	AD7	NC	
5	CAN1TX	NC		6	CAN1RX	NC	
7	CAN2TX	NC		8	CAN2RX	NC	
9	AD8	NC		10	AD9	NC	
11	AD10	NC		12	AD11	NC	
13	TIOC0A	NC		14	TICO0B	NC	
15	TIOC0C	NC		16	M2_TRISTn	NC	
17	TCLKC	NC		18	TCLKD	NC	
19	M2_Up	NC		20	M2_UN	NC	
21	M2_Vp	NC		22	M2_Vn	NC	
23	M2_Wp	NC		24	M2_Wn	NC	

Table 9-11: JA5 Standard Generic Header

JA6							
Pin	Generic Header Name	CPU board Signal Name	Device Pin	Pin	Generic Header Name	CPU board Signal Name	Device Pin
1	DREQ	DREQ1	C4*	2	DACK	DACK1	A3
3	TEND	TEND1	B3*	4	STBYn	NC	
5	RS232TX	RS232TX	**	6	RS232RX	RS232RX	**
7	SClBRX	RxD2	Y15	8	SClBTX	TXD2	Y16
9	SClCTX	NC		10	SClBCK	SCK2	Y14
11	SClCCK	NC		12	SClCRX	NC	
13	Reserved	NC		14	Reserved	NC	
15	Reserved	NC		16	Reserved	NC	
17	Reserved	NC		18	Reserved	NC	
19	Reserved	NC		20	Reserved	NC	
21	Reserved	NC		22	Reserved	NC	
23	Reserved	NC		24	Reserved	NC	

* Shared pins. Please refer to schematic.

** Option link.

Table 9-12: JA6 Standard Generic Header

JA3							
Pin	Generic Header Name	CPU board Signal Name	Device Pin	Pin	Generic Header Name	CPU board Signal Name	Device Pin
1	A0	BXA(0)	*	2	A1	BXA(1)	*
3	A2	BXA(2)	*	4	A3	BXA(3)	*
5	A4	BXA(4)	*	6	A5	BXA(5)	*
7	A6	BXA(6)	*	8	A7	BXA(7)	*
9	A8	BXA(8)	*	10	A9	BXA(9)	*
11	A10	BXA(10)	*	12	A11	BXA(11)	*
13	A12	BXA(12)	*	14	A13	BXA(13)	*
15	A14	BXA(14)	*	16	A15	BXA(15)	*
17	D0	BXD(0)	*	18	D1	BXD(1)	*
19	D2	BXD(2)	*	20	D3	BXD(3)	*
21	D4	BXD(4)	*	22	D5	BXD(5)	*
23	D6	BXD(6)	*	24	D7	BXD(7)	*
25	RDn	BXRDn	*	26	WR	BXWRn	*
27	CS0n	CS5An	*	28	CS1n	CS5Bn	*
29	D8	BXD(8)	*	30	D9	BXD(9)	*
31	D10	BXD(10)	*	32	D11	BXD(11)	*
33	D12	BXD(12)	*	34	D13	BXD(13)	*
35	D14	BXD(14)	*	36	D15	BXD(15)	*
37	A16	BXA(16)	*	38	A17	BXA(17)	*
39	A18	BXA(18)	*	40	A19	BXA(19)	*
41	A20	BXA(20)	*	42	A21	BXA(21)	*
43	A22	BXA(22)	*	44	SDCLK	BXCKIO	*
45	CS2n	CS5Cn_CS5Dn	*	46	ALE	BXBSn	*
47	WRHn	BXWR1n	*	48	WRLn	BXWR0n	*
49	-	NC	-	50	-	NC	-

* Buffered input/output signals.

Table 9-13: JA3 Standard Generic Header

Chapter 10. Code Development

10.1. Overview

Note: For all code debugging using Renesas software tools, the RSK2+ board must be connected to a PC USB port via an E10A. An E10A FSK is supplied with the RSK2+ product.

10.2. Compiler Restrictions

The compiler supplied with this RSK2+ is fully functional for a period of 60 days from first use. After the first 60 days of use have expired, the compiler will default to a maximum of 256k code and data. To use the compiler with programs greater than this size you need to purchase the full tools from your distributor.

Warning: The protection software for the compiler will detect changes to the system clock. Changes to the system clock back in time may cause the trial period to expire prematurely.

10.3. Breakpoint Support

The support of breakpoints is limited. Breakpoints may be enabled for RAM memory only. Instead of using breakpoints the User should use 'Eventpoints'.

'Eventpoints' are available for the both RAM and ROM memories. Up to 11 'Eventpoints' can be set into the user source code.

Double clicking in the 'Event' column in the code sets the 'Eventpoint'. 'Eventpoints' will remain unless they are double clicked to remove them.

10.4. Memory Map

In the architecture, this CPU has a 32-bit address space, which is divided into cache-enabled, cache-disabled, and on-chip spaces (on-chip RAM, on-chip peripheral modules, and reserved areas) according to the upper bits of the address.

Table 10-1 below shows the global memory map.

Internal Address Range	Description	Addressed Device	Cache Area
0x00000000 to 0x03FFFFFF	CS0 - Normal space containing 4MB Flash as 2Mx16bits	Boot Flash	Cache-enabled
0x04000000 to 0x07FFFFFF	Reserved area	Reserved	
0x08000000 to 0x0BFFFFFF	Reserved area	Reserved	
0x0C000000 to 0x01FFFFFF	CS3 - 32MB SDRAM organised as 8Mx32bits	SDRAM	
0x02000000 to 0x0FFFFFFF	Reserved area	Reserved	
0x10000000 to 0x107FFFFFFF	CS4 - Normal space containing 8MB Flash as 2Mx32bits	User Flash	
0x10800000 to 0x13FFFFFF	Reserved area	Reserved	
0x14000000 to 0x17FFFFFF	CS5 Normal space, See Table 10-2	External Interface	
0x18000000 to 0x1BFFFFFF	CS6 Normal space, See TFT controller data sheet	TFT Controller	
0x1C000000 to 0x1FFFFFFF	Other Reserved area	Reserved	
0x20000000 to 0x23FFFFFF	CS0 - Normal space containing 4MB Flash as 2Mx16bits	Boot Flash	Cache-disabled
0x24000000 to 0x27FFFFFF	Reserved area	Reserved	
0x28000000 to 0x2BFFFFFF	Reserved area	Reserved	
0x2C000000 to 0x21FFFFFF	CS3 - 32MB SDRAM organised as 8Mx32bits	SDRAM	
0x22000000 to 0x2FFFFFFF	Reserved area	Reserved	
0x30000000 to 0x307FFFFFFF	CS4 - Normal space containing 8MB Flash as 2Mx32bits	User Flash	
0x30800000 to 0x33FFFFFF	Reserved area	Reserved	
0x34000000 to 0x37FFFFFF	CS5 Normal space, See	External Interface	
0x38000000 to 0x3BFFFFFF	CS6 Normal space, See TFT controller data sheet	TFT Controller	
0x3C000000 to 0x3FFFFFFF	Other Reserved area	Reserved	

Table 10-1 Memory Map

Further information on internal memory can be found in the device hardware manual.

10.5.CPLD

The CPLD has 4 functions:

- Generate BUSCLK / 2 for TFT (50MHz).
- Synchronise the TFT controller accesses to the CPU clock.
- External buffer activation control.
- Split CS5 area into 4 for additional CS support on interfaces.

10.5.1. Local TFT Bus Clock

The TFT bus clock is generated in the CPLD by a simple divider function that is provided to the TFT controller and used internally to re-time the bus accesses.

10.5.2.Synchronise local TFT bus to CPU bus clock.

This is implemented as two state machines.

- The CPLD monitors the Bus Start (BSn) and Chip Select (CS6n) signals of the CPU. On detection it activated the TFT BS and CS signals.
- The CPLD monitors the Bus Start (BSn) and Chip Select (CS6n) and Read or Write signals of the CPU.

On activation the CPU wait line is held low to hold the CPU bus cycle while the TFT cycle is in progress.

CPU Read and Write signals are used to time the TFT signals now synchronised to the TFT clock

A delay (2 TFT cycles) is added to the read and write sequences to meet TFT controller timing requirements.

10.5.3.External buffer activation control.

The external buffers are active if either CS0 (FLASH), CS4(FLASH) or CS6(TFT) are not active.

10.5.4. Chip Select 5 Area allocation

Area 5 is split into four areas the size of each can be specified by the user by making a selection on the configuration switches SW4-7 and SW4-8. The area allocation is shown in Table 10-2. The option to provide three different CS size areas is required as the upper two address lines (A24 & A25) are shared with CPU functions (HIF MODE and DLCDRS). When Host interface mode or the on board LCD module are used then only the smaller area allocations should be used.

CS5 SEL 1	CS5 SEL 0	CS5_A Low	CS5_A High	CS5_B Low	CS5_B High	CS5_C Low	CS5_C High	CS5_D Low	CS5_D High	Note
0	0	14000000	143FFFFFF	14400000	147FFFFFF	14800000	14BFFFFFF	14C00000	14FFFFFF	No Cache 4Mbytes
0	0	34000000	343FFFFFF	34400000	347FFFFFF	34800000	34BFFFFFF	34C00000	34FFFFFF	Cached 4MBytes
0	1	14000000	147FFFFFF	14800000	14FFFFFF	15000000	157FFFFFF	15800000	15FFFFFF	No Cache 8Mbytes
0	1	34000000	347FFFFFF	34800000	34FFFFFF	35000000	357FFFFFF	35800000	35FFFFFF	Cached 8Mbytes
1	0	14000000	14FFFFFF	15000000	15FFFFFF	16000000	16FFFFFF	17000000	17FFFFFF	No Cache 16Mbytes
1	0	34000000	34FFFFFF	35000000	35FFFFFF	36000000	36FFFFFF	37000000	17FFFFFF	Cached 16MBytes
1	1	14000000	17FFFFFF	Inactive	Inactive	Inactive	Inactive	Inactive	Inactive	No Cache 32MBytes
1	1	34000000	37FFFFFF	Inactive	Inactive	Inactive	Inactive	Inactive	Inactive	Cached 32MBytes

Table 10-2 Chip Select Memory Mapping

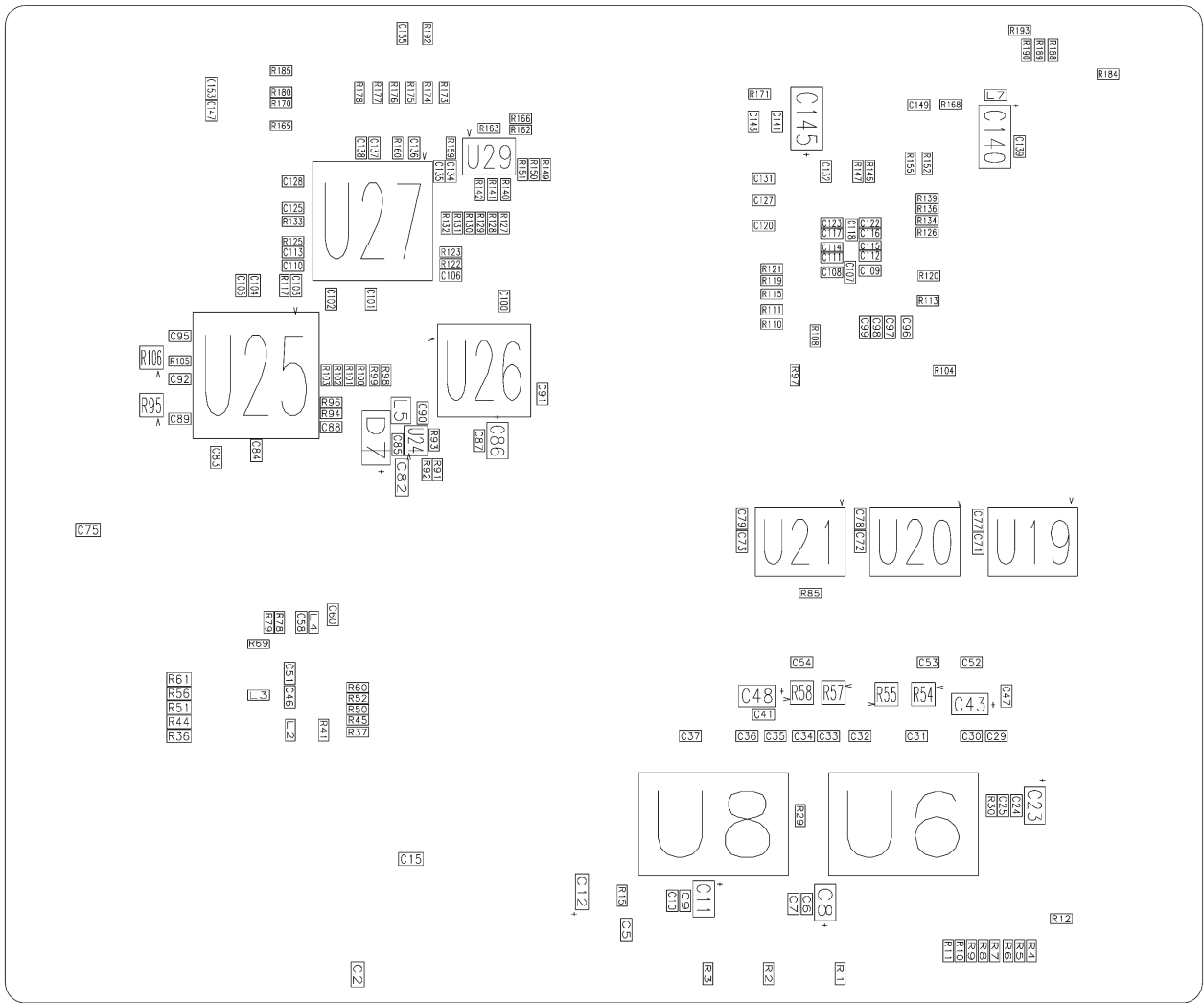


Figure 11-2: Component Placement – Bottom view

Chapter 12. CPLD Code Reference

The following VHDL code is the source for the CPLD fitted on this product.

This code is provided for reference only and no warranty expressed or implied is accepted for the re-use of this code.

12.1.CPLD Device Pinout

Device Part Number: (Xilinx) XC9536XL-10-VQ44

```

-----
/44 43 42 41 40 39 38 37 36 35 34 \
| 1                               33 |
| 2                               32 |
| 3                               31 |
| 4                               30 |
| 5          XC9536XL-10-VQ44      29 |
| 6                               28 |
| 7                               27 |
| 8                               26 |
| 9                               25 |
| 10                              24 |
| 11                              23 |
\ 12 13 14 15 16 17 18 19 20 21 22 /

```

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	KPR	12	CPU_WEn	23	CPU_BSn	34	CPU_CS0n
2	CPU_CS5Cn	13	TFT_WAIT	24	TDO	35	VCC
3	CPU_CS5n	14	TFT_CSn	25	GND	36	CPU_CS4n
4	GND	15	VCC	26	VCC	37	TFT_WE0n
5	CPU_CS5Dn	16	CPU_CSBn	27	CPU_ADDR<24>	38	TFT_READ
6	CPU_ADDR<23>	17	GND	28	CPU_WAITn	39	KPR
7	CPU_ADDR<25>	18	CPU_CS5An	29	CS5_SEL<1>	40	CPU_WE1n
8	TFT_BS	19	TFT_WRITE	30	CS5_SEL<0>	41	CPU_CS5Bn
9	TDI	20	CPU_WE0n	31	CPU_ADDR<22>	42	CPU_RDn
10	TMS	21	TFT_CLK	32	TFT_WE1n	43	CPU_CKIO
11	TCK	22	CPU_CS6n	33	SYS_RESEn	44	KPR

Table 12-1 CPLD Connection Table

Legend :

KPR = Unused I/O with weak keeper (leave unconnected)

VCC = Dedicated Power Pin

GND = Dedicated Ground Pin

CPLD VHDL Code

```
--*****  
--FILE NAME      lcl_bus_if_sync.vhd  
--DESCRIPTION    Synchronise slower speed TFT controller to high speed external bus.  
--              Control for splitting Chip Select Area 5.  
-- Copyright    : 2008 Renesas Technology Europe Ltd.  
-- Copyright    : 2008 Renesas Technology Corporation.  
-- All Rights Reserved  
-- *****  
-- Revision History  
-- DD.MM.YYYY OSO-UID Description  
-- 14.10.2008 RTE-MAB First Release.  
-- *****  
library IEEE;  
use IEEE.std_logic_1164.all;  
use IEEE.numeric_std.all;  
use IEEE.std_logic_unsigned.all;
```

```

entity LCL_TFT_IF is
port (
  -- System
  SYS_RESETEn      : in  std_logic;-- System Reset
  CS5_SEL          : in  std_logic_vector (1 downto 0);

  -- System Bus
  CPU_CKIO        : in std_logic;   -- uP Bus Clock
  CPU_ADDR        : in std_logic_vector(25 downto 22);  -- uP Address bus
  CPU_CS0n        : in std_logic;   -- Control the Buffered data bus (Boot Flash)
  CPU_CS4n        : in std_logic;   -- Control the Buffered data bus (Upper Flash)
  CPU_CS5n        : in std_logic;   -- uP to External Chip Select
  CPU_CS6n        : in std_logic;   -- uP to TFT Chip Select
  CPU_BSn         : in std_logic;   -- uP Bus Strobe
  CPU_RDn         : in std_logic;   -- uP Read
  CPU_WEn         : in std_logic;   -- uP Write
  CPU_WE0n        : in std_logic;   -- uP Write0
  CPU_WE1n        : in std_logic;   -- uP Write1
  CPU_WAITn       : out  std_logic;-- uP Wait

  CPU_CS5An       : out  std_logic;-- uP to External Chip Select
  CPU_CS5Bn       : out  std_logic;-- uP to External Chip Select
  CPU_CS5Cn       : out  std_logic;-- uP to External Chip Select
  CPU_CS5Dn       : out  std_logic;-- uP to External Chip Select
  CPU_CSBn        : out  std_logic;-- Control the Buffered bus (Buffer Control)

  -- LOCAL BUS (Slow TFT)
  TFT_CLK         : out  std_logic;-- TFT Slower Bus Clock
  TFT_CSn         : out  std_logic;-- TFT CS signal (synch with BS)
  TFT_READ        : out  std_logic;-- Read Strobe
  TFT_WRITE       : out  std_logic;-- Write Strobe
  TFT_BS          : out  std_logic;-- TFT Bus Strobe
  TFT_WE0n        : out  std_logic;-- TFT Bus Lower Byte Write
  TFT_WE1n        : out  std_logic;-- TFT Bus Upper Byte Write
  TFT_WAIT        : in  std_logic -- TFT Bus Wait
);

end LCL_TFT_IF;

```

architecture LCL_TFT_IF_arch of LCL_TFT_IF is

-- Internal State Machine Definitions

type type_state is (s_idle, s_read, s_write, s_end);

type type_bs_smc is (s_idle, s_low, s_high, s_wait);

-- Internal signal definitions

signal cpu_state : type_state; -- Follow CPU bus state

signal tft_state : type_state; -- Generated TFT bus state

signal bs_state : type_bs_smc; -- Generated TFT Bus Start signal state

signal tft_read_int : std_logic;

signal tft_write_int : std_logic;

signal tft_wait_int : std_logic;

signal cpu_ready : std_logic;

signal tft_clk_int : std_logic;

signal cpu_ckio_int : std_logic;

signal tft_we0_int : std_logic;

signal tft_we1_int : std_logic;

signal cpu_cs5n_int : std_logic;

signal tft_bs_int : std_logic;

signal cpu_bs_int : std_logic;

signal tft_cs_int : std_logic;

signal tft_delay : std_logic_vector(1 downto 0);

signal cs_bn_int : std_logic;

```

-- Begin Functional Description
begin
-- Internal signal sources
cpu_ckio_int  <= CPU_CKIO;
tft_wait_int  <= TFT_WAIT;
cpu_cs5n_int  <= CPU_CS5n;
-- Internal signal outputs
CPU_CSBn      <= cs_bn_int;
CPU_WAITn     <= cpu_ready;
TFT_CLK       <= tft_clk_int;
TFT_READ      <= tft_read_int;
TFT_WRITE     <= tft_write_int;
TFT_WE0n      <= tft_we0_int;
TFT_WE1n      <= tft_we1_int;
TFT_BS        <= tft_bs_int;
TFT_CSn       <= tft_cs_int;

-- External buffered bus asynchronous control
cs_bn_int     <= '0' when (CPU_CS0n='0' xor CPU_CS4n='0' xor CPU_CS6n='0') else '1';

-- Generate the TFT clock from the CPU clock
process(CPU_CKIO,cpu_ckio_int)
begin
    if rising_edge(CPU_CKIO) then
        if (tft_clk_int = '1') then
            tft_clk_int <= '0';
        else
            tft_clk_int <= '1';
        end if;
    end if;
end process;

```

```

-- Control TFT Read and Write Cycles
process(SYS_RESETEn, cpu_ckio_int)
begin
    if (SYS_RESETEn='0') then
        cpu_state      <= s_idle;
        cpu_ready <= '1';
        cpu_bs_int     <= '1';
    elsif (CPU_CS6n='0'and CPU_BSn='0') then
        cpu_bs_int <= '0'; -- Trigger the TFT process
        cpu_ready <= '0'; -- Hold the CPU
        cpu_state <= s_idle;
    elsif falling_edge(cpu_ckio_int) then
        case cpu_state is
            when s_idle      => -- Check for new bus cycle and select type
                if (cpu_bs_int = '0') then
                    if (CPU_WEn/= '1' ) then
                        cpu_state <= s_write;
                    else
                        cpu_state <= s_read;
                    end if;
                else
                    -- Release CPU_Wait when inactive
                    cpu_bs_int <= '1';
                    cpu_ready <= 'Z';
                end if;
            when s_read      => -- In Read Bus Cycle - wait for TFT controller
                cpu_bs_int <= '0';
                if (TFT_state=s_end) then
                    cpu_ready <= 'Z';
                    if (CPU_RDn='1') then
                        cpu_state <= s_end;
                    end if;
                end if;
            when s_write => -- In Write Bus Cycle - wait for TFT controller
                cpu_bs_int <= '0';
                if (TFT_state=s_end) then
                    cpu_ready <= 'Z';
                    if (CPU_WEn='1') then
                        cpu_state <= s_end;
                    end if;
                end if;
        end case;
    end if;
end process;

```

```
end if;
when s_end => -- Clean up after cycle - wait for TFT idle.
    cpu_bs_int <= '1';
    cpu_ready <= 'Z';
    if (TFT_state=s_idle) then
        cpu_state <= s_idle;
    end if;
end case;
end if;
end process;
```

```

-- Generate TFT Bus Strobe and Chip Select
process(SYS_RESETEn, tft_clk_int, CPU_BS6n)
begin
    if (SYS_RESETEn='0') then
        tft_cs_int <= '1';
        tft_bs_int <= '1';
        bs_state <= s_idle;
    else
        if (rising_edge(tft_clk_int)) then
            case bs_state is
                when s_idle => -- When a bus strobe is active - start the TFT cycle
                    if ( cpu_bs_int = '0' and CPU_CS6n = '0' )then
                        tft_bs_int <= '0';
                        tft_cs_int <='0';
                        bs_state <= s_low;
                    else
                        tft_bs_int <= '1';
                        tft_cs_int <='1';
                        bs_state <= s_idle;
                    end if;
                when s_low => -- Bus strobe was detected and generated.
                    -- So raise TFT bus strobe one clock later.
                        tft_cs_int <='0';
                        tft_bs_int <= '1';
                        bs_state <= s_high;
                when s_high => -- Waiting to be able to release TFT_CS
                    tft_bs_int <= '1';
                    -- Check for end of the CPU bus cycle.
                    if (cpu_state = s_end ) then
                        bs_state <= s_wait;
                    else
                        bs_state <= s_high;
                    end if;
                when s_wait => -- Wait for CS6 to have gone high
                    if (CPU_CS6n = '1' ) then
                        tft_cs_int <='1';
                        bs_state <= s_idle;
                    else
                        tft_cs_int <='0';
                        bs_state <= s_wait;
                    end if;
            end case;
        end if;
    end if;
end process;

```

```
end if;
    when others =>
        tft_cs_int <='1';
        tft_bs_int <= '1';
        bs_state <= s_idle;
    end case;
end if;
end if;
end process;
```

```

-- Re-Sync CPU signals to internal bus clock
process(SYS_RESETEn, tft_clk_int)
begin
    if (SYS_RESETEn='0') then
        tft_state <= s_idle;
        tft_read_int <= '1';
        tft_write_int <= '1';
        tft_we0_int <= '1';
        tft_we1_int <= '1';
        tft_delay <="00";
    elsif rising_edge(tft_clk_int) then
        case TFT_state is
            when s_idle => -- Wait for Chip select and bus strobe state machine.
                if (CPU_CS6n='0' and CPU_RDn='0' and cpu_bs_int = '0') then
                    tft_read_int <= '0';
                    tft_state <= s_read;
                end if;
                if (CPU_CS6n='0' and CPU_WEn/= '1' and cpu_bs_int = '0') then
                    tft_write_int <= '0';
                    tft_state <= s_write;
                end if;
                tft_delay <="00";
            when s_read => -- Insert minimum wait of 2 clocks on TFT bus.
                if (tft_wait_int='1' and tft_delay = "10" ) then
                    tft_read_int <= '1';
                    tft_state <= s_end;
                end if;
                tft_delay <= tft_delay + '1';
            when s_write => -- Insert minimum wait of 2 clocks on TFT bus.
                if (tft_wait_int='1' and tft_delay = "10") then
                    tft_write_int <= '0'; -- write is rd/wr signal
                    tft_state <= s_end;
                end if;
                tft_delay <= tft_delay + '1';
            when s_end => -- Clean up for writes
                if (cpu_state=s_end) then
                    tft_write_int <= '1';
                    tft_state <= s_idle;
                end if;
            when others => null;
        end case;
    end if;
end process;

```

```
        end case;  
        tft_we0_int    <= CPU_WE0n;  
        tft_we1_int    <= CPU_WE1n;  
    end if;  
end process;
```

```

-- Chip Select 5 Address Decoder
process(SYS_RESETEn, CPU_CS5n, cpu_cs5n_int, CS5_SEL, CPU_ADDR)
begin
    if (SYS_RESETEn='0') then
        CPU_CS5An <= '1';
        CPU_CS5Bn <= '1';
        CPU_CS5Cn <= '1';
        CPU_CS5Dn <= '1';
    else if (CPU_CS5n = '0') then
        case CS5_SEL(1 downto 0) is
            when "00" =>
                case(CPU_ADDR(23 downto 22)) is
                    when "00" => CPU_CS5An <= cpu_cs5n_int;
                                CPU_CS5Bn <= '1';
                                CPU_CS5Cn <= '1';
                                CPU_CS5Dn <= '1';
                    when "01" => CPU_CS5An <= '1';
                                CPU_CS5Bn <= cpu_cs5n_int;
                                CPU_CS5Cn <= '1';
                                CPU_CS5Dn <= '1';
                    when "10" => CPU_CS5An <= '1';
                                CPU_CS5Bn <= '1';
                                CPU_CS5Cn <= cpu_cs5n_int;
                                CPU_CS5Dn <= '1';
                    when "11" => CPU_CS5An <= '1';
                                CPU_CS5Bn <= '1';
                                CPU_CS5Cn <= '1';
                                CPU_CS5Dn <= cpu_cs5n_int;
                    when others => CPU_CS5An <= '1';
                                CPU_CS5Bn <= '1';
                                CPU_CS5Cn <= '1';
                                CPU_CS5Dn <= '1';
                end case;
            when "01" =>
                case(CPU_ADDR(24 downto 23)) is
                    when "00" => CPU_CS5An <= cpu_cs5n_int;
                                CPU_CS5Bn <= '1';
                                CPU_CS5Cn <= '1';
                                CPU_CS5Dn <= '1';
                    when "01" => CPU_CS5An <= '1';
                end case;
        end case;
    end if;
end process;

```

```

        CPU_CS5Bn <= cpu_cs5n_int;
        CPU_CS5Cn <= '1';
        CPU_CS5Dn <= '1';
    when "10" => CPU_CS5An <= '1';
        CPU_CS5Bn <= '1';
        CPU_CS5Cn <= cpu_cs5n_int;
        CPU_CS5Dn <= '1';
    when "11" => CPU_CS5An <= '1';
        CPU_CS5Bn <= '1';
        CPU_CS5Cn <= '1';
        CPU_CS5Dn <= cpu_cs5n_int;
    when others => CPU_CS5An <= '1';
        CPU_CS5Bn <= '1';
        CPU_CS5Cn <= '1';
        CPU_CS5Dn <= '1';
end case;
when "10" =>
    case(CPU_ADDR(25 downto 24) )is
        when "00" => CPU_CS5An <= cpu_cs5n_int;
            CPU_CS5Bn <= '1';
            CPU_CS5Cn <= '1';
            CPU_CS5Dn <= '1';
        when "01" => CPU_CS5An <= '1';
            CPU_CS5Bn <= cpu_cs5n_int;
            CPU_CS5Cn <= '1';
            CPU_CS5Dn <= '1';
        when "10" => CPU_CS5An <= '1';
            CPU_CS5Bn <= '1';
            CPU_CS5Cn <= cpu_cs5n_int;
            CPU_CS5Dn <= '1';
        when "11" => CPU_CS5An <= '1';
            CPU_CS5Bn <= '1';
            CPU_CS5Cn <= '1';
            CPU_CS5Dn <= cpu_cs5n_int;
        when others => CPU_CS5An <= '1';
            CPU_CS5Bn <= '1';
            CPU_CS5Cn <= '1';
            CPU_CS5Dn <= '1';
    end case;
when "11" =>

```

```
        CPU_CS5An <= cpu_cs5n_int;
        CPU_CS5Bn <= '1';
        CPU_CS5Cn <= '1';
        CPU_CS5Dn <= '1';
    when others =>
        CPU_CS5An <= '1';
        CPU_CS5Bn <= '1';
        CPU_CS5Cn <= '1';
        CPU_CS5Dn <= '1';
    end case;
else
    CPU_CS5An <= '1';
    CPU_CS5Bn <= '1';
    CPU_CS5Cn <= '1';
    CPU_CS5Dn <= '1';
end if;
end if;
end process;

end LCL_TFT_IF_arch;
```

Chapter 13. Additional Information

For details on how to use High-performance Embedded Workshop (HEW, refer to the HEW manual available on the CD or from the web site.

For information about the SH/7670 series microcontrollers refer to the SH/7670 Group hardware manual.

For information about the SH/7670 assembly language, refer to the SH2-A Series Software Manual.

Online technical support and information is available at: http://www.renesas.com/renesas_starter_kits

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General information on Renesas Microcontrollers can be found on the Renesas website at: <http://www.renesas.com/>

Renesas Starter Kit 2+ for SH/7670

User's Manual

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