User's Manual

RZ/G2L-SBC, Single Board Computer

Quick Start Guide

Renesas Microprocessor
RZ Family RZ/G Series

OPN
US157-G2LSBCPOCZ

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1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Introduction

This Quick Start Guide describes the RZ/G2L based single board computer setup. This system architecture is of a generic single-board computer based on the Renesas RZ/G2L series SoC. It is a fully capable general purpose computer module aimed at HMI, industrial, and robotics applications.

This SBC features a Renesas RZ/G2L MPU as the main processor and runs a Linux distro built on Yocto OE using the Renesas VLP 3.0.5 package as its source.

One of the key highlights is the ease at which the board can be used to quickly create a PoC using a wide array of peripheral ports and proven accessories / modules. It comes equipped with an extensive set of features and interfaces, including onboard Wi-Fi, PMOD interface and dual ethernet ports.

Features

The RZ/G2L-SBC board contains the following features:

- RZ/G2L consisting of Dual core Cortex®A55 SoC with on-chip Cortex M33 core for real time applications.
- 1 GiB DDR4 (single chip of 4 Gbit)
- Micro SD card socket for OS image and rootfs
- 64 MB QSPI flash for boot
- Temperature sensor with on-chip EEPROM holding board configuration data.
- Onboard Laird 802.11 Wi-Fi module
- 40-pin Header connector (Raspberry Pi 3B compatible)
- Four USB 2.0 Type-A ports
- Dual Gigabit Ethernet ports
- 3.5mm Audio Port
- Mini- HDMI supporting full HD displays.
- MIPI-CSI port (Arduino compatible)
- MIPI-DSI port (Raspberry Pi compatible)
- Dual expansion ports for adapter board interfacing:
    - 40-pin DSI display modules.
    - 6 pin I2C touch modules.
    - ADC.
    - Bootstrapping.
    - External power and ground.
- USB Type-C Power connector
- Status LED indicators
- Board dimensions: 82 mm * 50 mm
- Mount: Double-sided mounting (10 layers)

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Physical View

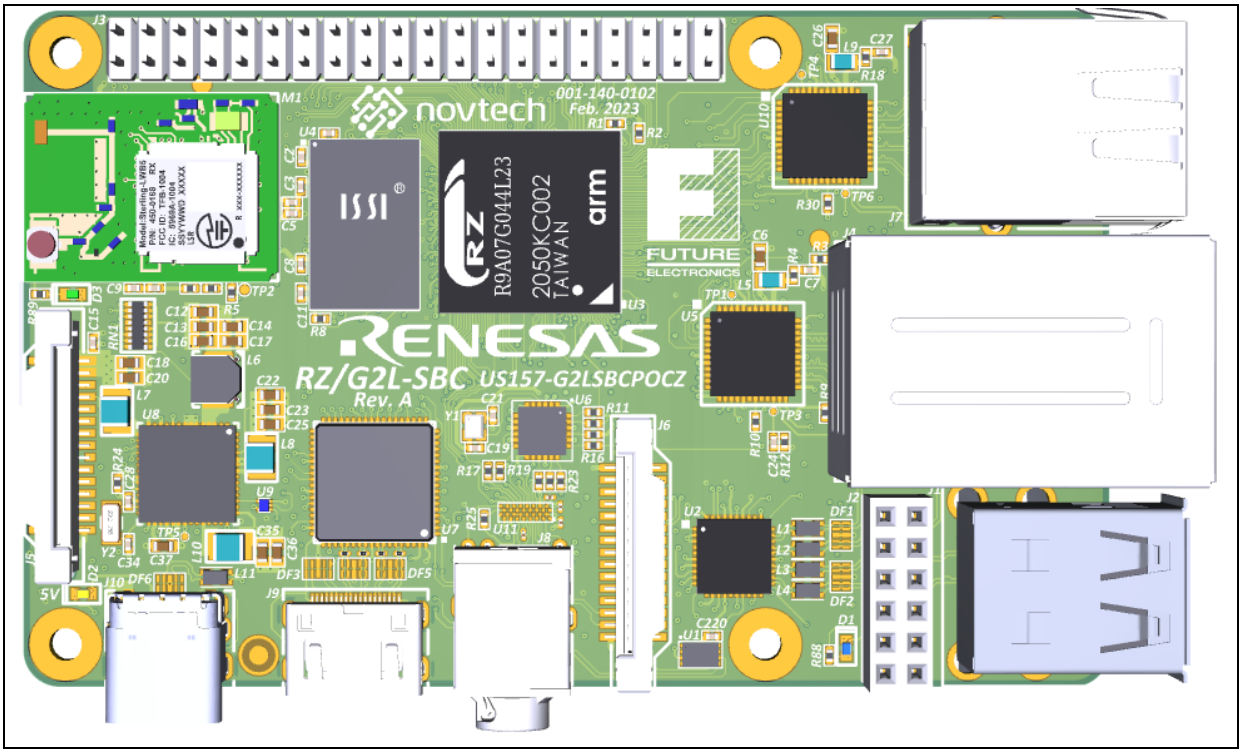

Figure 1: Top side view of the RZ/G2L-SBC

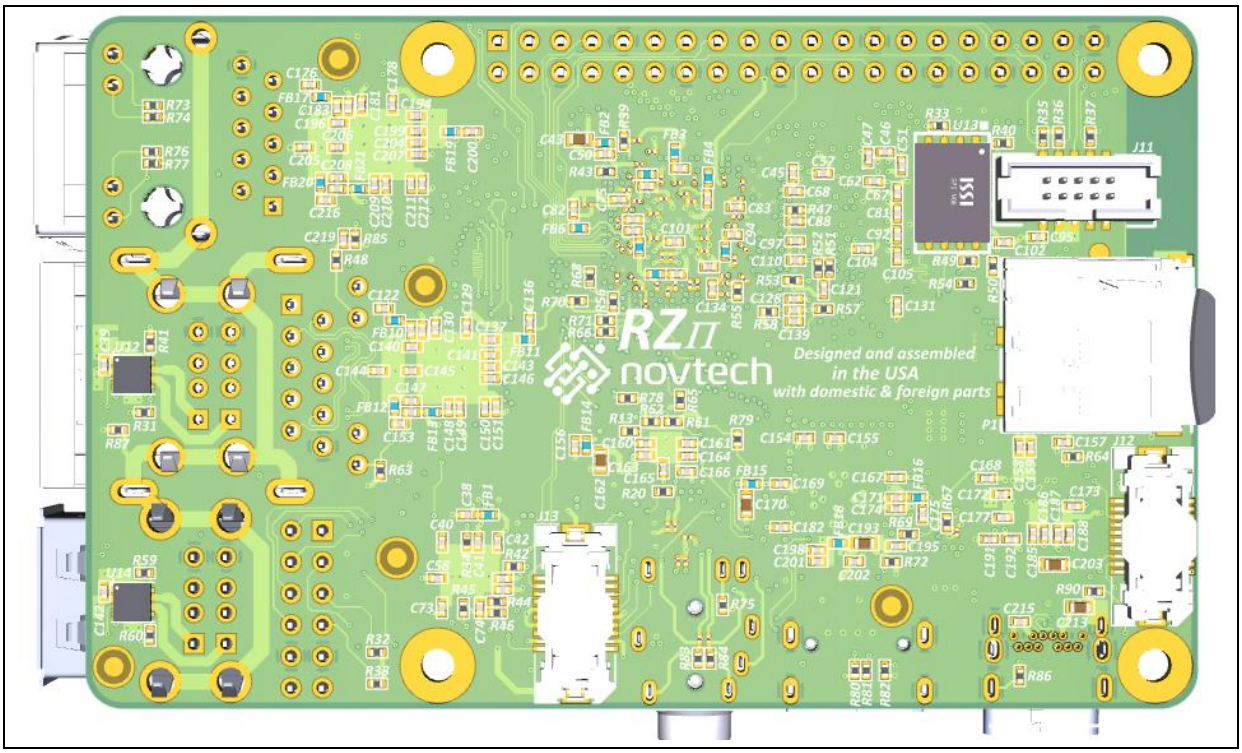

Figure 2: Bottom side of the RZ/G2L-SBC

Quick Start

Hardware requirement

The basic hardware setup consists of the following:

1. RZ/G2L-SBC
2. FTDI RS232 UART cable
3. USB-C 5V 3A+ power supply
4. SD-mmc card (minimum 8 GB)
5. 1080p HDMI display / Waveshare 5” MIPI DSI display touch panel
6. Ethernet cables (optional for wired networking).
7. OV5640 MIPI CSI camera (Optional for image capture).
8. USB keyboard and mouse
9. 3.5mm Headphone with microphone

Essential Hardware Setup

Given below is the basic essential hardware setup. We expect at least the UART cable and an HDMI display to be available.

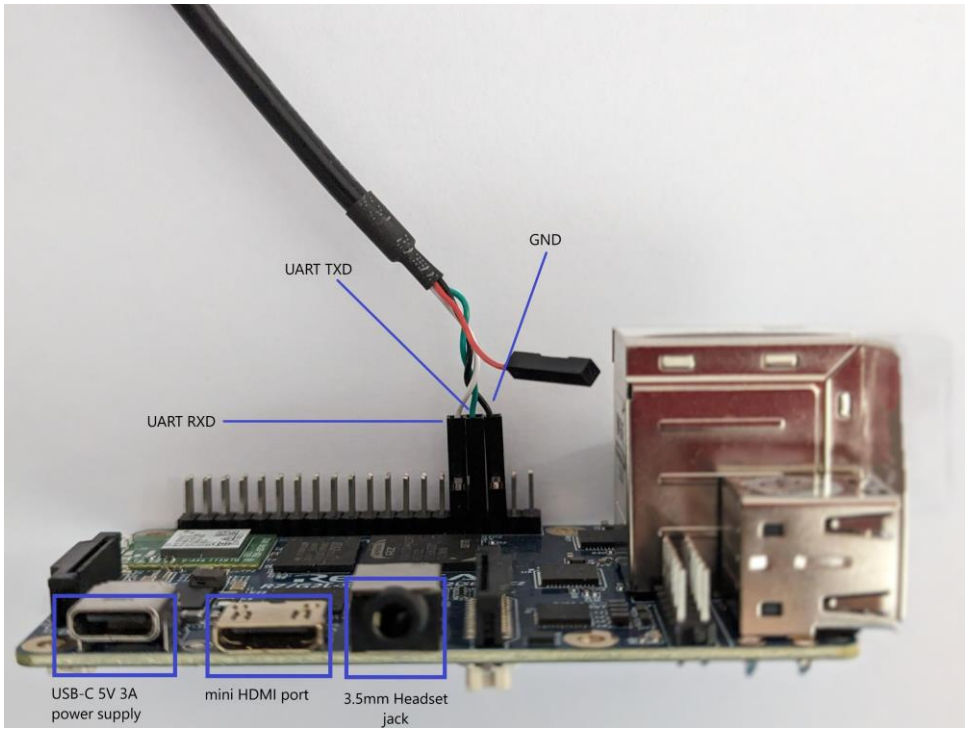

Figure 3: Essential minimum interfaces needed

Note: Please note that the release consists of a QT demo image. Due to this we expect at least one display to be available which is the basic 1080p HDMI monitor. However, you may also use the DSI touch panel as described in **Error! Reference source not found.** section in the User manual.

We also highly recommend that you use an FTDI cable for the UART and not any other converter chip.

Complete Hardware Setup

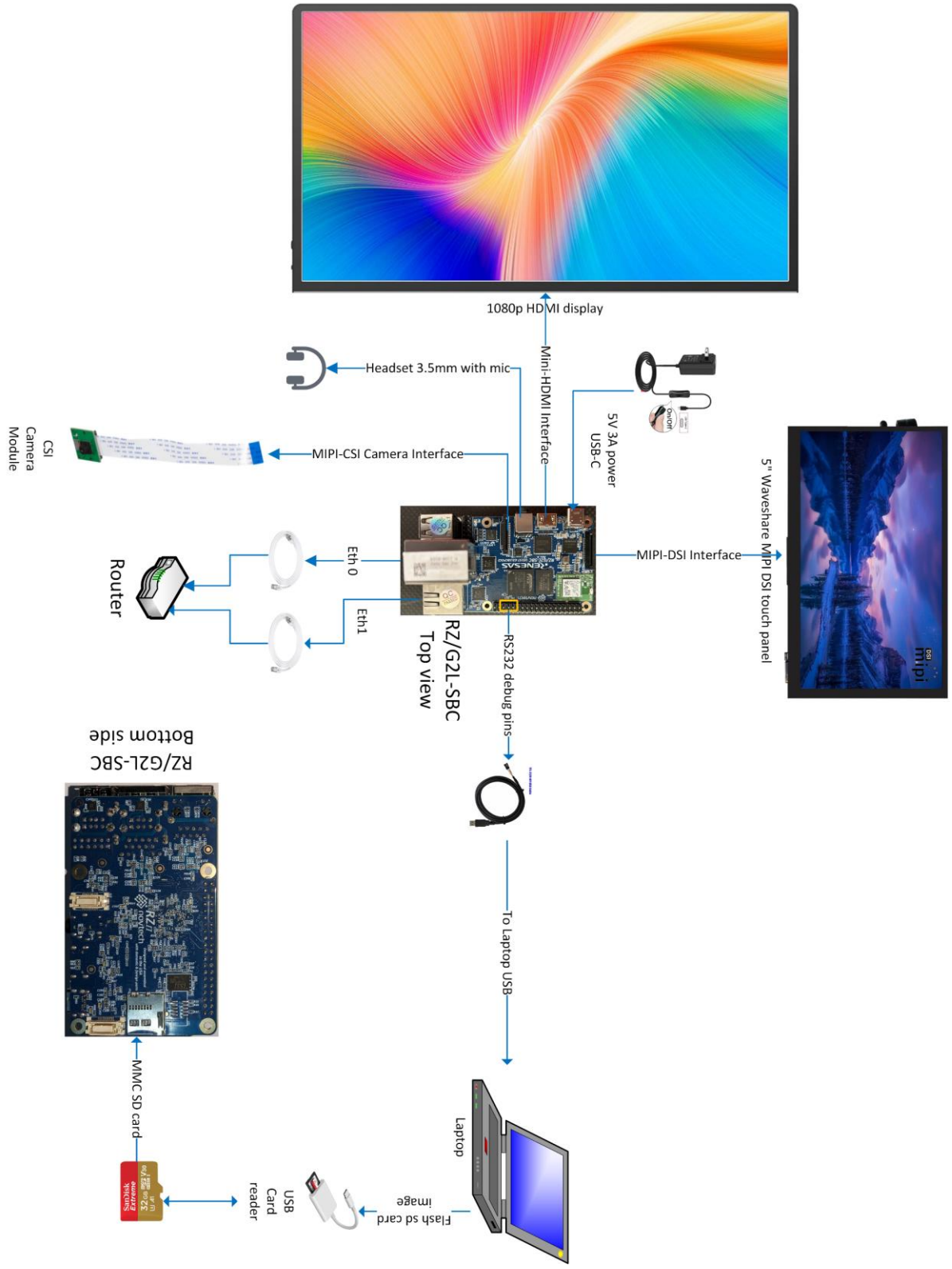

Figure 4: Complete setup

Linux SD Card Creation

The Linux bootable SD card creation is a very simple process. The idea is to use any filesystem imaging tool (etcher) to burn the '.wic' file (core-image-qt-rzpi.wic) located in the 'target/images' directory of the release. to the sd card. We recommend that you install Balena etcher which is available for Linux, MacOS and Windows.

The UI is Straight forward.

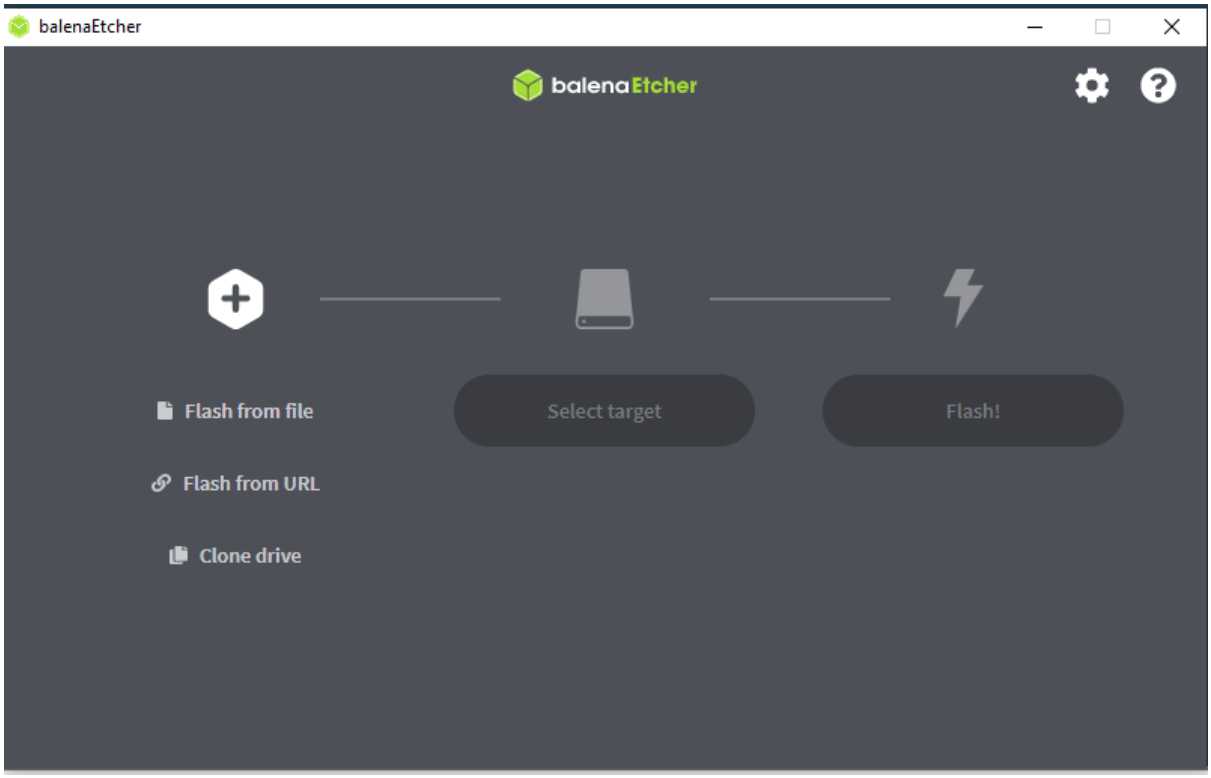

Figure 5: Balena etcher UI

Steps:

1. Select "Flash from File".
2. In popup window, navigate to your release and select the file '(core-image-qt-rzpi.wic'.
3. Then click on 'Select target' and it will list all available devices. Select your sd card. Be mindful not to select your primary laptop hard drive.
4. Select 'Flash'.
5. When Flashing is completed, it will automatically dismount the sd-card device.
6. Insert the sd-card into the RZ/G2L-SBC bottom sd-card connector.

Booting

The booting is straight forward. Insert the MMc card to the mmc port in the bottom side of the RZ/G2L-SBC. Connect keyboard, mouse, hdmi display; then insert the USB-C power supply and turn the power on. You should see the boot log on the UART console and the Weston desktop with qt apps on the HDMI screen. You can now click on any of the applications and interact with it.

The image is fully featured and has powerful desktop grade features. Explore the user manual from the release package to learn about all the features packed into the Linux image.

Overview of Connectors

Given below is the basic positioning of the top-level connectors.

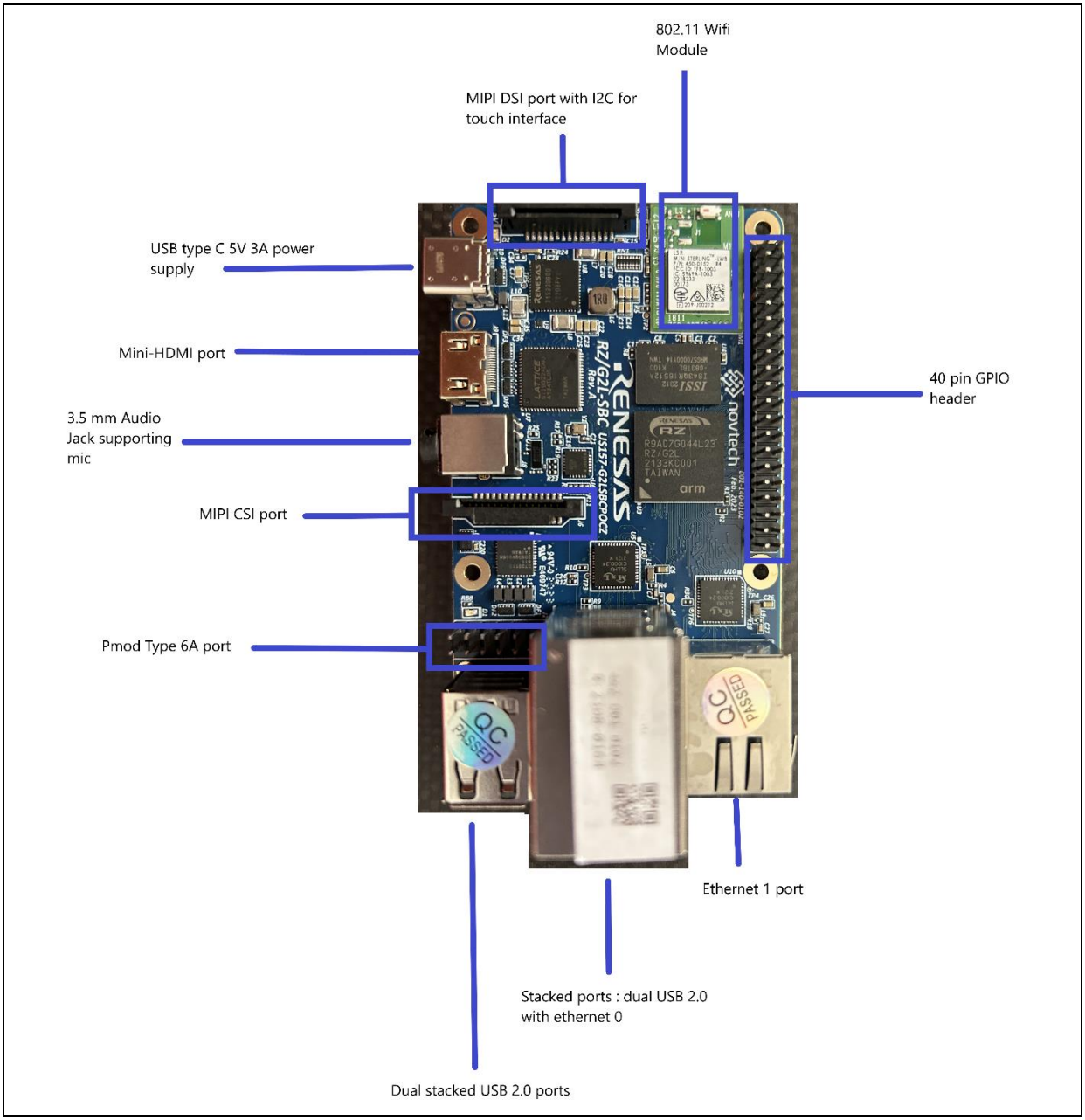

Figure 6: RZ/G2L-SBC top side connectors.

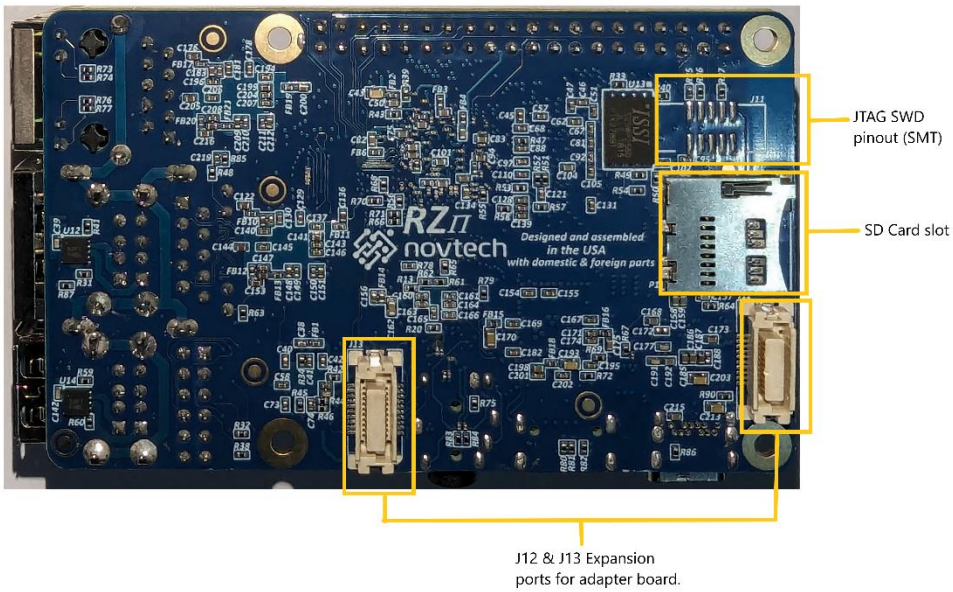

Figure 7: RZ/G2L-SBC Bottom view connectors.

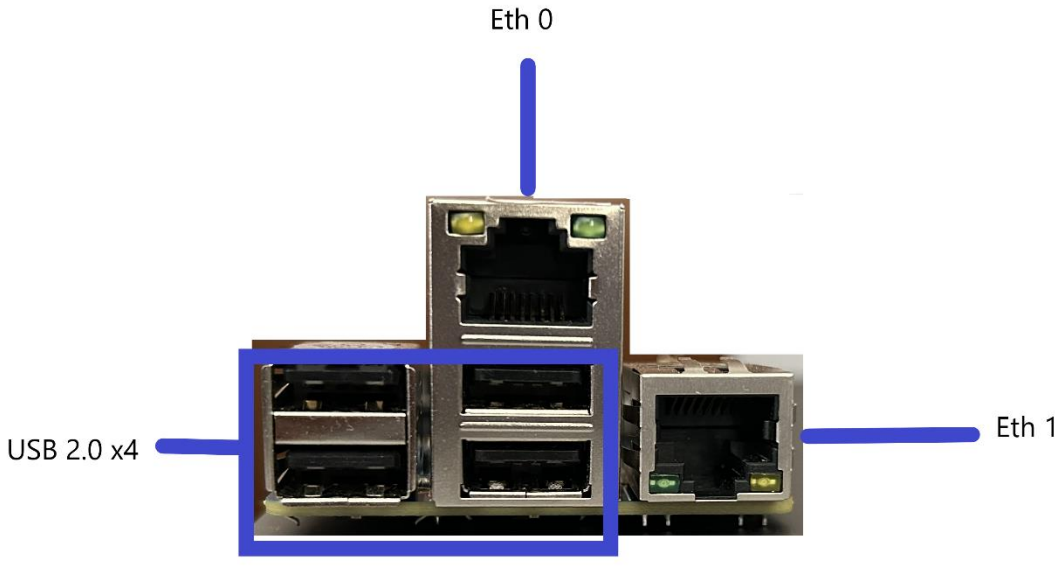

Figure 8: RZ/G2L-SBC side view I/O ports.

Power Supply

This section delves into the RZ/G2L-SBC's power supply architecture. The RZ/G2L-SBC uses a simple design, with a 5V supply as the single external power source.

USB Type-C Power

This board has one USB Type-C receptacle for power input with USB chargers. The USB type–C power connector is meant to connect to a 5V power supply. The RZ/G2L-SBC requires a minimum of 3A power to prevent brownouts. However, we recommend a 4.5 -5A power supply as several ports support peripherals consuming substantial power.

Peripheral Interface

40-pin I/O Header

The RZ/G2L-SBC comes with a 40-pin GPIO interface which is broadly compliant with Raspberry Pi 3 40-pin GPIO interface and provides additional interfaces like two CAN ports. The diagram below shows the pin configuration along with marking of the bottom I/O ports for reference of the orientation of the board.

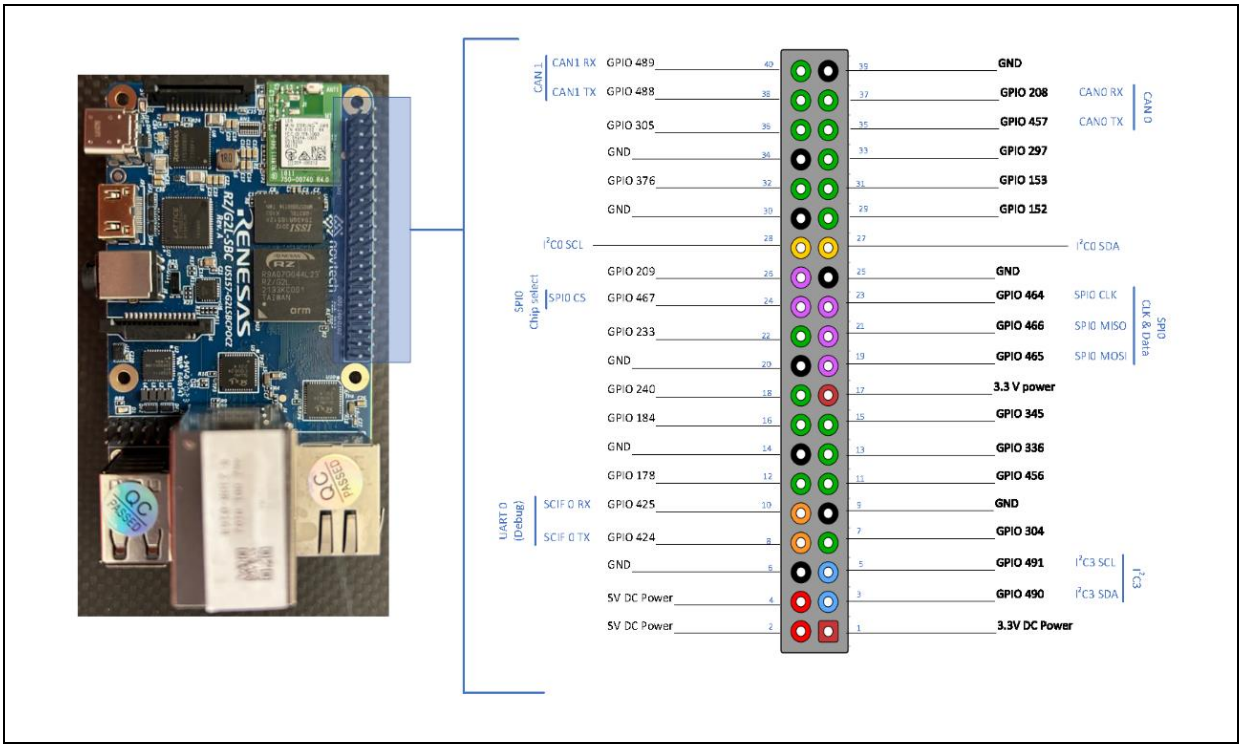

Figure 9: 40 PIN GPIO map with orientation details.

PMOD Type 6A Standard Interface

The RZ/G2L-SBC is equipped with a 2x6 pin header routed to the PMOD Type-6A interface conforming to the 1.3.0 specification of PMOD. It includes the alternate pin functions from the specification.

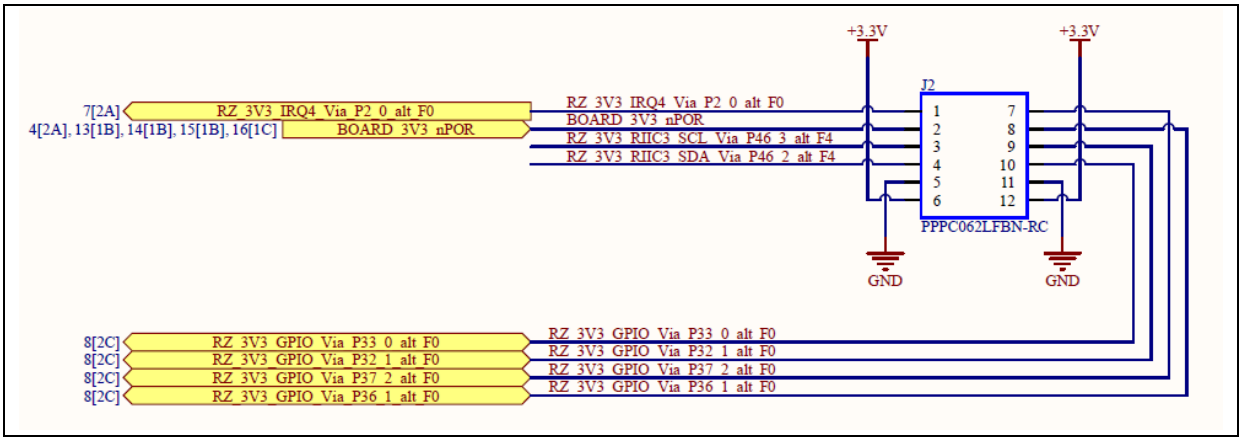

Figure 10: Schematic of PMOD Type 6 A pin header J2.

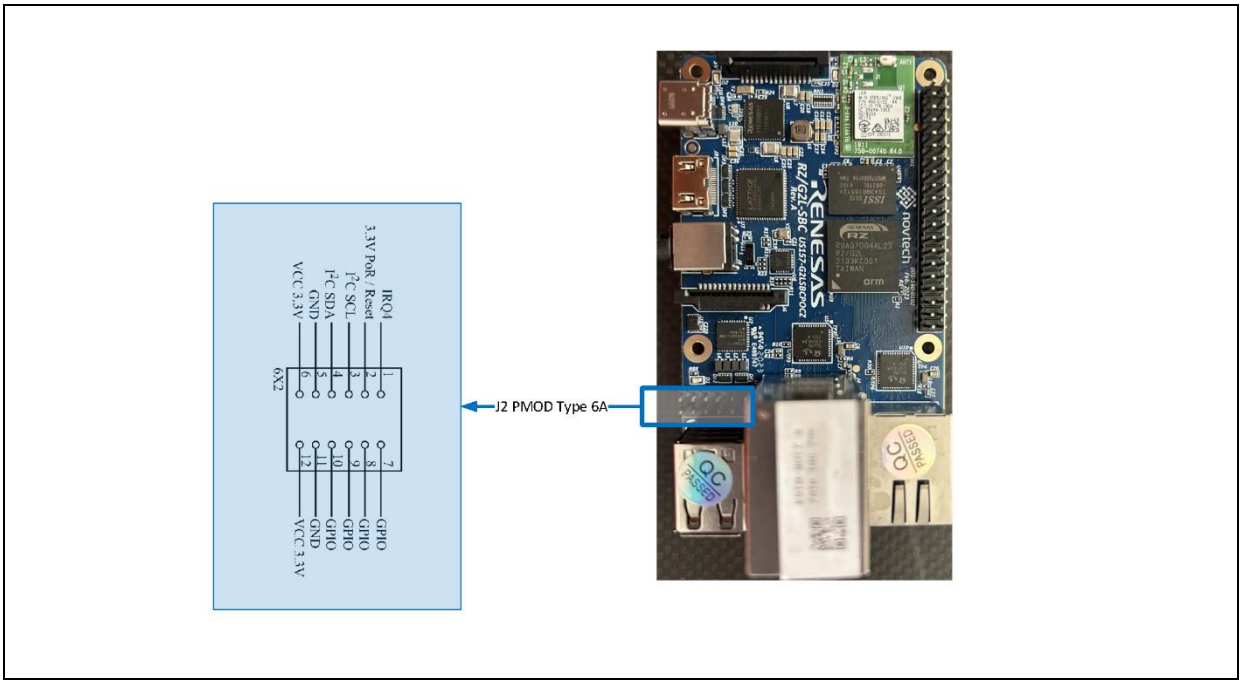

Figure 11: PMOD Type 6A 2x6 0.1mm pin out with orientation details.

uSD-Card Interface

The RZ/G2L-SBC comes with a spring-loaded micro-sd card slot. This is intended to be the primary storage as well as the OS boot device. The SD card is connected to channel 0 of the RZ/G2L SoC SD/MMC interface. The SoC SDIO interface is compliant with memory card standard version 3.0 and supports UHS-1 mode of 50 MB/s (SDR50) and 104 MB/s (SDR104).

How to get the console after bootup

Once the RZ/G2L-SBC has booted, on the UART terminal you will be able to login using the default user ‘root’. There is no password. Leave the password field empty and just hit the return / enter key.

Figure 12: Root login of Linux console over UART 0.

RZ/G2L SoC MPU Architecture

The RZ/G2L MPU is a feature-packed SoC (System on Chip) that can support a variety of applications. Below is an overview of SoC architecture.

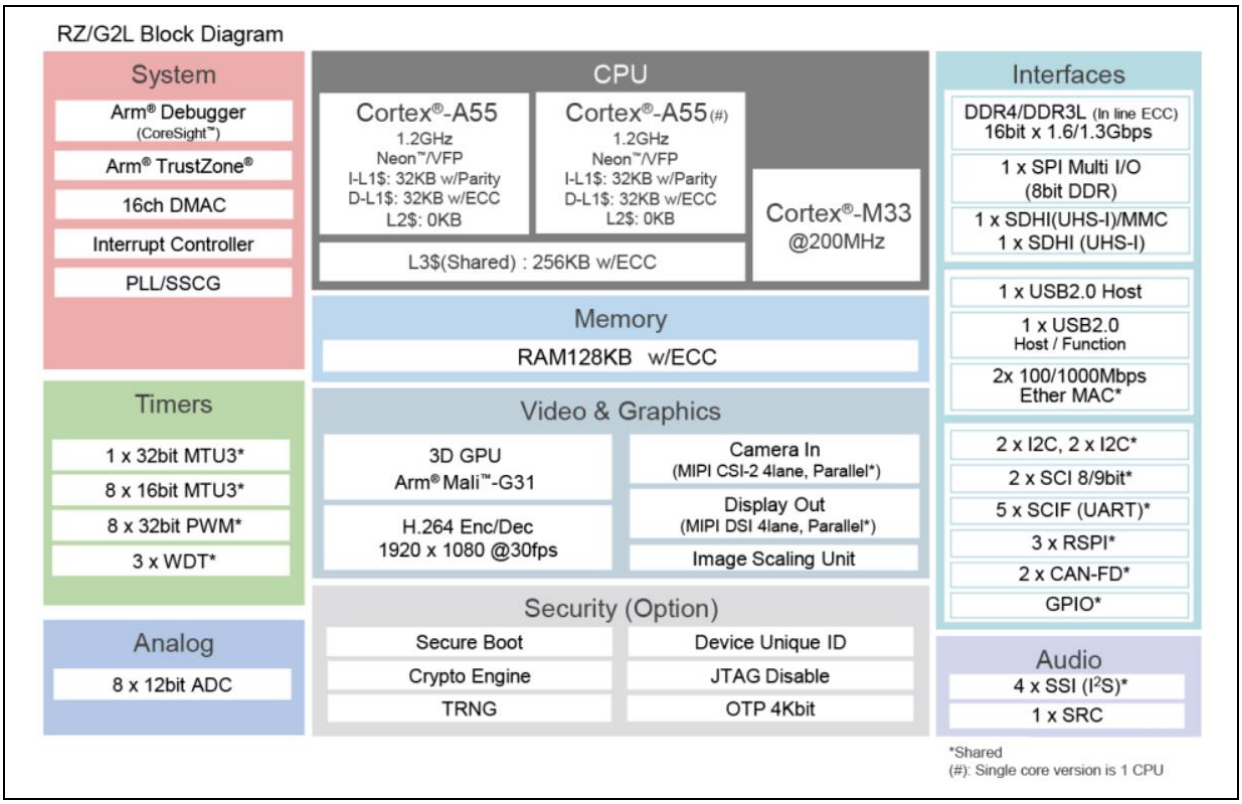

Figure 13: RZ/G2L SoC (System on Chip) Overview

Operational Flow

The diagram below will show the operational flow of the RZ/G2L-SBC system during power ON.

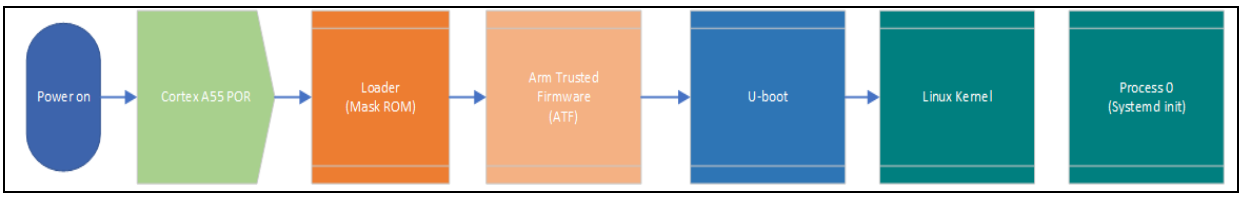

Figure 14: RZ/G2L-SBC boot operational flow

By default, the main processor will be in power OFF state to conserve battery. When the power is supplied, the PMIC immediately cycles power and puts the Cortex A55 into a POR state. This kickstarts the boot process with the Loader and ends with the Linux booting into user space.

While u-boot passes full control to the Linux kernel, arm trust zone remains active along with op-tee within the Arm core's trust zone of operations.

The exact boot time depends on the boot environment and the number of services in the initialization process.

Revision History

Rev.	Date	Description	
		Page	Summary
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