ISL70244SEH

Neutron Test Report

Introduction

This report summarizes results of 1MeV equivalent neutron testing of the ISL70244SEH 40V dual rail-to-rail input-output, low-power operational amplifier. These results also apply to the ISL73244SEH. The test was conducted to determine the sensitivity of the part to Displacement Damage (DD) caused by neutron or proton environments. Planned neutron fluences ranged from $5x10^{11}n/cm^2$ to $1x10^{14}n/cm^2$ with actual fluences coming in within ±15% of that. This project was carried out in collaboration with Honeywell Aerospace in Clearwater, FL, and their support is gratefully acknowledged.

Related Literature

For a full list of related documents, visit our website:

- ISL70244SEH and ISL73244SEH device pages
- MIL-STD-883 test method 1017

Product Description

The radiation hardened ISL7x244SEH is a 40V dual rail-to-rail input-output, low-power operational amplifier featuring two low-power amplifiers optimized to provide maximum dynamic range. These operational amplifiers (op amps) feature a unique combination of rail-to-rail operation on the input and output and a slew-rate enhanced front end that provides ultra fast slew rates positively proportional to a given step size. These features increase accuracy under both periodic and transient conditions. The ISL7x244SEH also offers low power, low offset voltage, and low temperature drift, which makes it ideal for applications requiring both high DC accuracy and AC performance.

The amplifiers are designed to operate over a single supply range of 2.7V to 40V or a split supply voltage range of ±1.35V to ±20V.

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency (DLA) in Columbus, OH. The SMD is the controlling document and must be cited when ordering.

1. Test Description

1.1 Irradiation Facility

Neutron fluence irradiations were performed on the test samples on June 26, 2018, at the WSMR Fast Burst Reactor (FBR) per Mil-STD-883G, Method 1017.2, with each part unpowered during irradiation and all leads shorted. The target irradiation levels were $5x10^{11}n/cm^2$, $2x10^{12}n/cm^2$, $1x10^{13}n/cm^2$, and $1x10^{14}n/cm^2$. As neutron irradiation activates many of the heavier elements found in a packaged integrated circuit, the parts exposed at the higher neutron levels required (as expected) some cooldown time before being shipped back to Renesas (Palm Bay, FL) for electrical testing.

1.2 Test Fixturing

No formal irradiation test fixturing is involved, as these DD tests are bag tests in the sense that the parts are irradiated with all leads shorted together.

1.3 Radiation Dosimetry

Table 1 shows the TLD and Sulfur pellet dosimetry from WSMR indicating the total accumulated gamma dose and actual neutron fluence exposure levels for each sets of samples. This dosimetry process is traceable to NIST (IAW ASTM E722).

Table 1. ISL7x244SEH Neutron Fluence Dosimetry Data

TLD		Sulfur Pellet						
TLD #	cGy(Si) (Note 1)	Pellet #	Distance (inches)	Exposure ID	Flu >3MeV (n/cm^2)	% Uncertainty (Note 2)	Total Fluence (n/cm^2)	1Mev Si (n/cm^2)
290	1.190E+02	6478	26.6	Free Field	7.493E+10	7.1%	6.059E+11	5.212E+11
280	3.802E+02	6416	13.45	Free Field	2.702E+11	7.1%	2.132E+12	1.890E+12
260	2.255E+03	6485	24	Free Field	1.427E+12	7.1%	1.145E+13	9.907E+12
257	1.562E+04	6482	8	Free Field	1.221E+13	7.1%	9.588E+13	8.565E+13

Notes:
1. 1 cGy(Si) = 1rad(Si)
2. The % Uncertainty column is applicable only to the Fluence >3MeV.

1.4 Characterization Equipment and Procedures

Electrical testing was performed before and after irradiation using the Renesas production Automated Test Equipment (ATE). All electrical testing was performed at room temperature.

1.5 Experimental Matrix

Testing proceeded in general accordance with the guidelines of MIL-STD-883 TM 1017. The experimental matrix consisted of five samples to be irradiated at $5x10^{11}n/cm^2$, five to be irradiated at $2x10^{12}n/cm^2$, five to be irradiated at $1x10^{13}n/cm^2$ and five to be irradiated at $1x10^{14}n/cm^2$. The actual levels achieved, which are shown in Table 2, were $5.2x10^{11}n/cm^2$, $1.9x10^{12}n/cm^2$, $9.9x10^{12}n/cm^2$ and $8.6x10^{13}n/cm^2$. Two control units were used.

The 20 ISL7x244SEH samples were drawn from Lots X2LOTT (18) and X2LOTS (2). Samples were packaged in the standard hermetic 10 lead Ceramic Flatpack (CFP) production package, code K10.A. Samples were processed through burn-in before irradiation and were screened to the SMD limits at room, low and high temperatures before the start of neutron testing.

2. Results

Neutron testing of the ISL7x244SEH is complete and the results are reported in the balance of this report. It should be understood when interpreting the data that each neutron irradiation was performed on a different set of samples; this is *not* total dose testing, where the damage is cumulative.

2.1 Attributes Data

Table 2. ISL7x244SEH Attributes Data

1MeV Fluence, (n/cm^2)		Sample Size	Pass (Note 3)	Fail	Notes
Planned	Actual				
5x10^{11}	5.2x10^{11}	5	5	0	All passed
2x10^{12}	1.9x10^{12}	5	5	0	All passed
1x10^{13}	9.9x10^{12}	5	0	5	Failed I_B at ±2.5V
1x10^{14}	8.6x10^{13}	5	0	5	Failed V_{OS}, I_B, A_{VOL}, PSRR

Note:
3. Pass indicates a sample that passes all SMD limits.

2.2 Variables Data

The plots in Figures 1 through 36 show data plots for key parameters before and after irradiation to each level. The plots show the mean of each parameter as a function of neutron irradiation. The plots also include error bars at each down-point, representing the minimum and maximum measured values of the samples, although in some plots the error bars might not be visible due to their values compared to the scale of the graph. While the applicable electrical limits taken from the SMD are also shown. **Note:** These limits are provided for guidance only as the ISL7x244SEH is not specified for the neutron environment.

All samples passed the post-irradiation SMD limits after all exposures up to and including 1.9x10^{12}n/cm^2, but all five tested units failed the SMD post-irradiation limits for input bias (I_B) at 2.5V (Figure 15) after 9.9x10^{12}n/cm^2 and some or all units failed measurements for input offset voltage (V_{OS}), input bias (I_B), open loop gain (A_{VOL}), Power Supply Rejection Ratio (PSRR), output voltage high (V_{OH}) and output voltage low (V_{OL}) after 8.6x10^{13}n/cm^2. Several of the V_{OS} measurements clamped the ATE at 509µV.

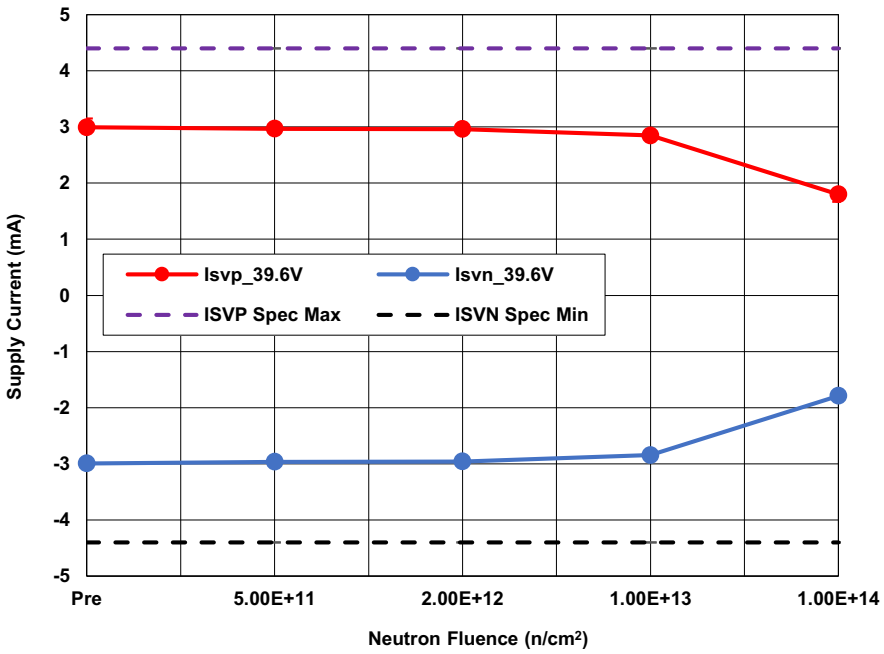

Figure 1. ISL7x244SEH positive (I_{SVP}) and negative (I_{SVN}) supply current (sum of both channels) at V_S = ±19.8V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -4.4mA minimum and 4.4mA maximum.

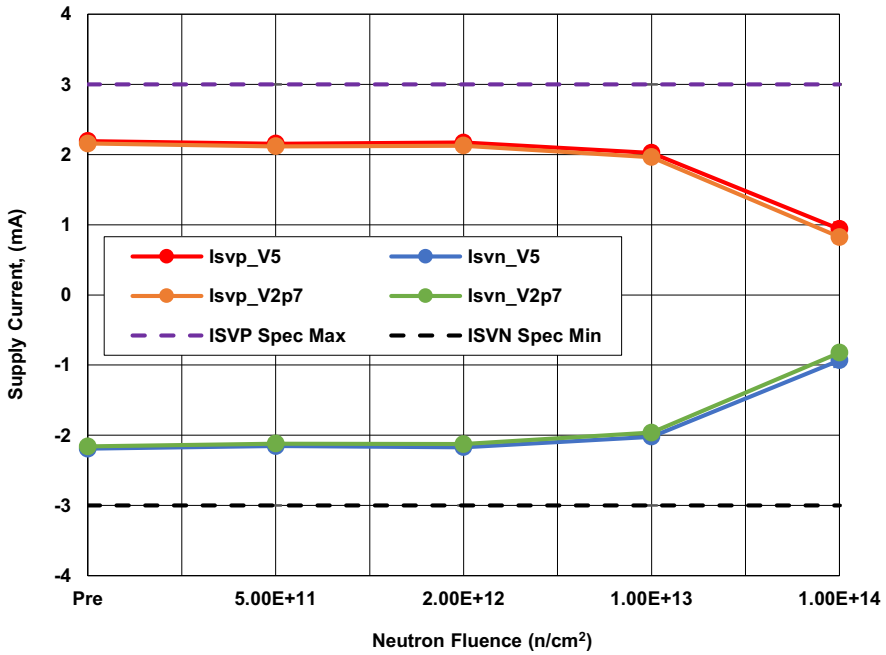

Figure 2. ISL7x244SEH positive (I_{SVP}) and negative (I_{SVN}) supply current (sum of both channels) at V_S = ±2.5V and ±1.35V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -3mA minimum and 3mA maximum.

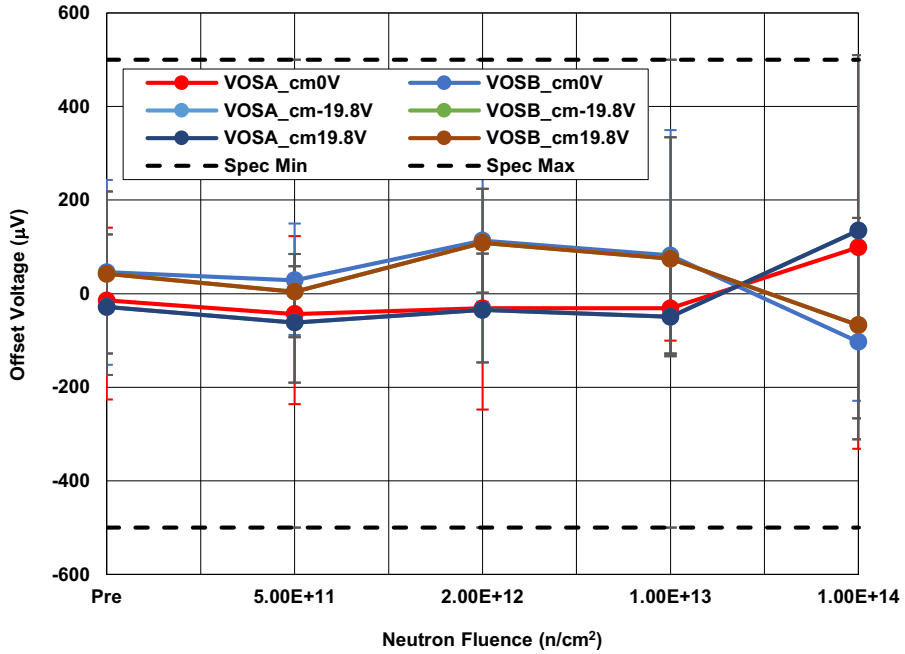

Figure 3. ISL7x244SEH input offset voltage (V_{OS}) at V_S = ±19.8V and V_{CM} = 0V, +19.8V and -19.8V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -500µV minimum and 500µV maximum.

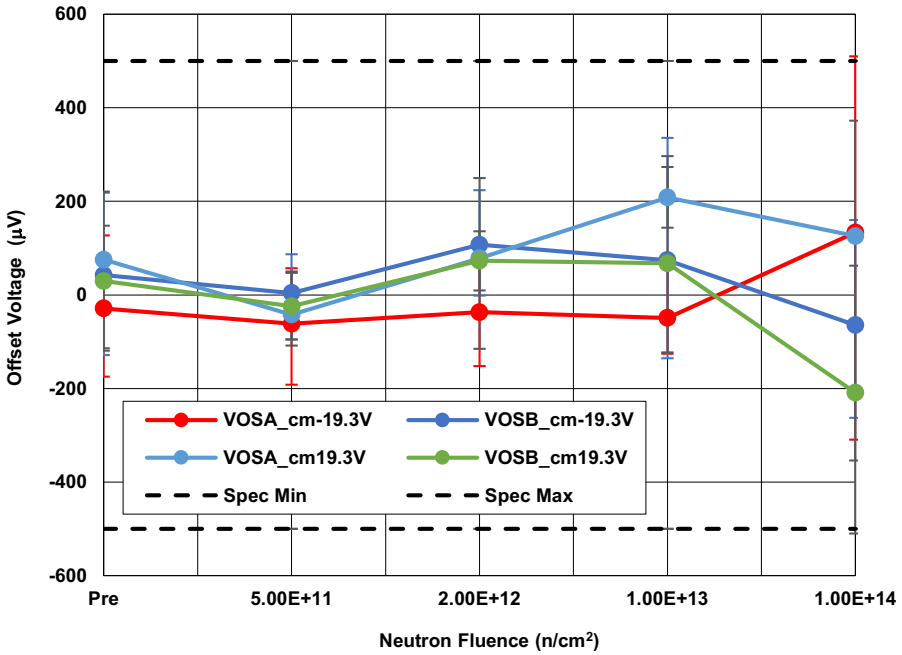

Figure 4. ISL7x244SEH input offset voltage (V_{OS}) at V_S = ±19.8V and V_{CM} = +19.3V and -19.3V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -500µV minimum and 500µV maximum.

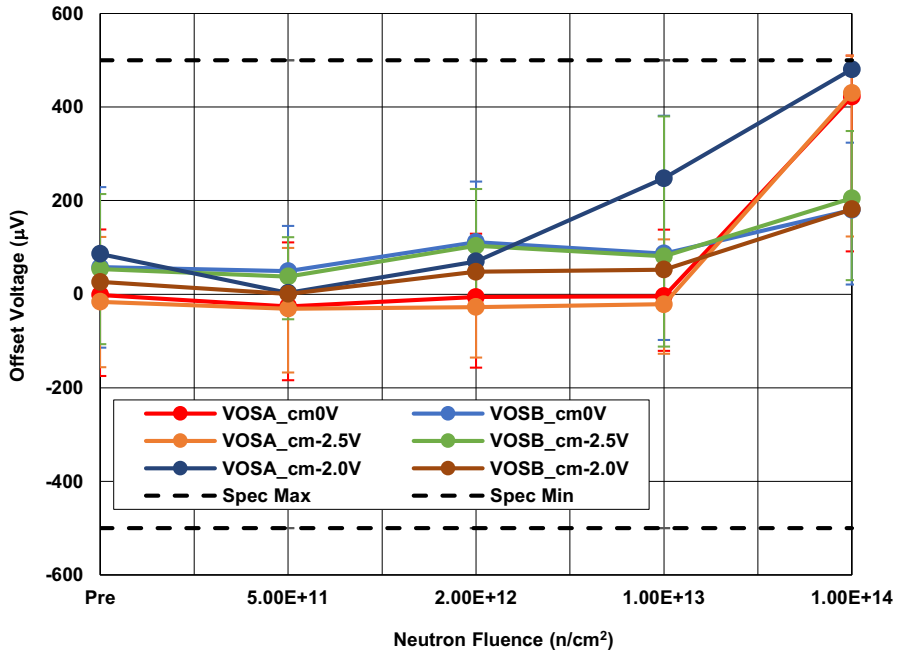

Figure 5. ISL7x244SEH input offset voltage (V_{OS}) at V_S = ±2.5V and V_{CM} = 0V, +2.5V and -2.5V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -500µV minimum and 500µV maximum.

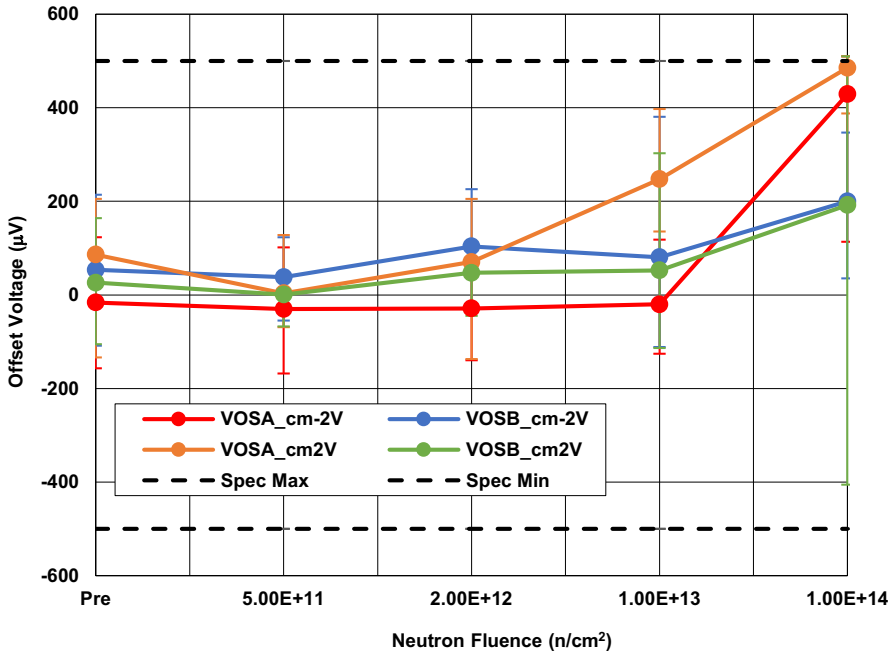

Figure 6. ISL7x244SEH input offset voltage (V_{OS}) at V_S = ±2.5V and V_{CM} = +2.0V and -2.0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -500µV minimum and 500µV maximum.

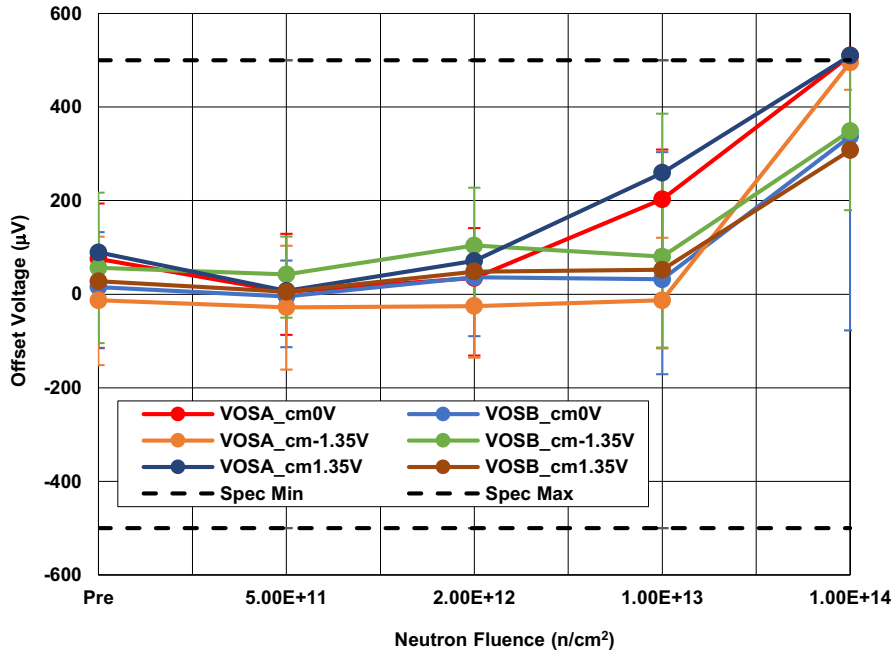

Figure 7. ISL7x244SEH input offset voltage (V_{OS}) at V_S = ±1.35V and V_{CM} = 0V, +1.35V and -1.35V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -500µV minimum and 500µV maximum.

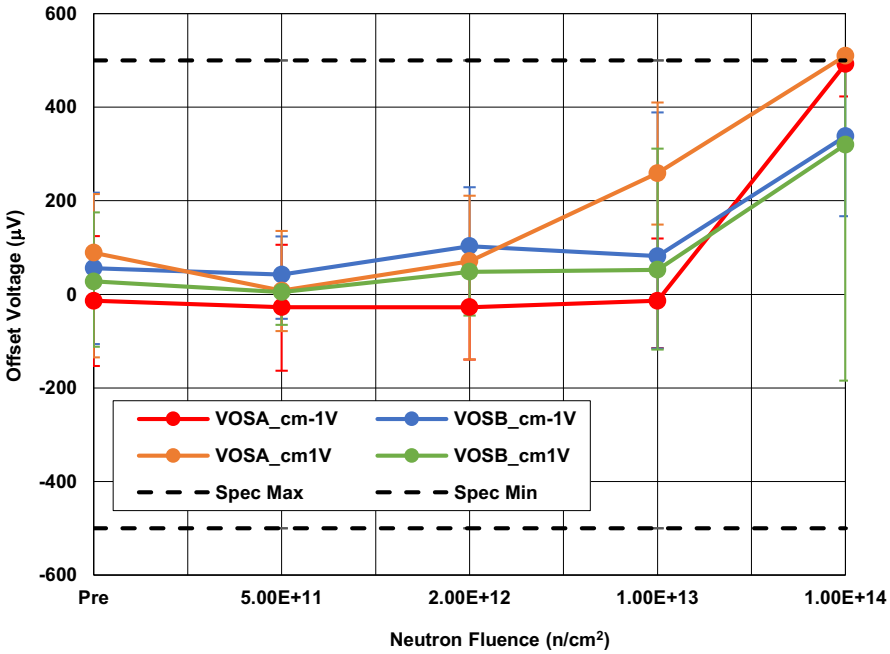

Figure 8. ISL7x244SEH input offset voltage (V_{OS}) at V_S = ±1.35V and V_{CM} = +1.0V and -1.0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -500µV minimum and 500µV maximum.

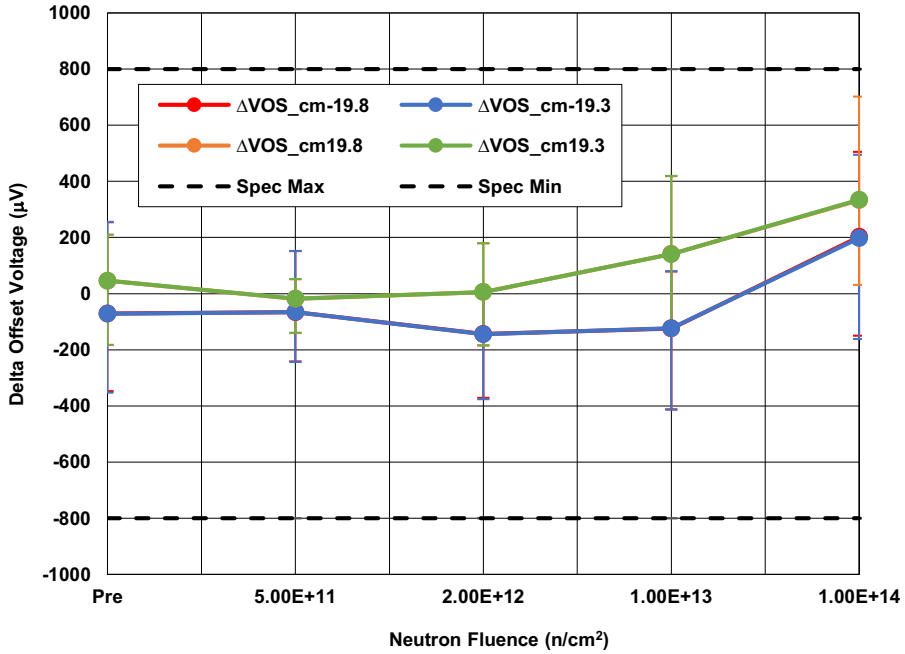

Figure 9. ISL7x244SEH input offset channel to channel match (ΔV_{OS}) at V_S = ±19.8V and V_{CM} = ±19.8V and ±19.3V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -800µV minimum and 800µV maximum.

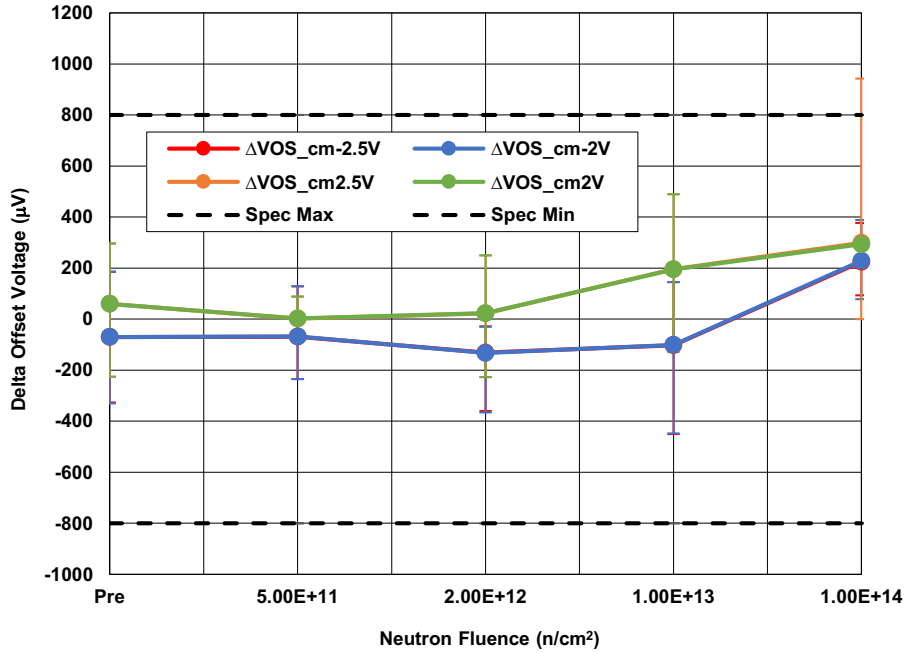

Figure 10. ISL7x244SEH input offset channel to channel match (ΔV_{OS}) at V_S = ±2.5V and V_{CM} = ±2.5V and ±2.0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -800µV minimum and 800µV maximum.

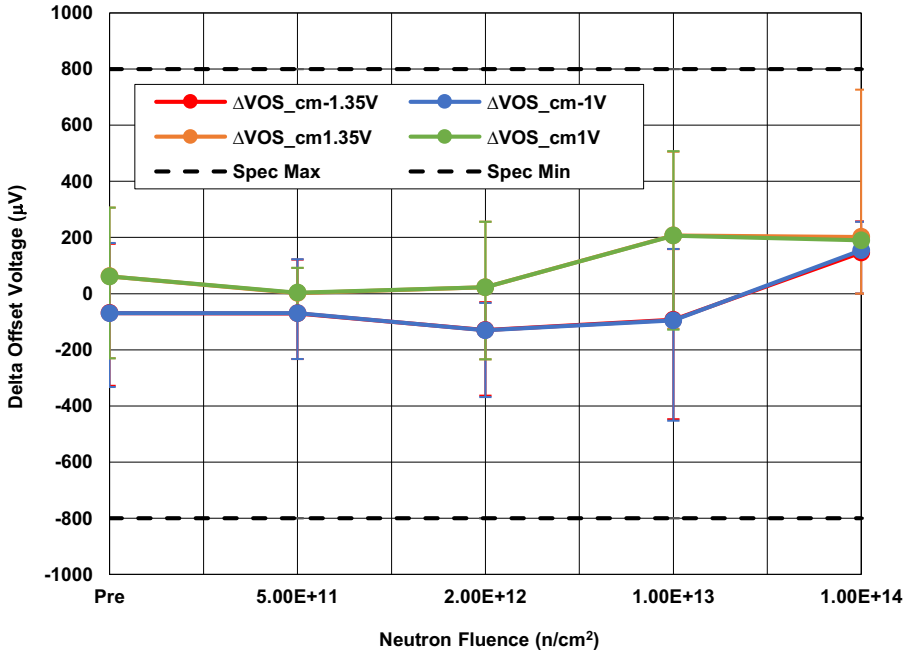

Figure 11. ISL7x244SEH input offset channel to channel match (ΔV_{OS}) at V_S = ±1.35V and V_{CM} = ±1.35V and ±1.0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -800µV minimum and 800µV maximum.

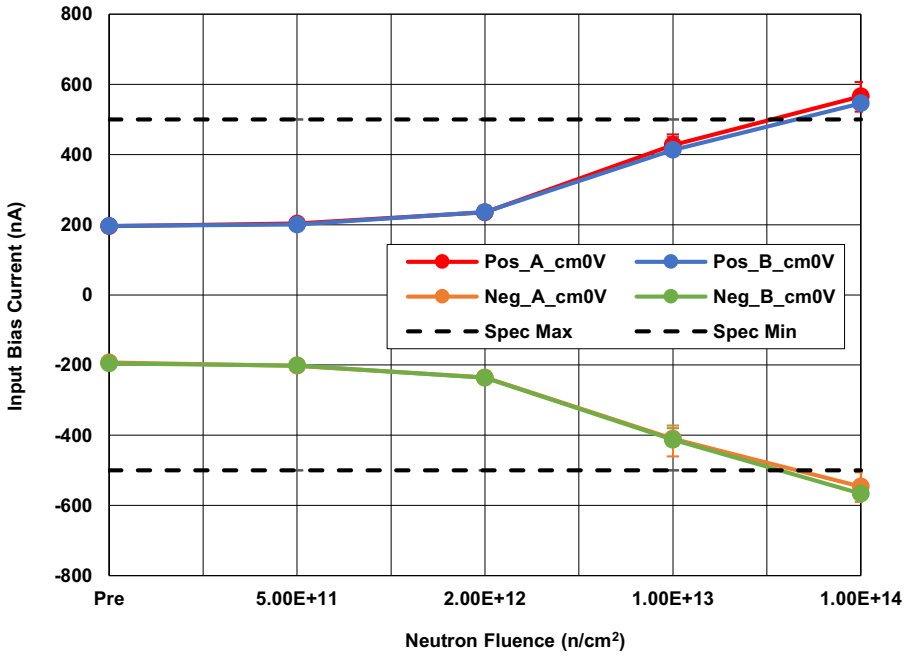

Figure 12. ISL7x244SEH input bias current (I_B) at V_S = ±19.8V and V_{CM} = 0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -500nA minimum and 500nA maximum.

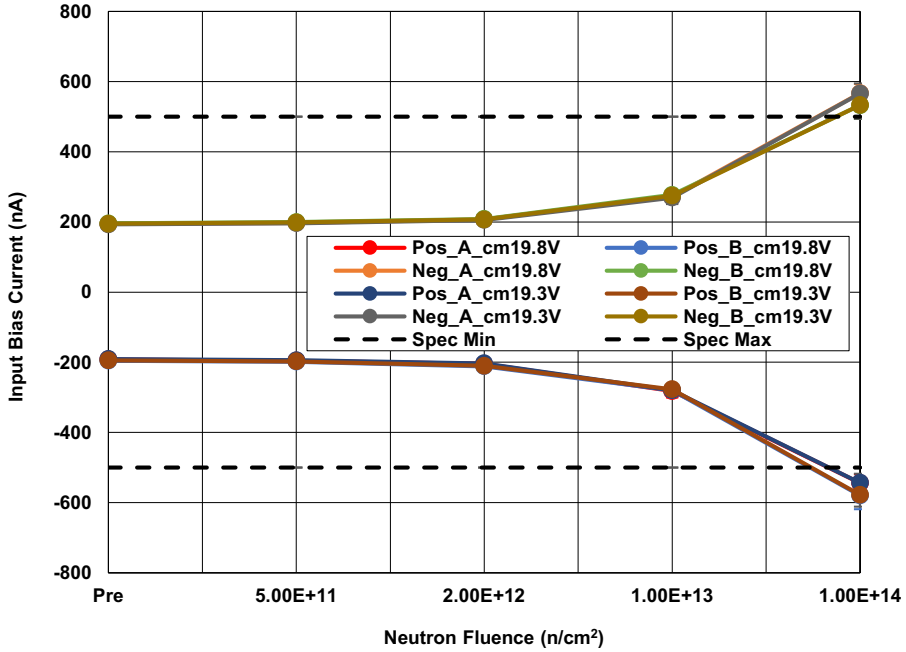

Figure 13. ISL7x244SEH input bias current (I_B) at V_S = ±19.8V and V_{CM} = +19.8V and +19.3V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -500nA minimum and 500nA maximum.

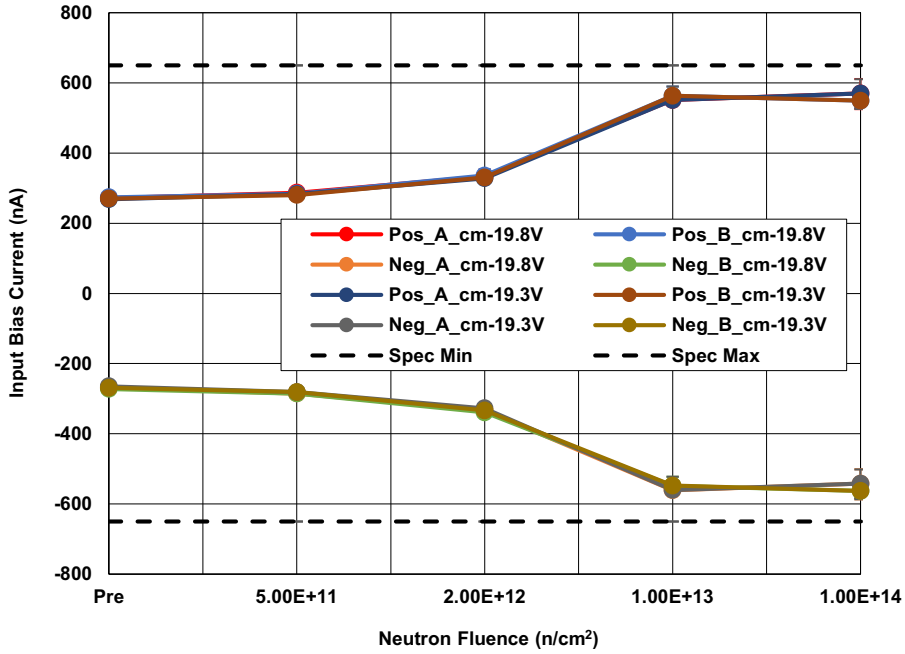

Figure 14. ISL7x244SEH input bias current (I_B) at V_S = ±19.8V and V_{CM} = -19.8V and -19.3V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -650nA minimum and 650nA maximum.

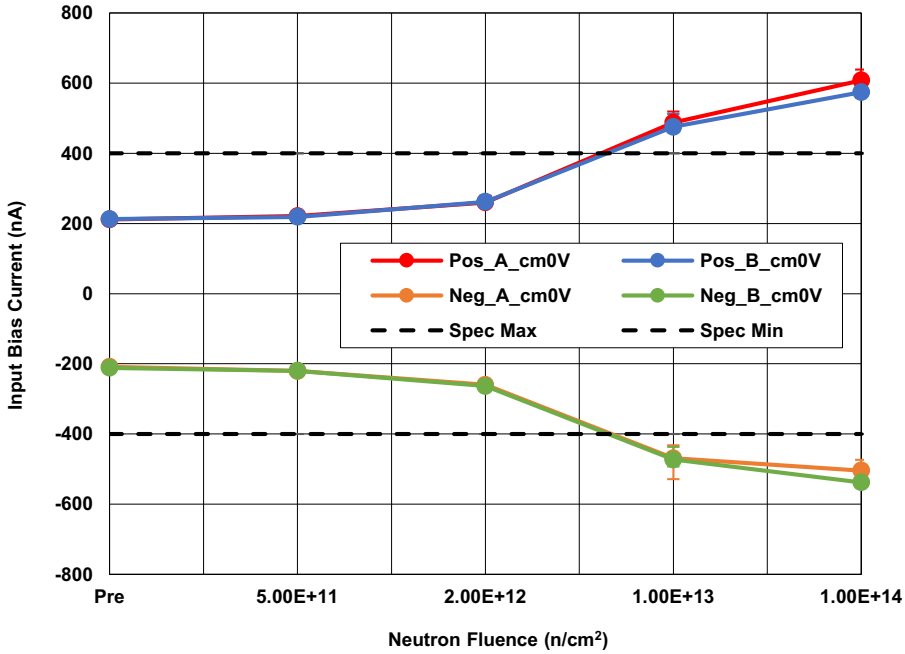

Figure 15. ISL7x244SEH input bias current (I_B) at V_S = ±2.5V and V_{CM} = 0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -400nA minimum and 400nA maximum.

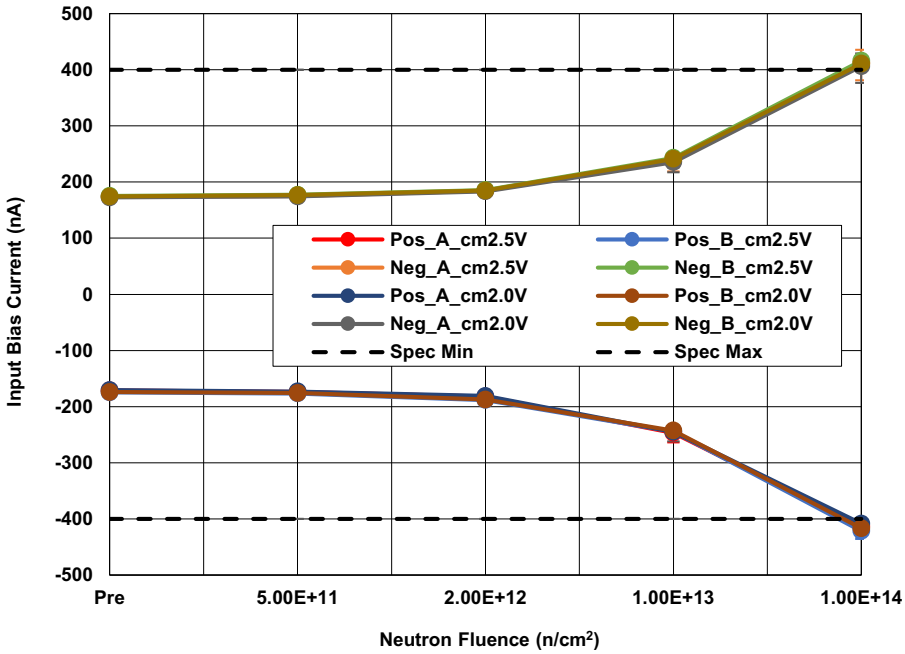

Figure 16. ISL7x244SEH input bias current (I_B) at V_S = ±2.5V and V_{CM} = +2.0V and +2.5V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -400nA minimum and 400nA maximum.

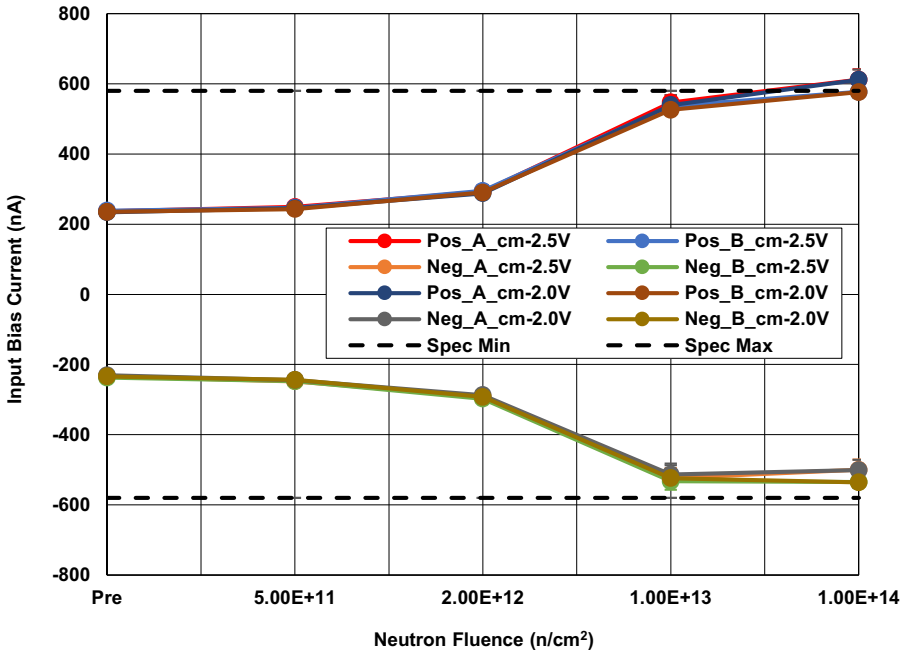

Figure 17. ISL7x244SEH input bias current (I_B) at V_S = ±2.5V and V_{CM} = -2.0V and -2.5V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -580nA minimum and 580nA maximum.

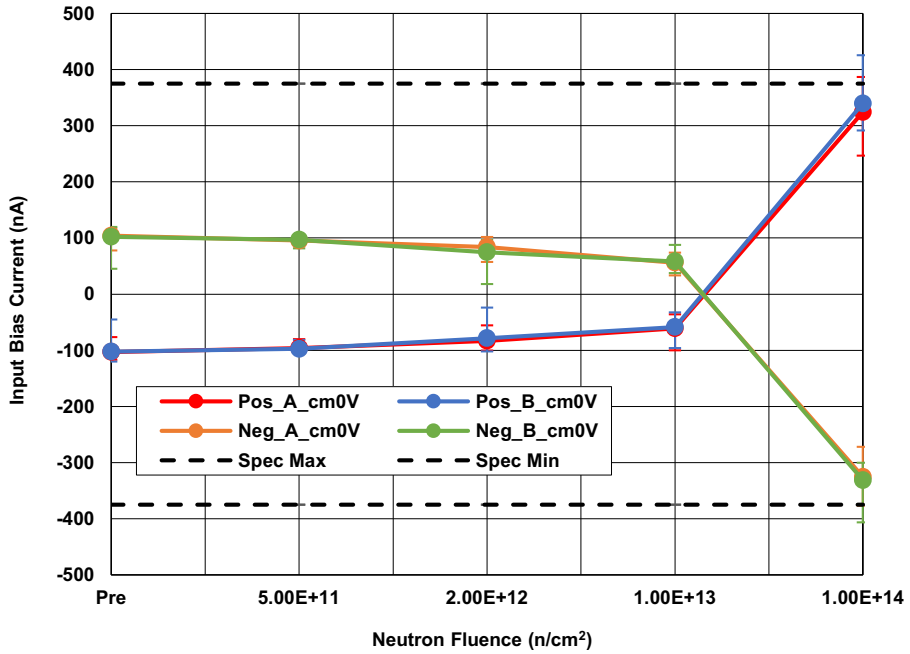

Figure 18. ISL7x244SEH input bias current (I_B) at V_S = ±1.35V and V_{CM} = 0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -375nA minimum and 375nA maximum

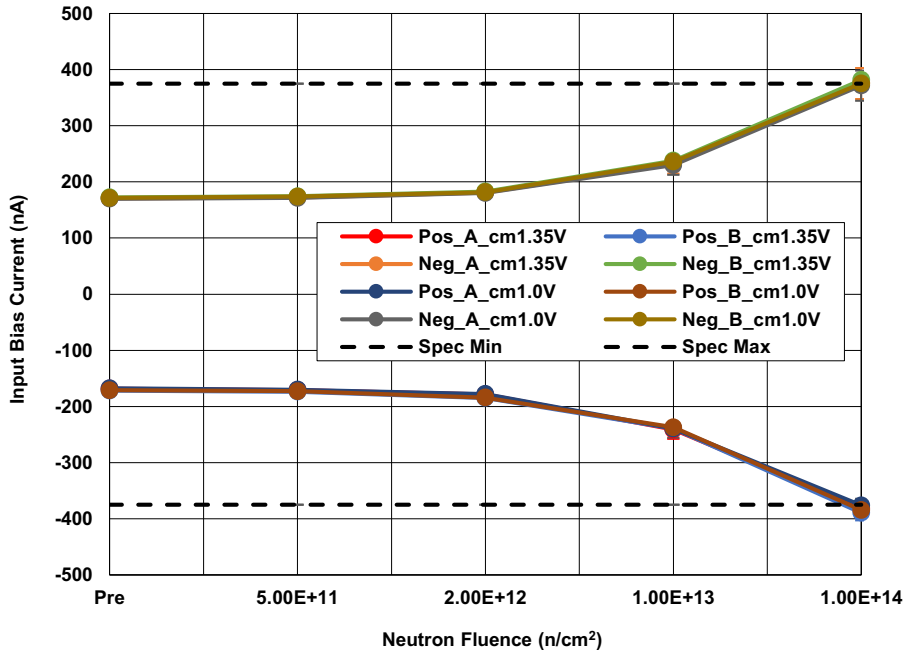

Figure 19. ISL7x244SEH input bias current (I_B) at V_S = ±1.35V and V_{CM} = +1.0V and +1.35V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -375nA minimum and 375nA maximum.

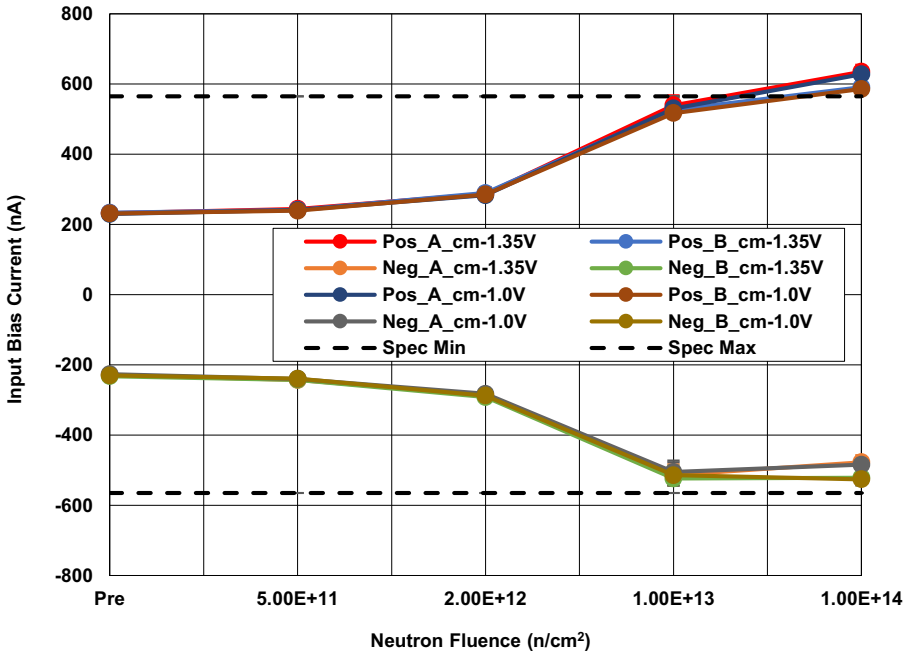

Figure 20. ISL7x244SEH input bias current (I_B) at V_S = ±1.35V and V_{CM} = -1.0V and -1.35V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -565nA minimum and 565nA maximum.

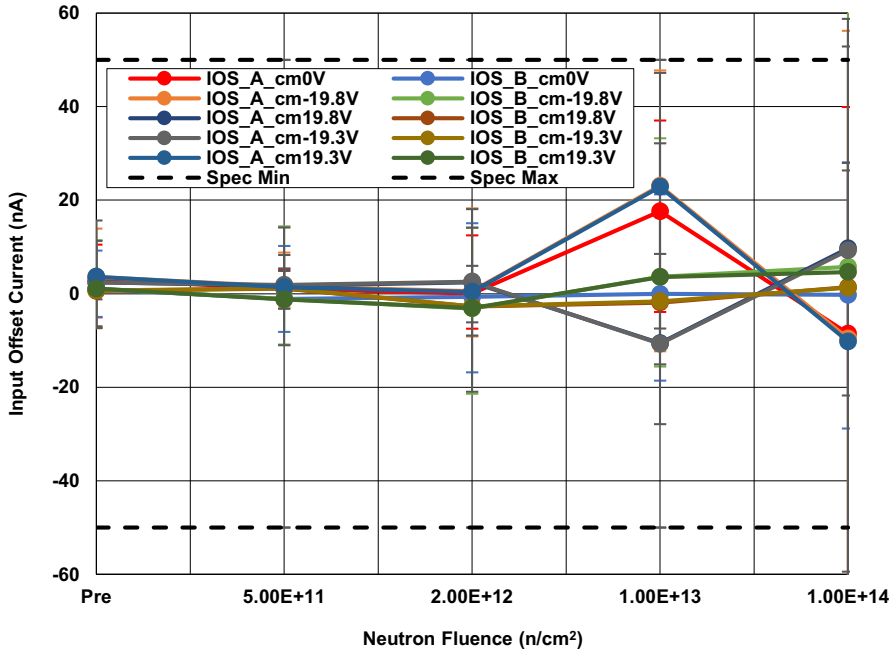

Figure 21. ISL7x244SEH input offset current (I_{OS}) at V_S = ±19.8V and V_{CM} = 0V, ±19.3V and ±19.8V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -50nA minimum and 50nA maximum.

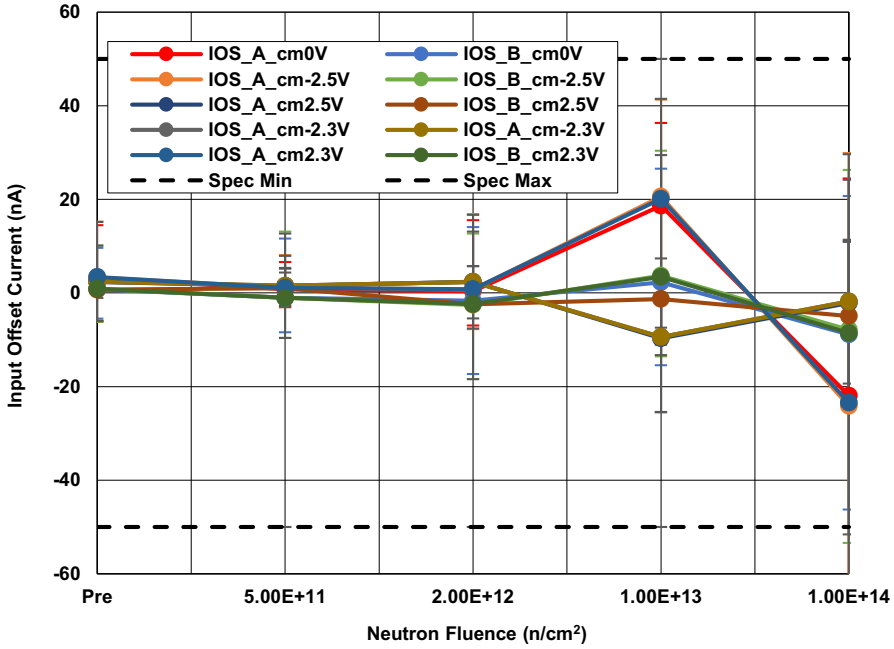

Figure 22. ISL7x244SEH input offset current (I_{OS}) at V_S = ±2.5V and V_{CM} = 0V, ±2.3V and ±2.5V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -50nA minimum and 50nA maximum.

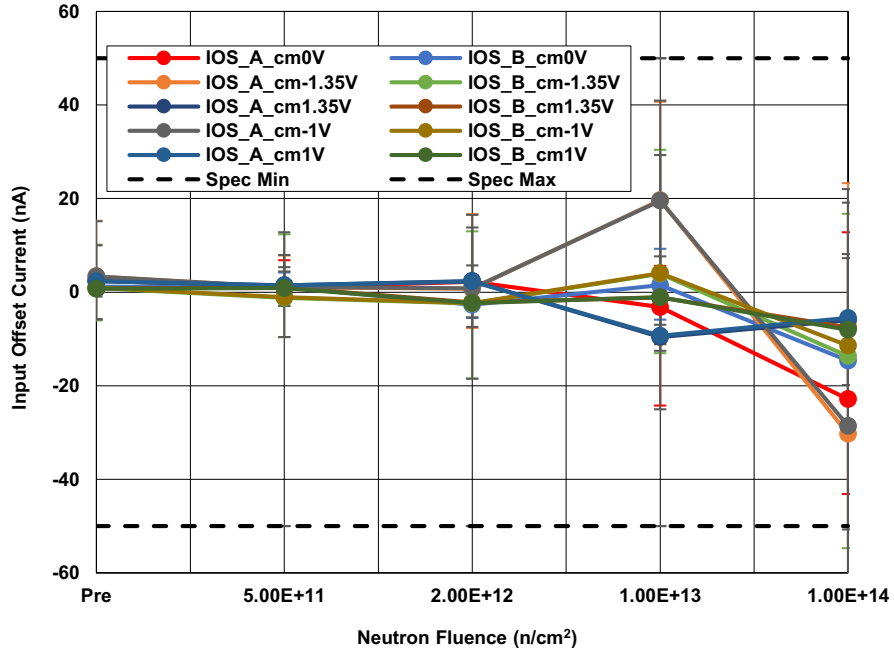

Figure 23. ISL7x244SEH input offset current (I_{OS}) at V_S = ±1.35V and V_{CM} = 0V, ±1.0V and ±1.35V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -50nA minimum and 50nA maximum.

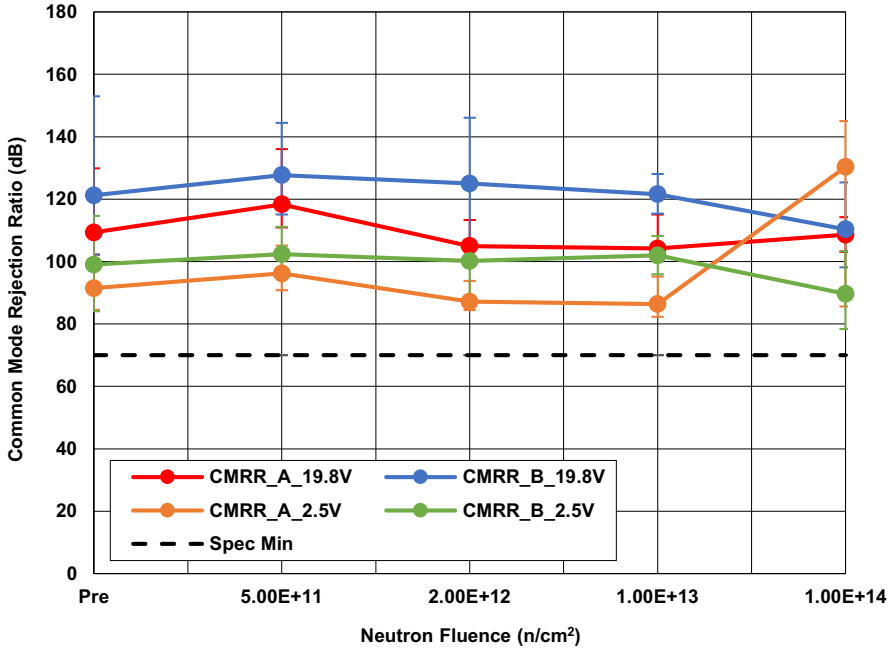

Figure 24. ISL7x244SEH Common Mode Rejection Ratio (CMRR) at V_S = ±2.5V and ±19.8V and V_{CM} = -V_S to +V_S following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 70dB minimum.

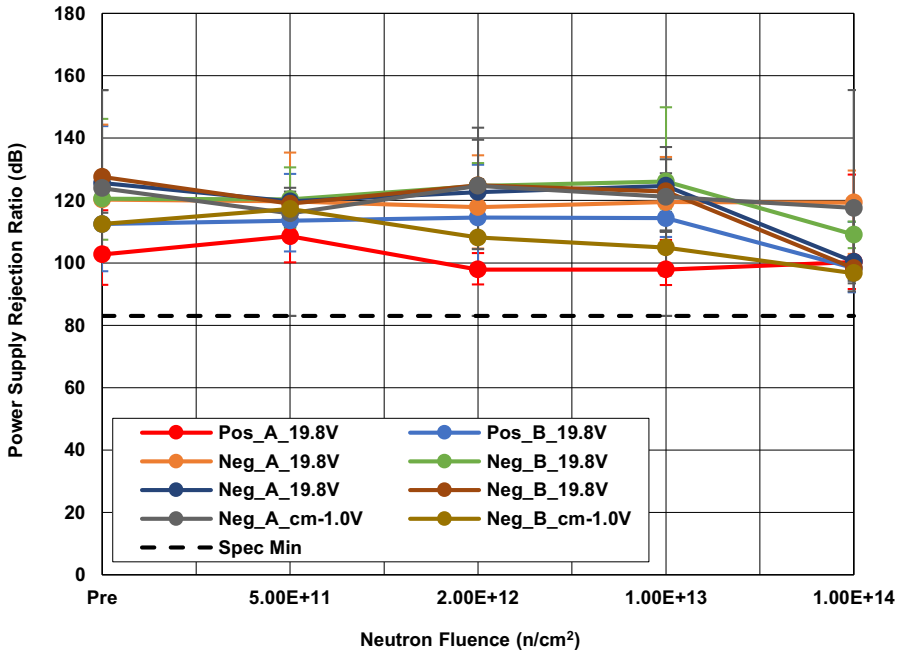

Figure 25. ISL7x244SEH Power Supply Rejection Ratio (PSRR) at V_S = ±18V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 83dB minimum.

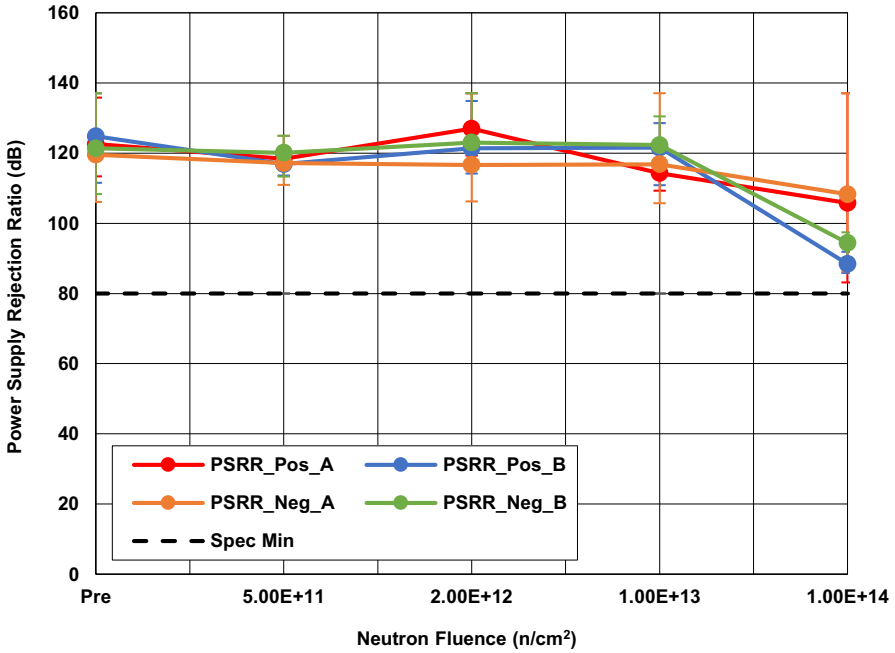

Figure 26. ISL7x244SEH power supply rejection ratio (PSRR) at V_S = ±2.5V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 80dB minimum.

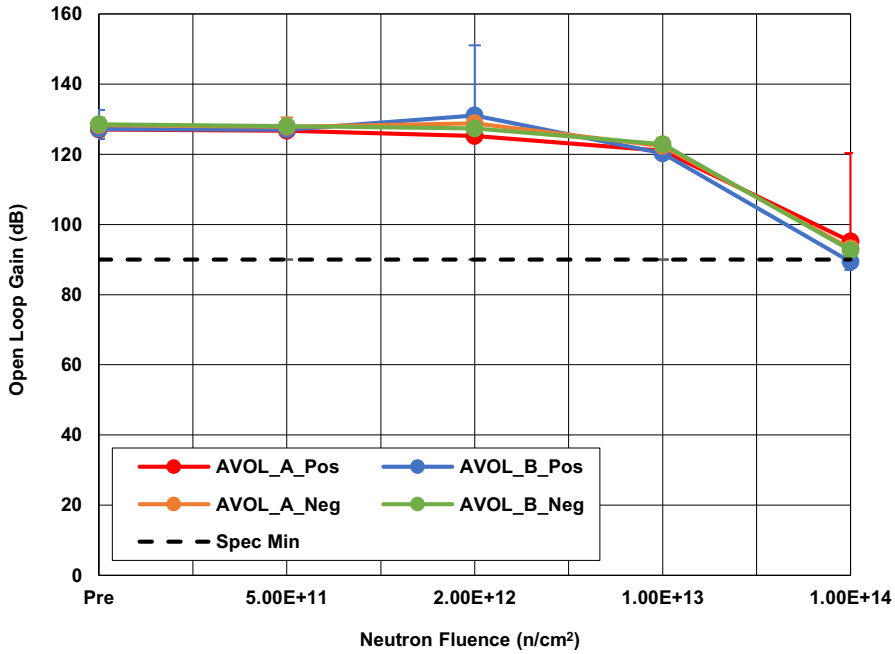

Figure 27. ISL7x244SEH open loop gain (A_{VOL}) at V_S = ±19.8V and R_L = 10kΩ to ground following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 90dB minimum.

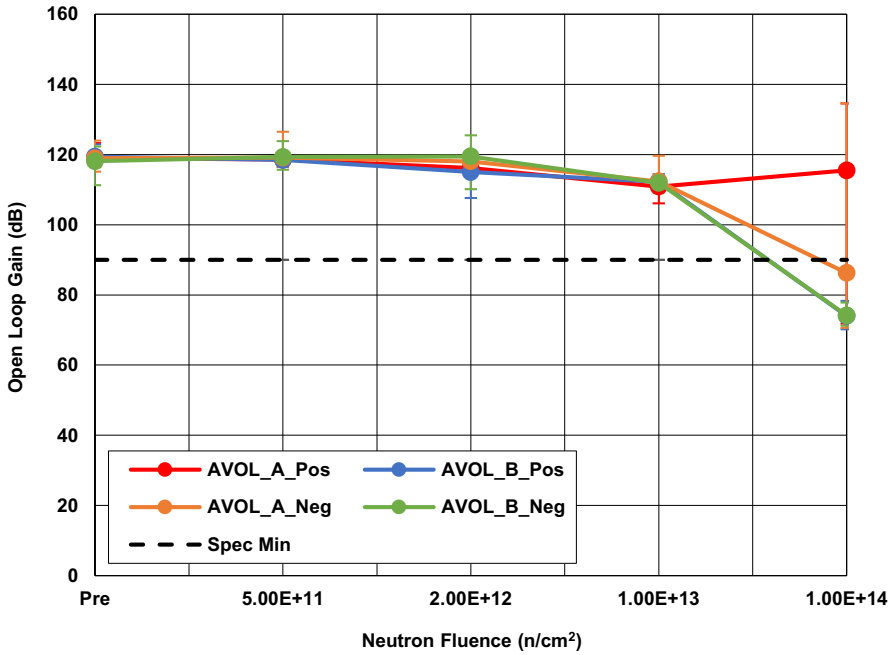

Figure 28. ISL7x244SEH open loop gain (A_{VOL}) at V_S = ±2.5V and R_L = 10kΩ to ground following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 90dB minimum.

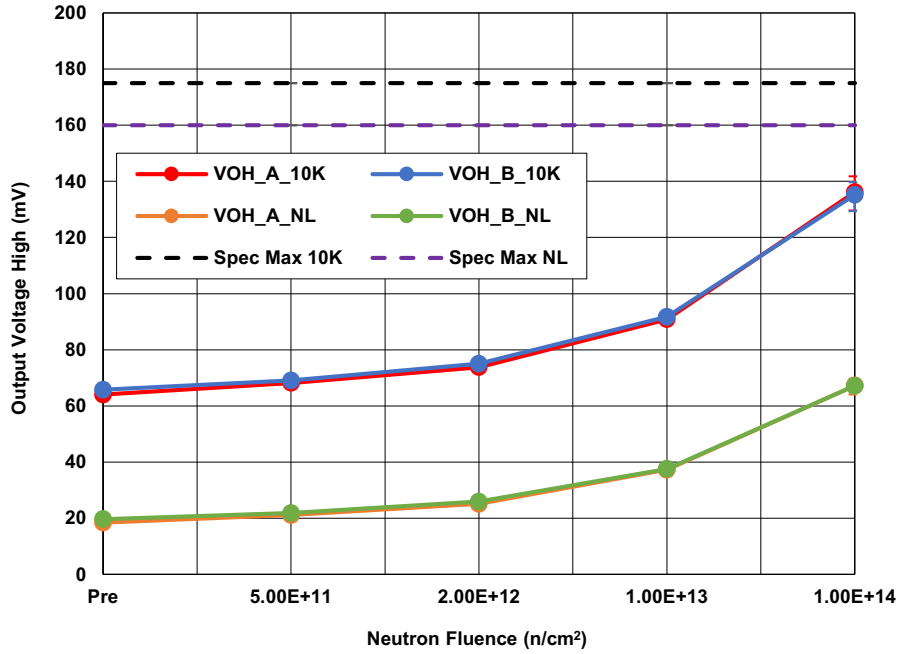

Figure 29. ISL7x244SEH output voltage high (V_{OH}) at V_S = ±19.8V and R_L = 10kΩ to ground and No Load (NL) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 175mV maximum for R_L = 10kΩ and 160mV maximum for NL.

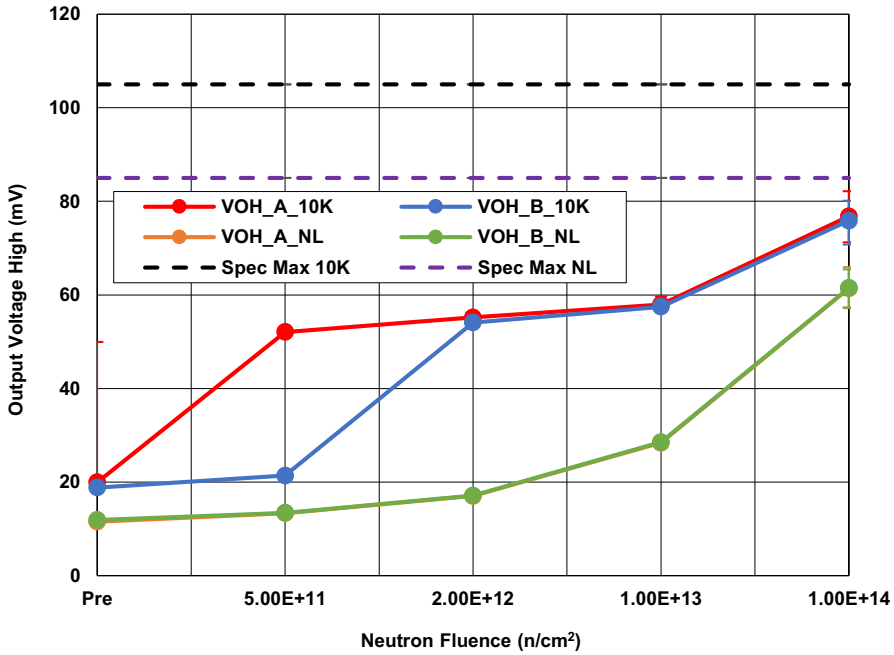

Figure 30. ISL7x244SEH output voltage high (V_{OH}) at V_S = ±2.5V and R_L = 10kΩ to ground and No Load (NL) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 105mV maximum for R_L = 10kΩ and 85mV maximum for NL.

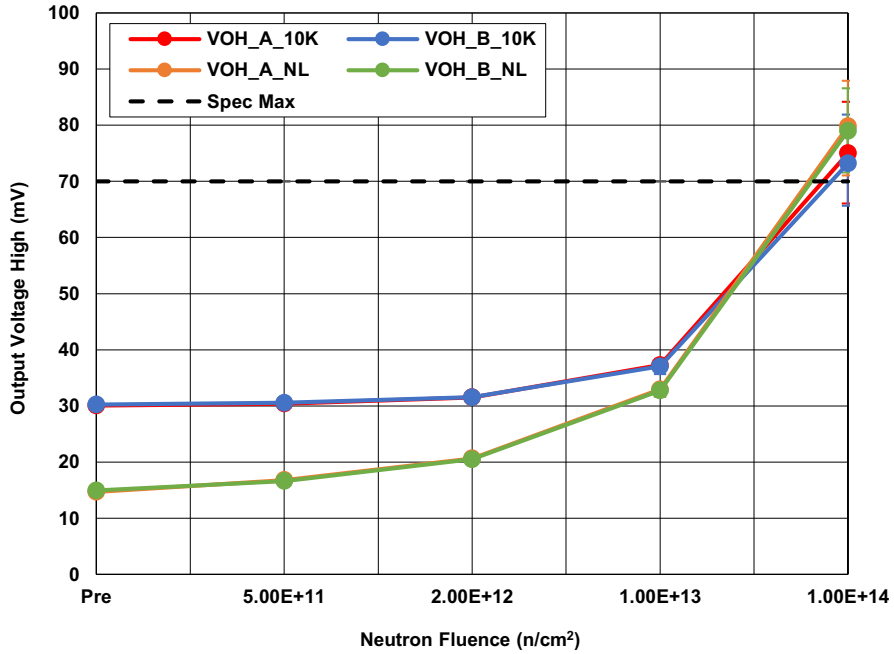

Figure 31. ISL7x244SEH output voltage high (V_{OH}) at V_S = ±1.35V and R_L = 10kΩ to ground and No Load (NL) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 70mV maximum for R_L = 10kΩ and NL.

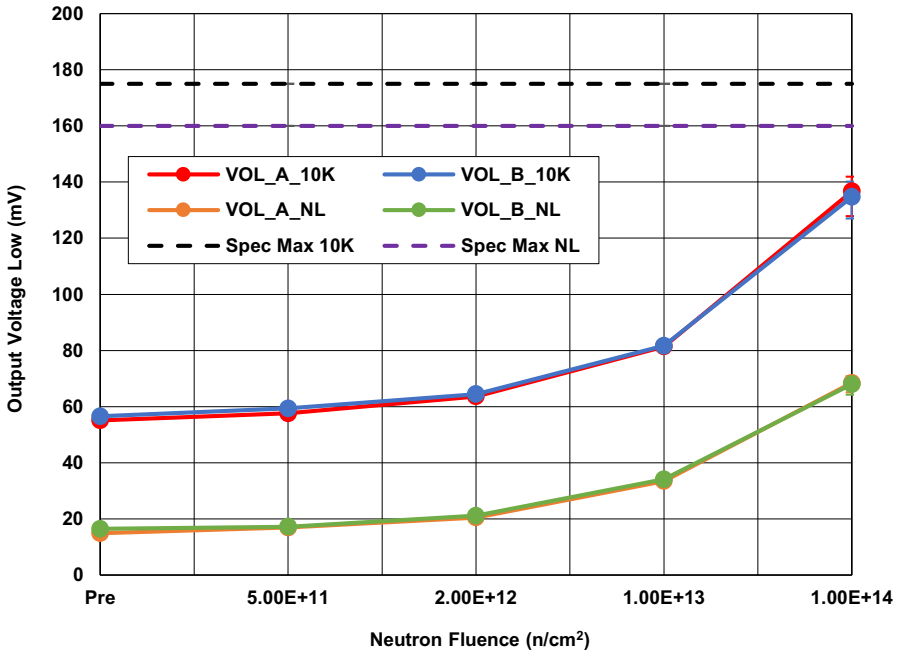

Figure 32. ISL7x244SEH output voltage low (V_{OL}) at V_S = ±19.8V and R_L = 10kΩ to ground and No Load (NL) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 175mV maximum for R_L = 10kΩ and 160mV maximum for NL.

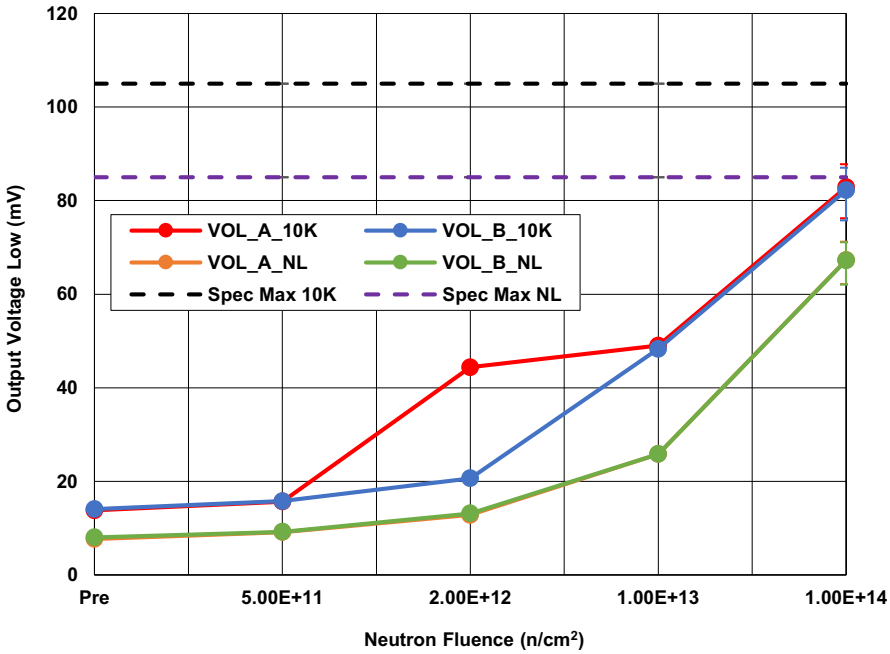

Figure 33. ISL7x244SEH output voltage low (V_{OL}) at V_S = ±2.5V and R_L = 10kΩ to ground and No Load (NL) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 105mV maximum for R_L = 10kΩ and 85mV maximum for NL.

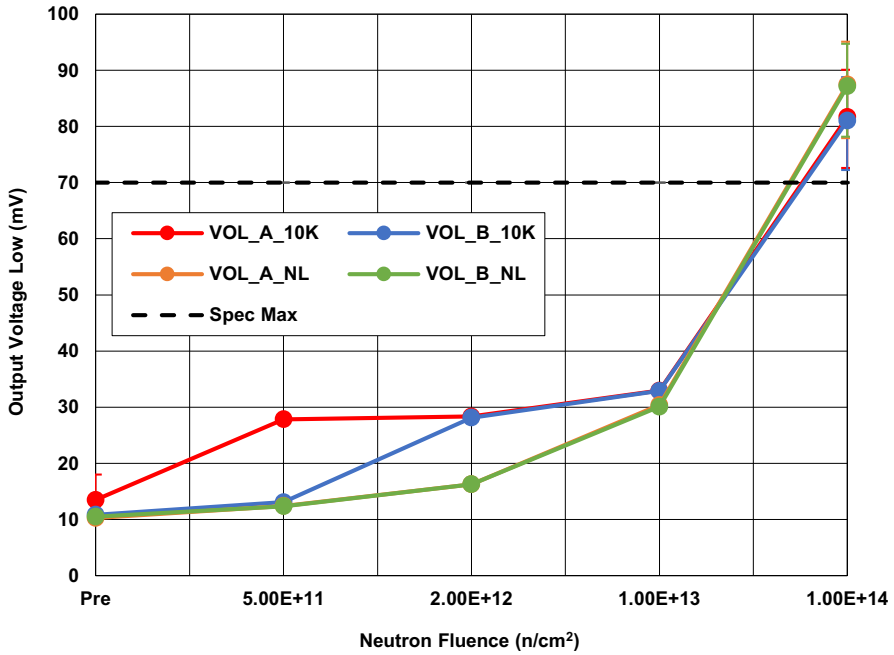

Figure 34. ISL7x244SEH output voltage low (V_{OL}) at V_S = ±1.35V and R_L = 10kΩ to ground and No Load (NL) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 70mV maximum for R_L = 10kΩ and NL.

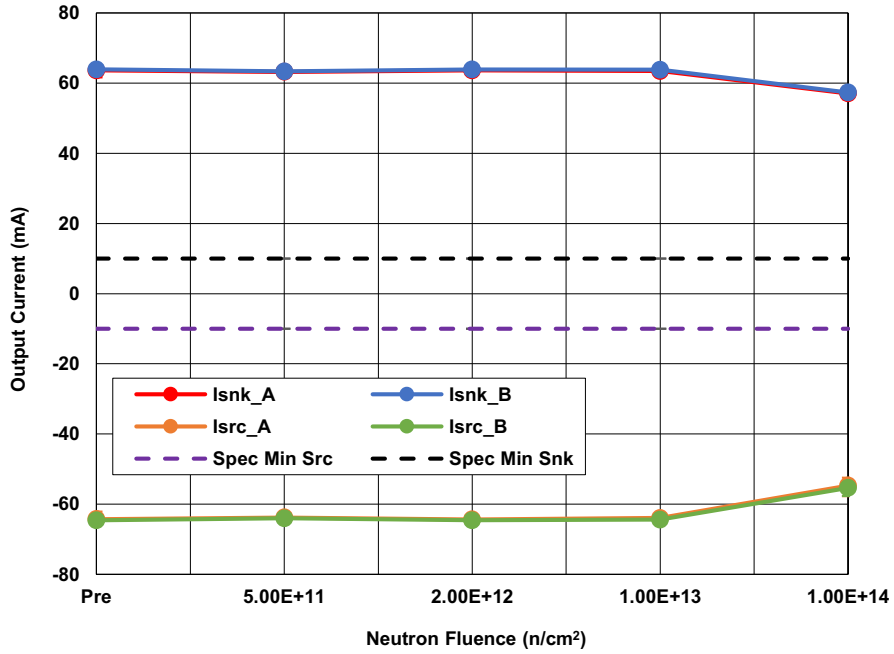

Figure 35. ISL7x244SEH output short circuit current (I_{SC}), sourcing and sinking at V_S = ±19.8V and V_{OUT} = -18V sourcing and +18V sinking, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are -10mA minimum (sourcing) and 10mA minimum (sinking).

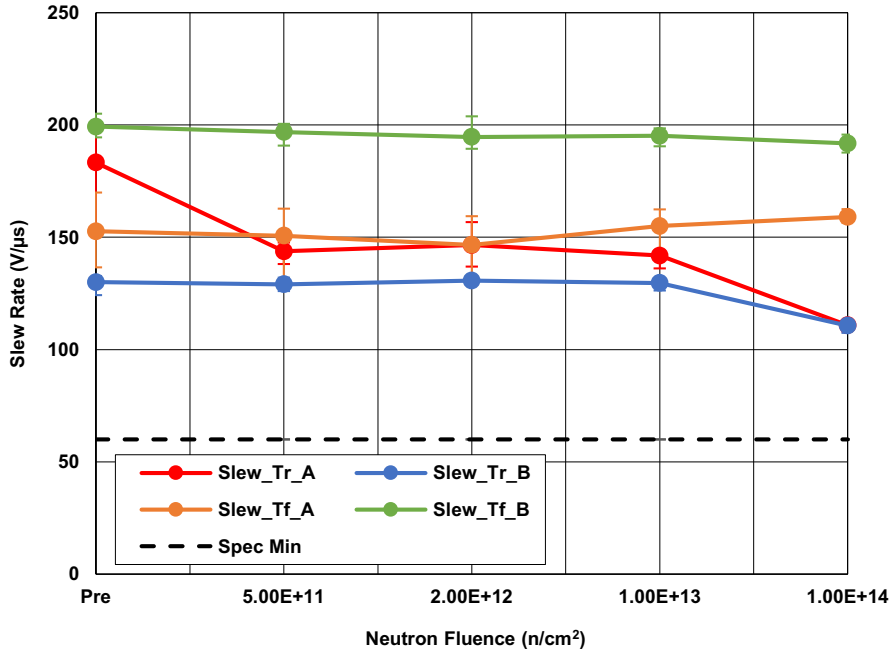

Figure 36. ISL7x244SEH slew rate (SR) at V_S = ±19.8V and A_V = 1, R_L = 10kΩ to ground and V_O = 10V_{PP} following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 60V/µs minimum.

3. Discussion and Conclusion

This document reports the results of 1MeV equivalent neutron testing of the ISL7x244SEH radiation hardened 40V dual rail-to-rail input-output, low-power operational amplifier. Parts were tested at 5.2x10^{11}n/cm^2, 1.9x10^{12}n/cm^2, 9.9x10^{12}n/cm^2 and 8.6x10^{13}n/cm^2. The results of key parameters before and after irradiation to each level are plotted in Figures 1 through 36. The plots show the mean of each parameter as a function of neutron irradiation, with error bars that represent the minimum and maximum measured values. The figures also show the applicable electrical limits taken from the SMD, but it should be noted that these limits are provided for guidance only as the ISL7x244SEH is not specified for the neutron environment.

All samples passed the post-irradiation SMD limits after all exposures up to and including 1.9x10^{12}n/cm^2, but all five tested units failed the SMD post-irradiation limits for input bias (I_B) at 2.5V (Figure 15) after 9.9x10^{12}n/cm^2 and some or all units failed measurements for input offset voltage (V_{OS}), input bias (I_B), open loop gain (A_{VOL}), power supply rejection ratio (PSRR), output voltage high (V_{OH}) and output voltage low (V_{OL}) after 8.6x0^{13}n/cm^2. Several of the V_{OS} measurements clamped the ATE at 509µV.

4. Appendices

4.1 Reported Parameters

Fig.	Parameter	Symbol	Limit, Low	Limit, High	Units	Notes
1	Supply current, V_S = ±19.8V	I_{SVN}	-4.4		mA	Sum of both channels
		I_{SVP}		4.4		
2	Supply current, V_S = ±1.35V, ±2.5V	I_{SVN}	-3		mA	Sum of both channels
		I_{SVP}		3		
3	Input offset voltage, V_{CM} = 0V, ±19.8V	V_{OS}	-500	500	µV	V_S = ±19.8V
4	Input offset voltage, V_{CM} = ±19.3V					
5	Input offset voltage, V_{CM} = 0V, ±2.5V	V_{OS}	-500	500	µV	V_S = ±2.5V
6	Input offset voltage, V_{CM} = ±2.0V					

Fig.	Parameter	Symbol	Limit, Low	Limit, High	Units	Notes
7	Input offset voltage, V_{CM} = 0V, ±1.35V	V_{OS}	-500	500	µV	V_S = ±1.35V
8	Input offset voltage, V_{CM} = ±1.0V					
9	Offset voltage match, V_{CM} = ±19.3V, ±19.8V	ΔV_{OS}	-800	800	µV	V_S = ±19.8V
10	Offset voltage match, V_{CM} = ±2.0V, ±2.5V					V_S = ±2.5V
11	Offset voltage match, V_{CM} = ±1.0V, ±1.35V					V_S = ±1.35V
12	Input bias current, V_{CM} = 0V	I_B	-500	500	nA	V_S = ±19.8V
13	Input bias current, V_{CM} = +19.3V, +19.8V					
14	Input bias current, V_{CM} = -19.3V, -19.8V		-650	650		
15	Input bias current, V_{CM} = 0V	I_B	-400	400	nA	V_S = ±2.5V
16	Input bias current, V_{CM} = +2.0V, +2.5V					
17	Input bias current, V_{CM} = -2.0V, -2.5V		-580	580		
18	Input bias current, V_{CM} = 0V	I_B	-375	375	nA	V_S = ±1.35V
19	Input bias current, V_{CM} = +1.0V, +1.35V					
20	Input bias current, V_{CM} = -1.0V, -1.35V		-565	565		
21	Input offset current, V_{CM} = 0V, ±19.3V, ±19.8V	I_{OS}	-50	50	nA	V_S = ±19.8V
22	Input offset current, V_{CM} = 0V, ±2.3V, ±2.5V	I_{OS}	-50	50	nA	V_S = ±2.5V
23	Input offset current, V_{CM} = 0V, ±1.0V, ±1.35V	I_{OS}	-50	50	nA	V_S = ±1.35V
24	Common-mode rejection ratio, V_{CM} = $-V_S$ to $+V_S$	CMRR	70	-	dB	V_S = ±2.5V, ±19.8V
25	Power supply rejection ratio	PSRR	83	-	dB	V_S = ±18V
26			80			V_S = ±2.5V
27	Open loop gain, R_L = 10kΩ to ground	A_{VOL}	90	-	dB	V_S = ±19.8V
28						V_S = ±2.5V
29	Output voltage high, V_S = ±19.8V	V_{OH}	-	175	mV	R_L = 10kΩ
				160		R_L = NL
30	Output voltage high, V_S = ±2.5V	V_{OH}	-	105	mV	R_L = 10kΩ
				85		R_L = NL
31	Output voltage high, V_S = ±1.35V	V_{OH}	-	70	mV	R_L = NL or 10kΩ
32	Output voltage low, V_S = ±19.8V	V_{OL}	-	175	mV	R_L = 10kΩ
				160		R_L = NL
33	Output voltage low, V_S = ±2.5V	V_{OL}	-	105	mV	R_L = 10kΩ
				85		R_L = NL
34	Output voltage low, V_S = ±1.35V	V_{OL}	-	70	mV	R_L = NL or 10kΩ
35	Output short-circuit current, sourcing	I_{SC}	-10	-	mA	V_{OUT} = -18 V
	Output short-circuit current, sinking		10	-		V_{OUT} = +18 V
36	Slew rate, A_V = 1, R_L = 10kΩ, V_O = $10V_{PP}$	SR	60	-	V/µs	V_S = ±19.8V

5. Revision History

Rev.	Date	Description
1.00	Apr.30.20	Initial release

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