
ISL70444SEH, ISL73444SEH

Total Dose Testing of the ISL70444SEH and ISL73444SEH Radiation Hardened Quad Operational Amplifiers

Introduction and Executive Summary

This document reports the results of low dose rate (LDR) and high dose rate (HDR) total dose testing of the [ISL70444SEH](#) and [ISL73444SEH](#) (ISL7x444SEH) quad operational amplifiers. The tests were conducted to provide an assessment of the total dose hardness of the part. Parts were irradiated under bias and with all pins grounded at LDR and under bias at HDR. The HDR samples were also taken out to the 50% overtest and subsequent anneal as described in MIL-STD-883 Test Method 1019. The anneal was performed under bias at an ambient temperature of 100°C for 168 hours.

The ISL70444SEH is specified to total dose levels of 300krad(Si) at HDR (50-300rad(Si)/s) and of 50krad(Si) at LDR (0.01rad(Si)/s). The ISL73444SEH is specified to 50krad(Si) at LDR (0.01rad(Si)/s) only. The ISL70444SEH is acceptance tested on a wafer-by-wafer basis to 300krad(Si) at HDR (50-300rad(Si)/s) and to 50krad(Si) at LDR (0.01rad(Si)/s), while the ISL73444SEH is acceptance tested on a wafer-by-wafer basis to 50krad(Si) at LDR (0.01rad(Si)/s).

Given the excellent performance shown in the attributes and variables data, and in particular the stability shown by the key positive and negative input bias current parameters, the part is not considered dose rate sensitive. No significant differences in total dose response were noted between biased and grounded irradiation for any parameters, and all channels maintained variations within established limits in the pre-irradiation data or in the total dose response of the parts.

Part Description

The ISL7x444SEH features four low-power operational amplifiers optimized to provide maximum dynamic range. These op amps feature a unique combination of rail to rail operation on the input and output as well as a slew enhanced front end, providing ultra fast slew rates that are proportional to a given step size, increasing accuracy under transient conditions. The part also offers low power, low input offset voltage and low temperature drift, making it ideal for applications requiring both high DC accuracy and AC performance. With <math><5\mu\text{s}</math> recovery from single event transients (SET) at an LET of 86.4MeV.cm²/mg), the number of filtering components needed is drastically reduced. The ISL7x444SEH is also immune to single event latch-up (SEL) as it is fabricated in the Renesas proprietary PR40 silicon on insulator (SOI) process. The part is designed to operate over a single supply range of 2.7V to 40V or a split supply voltage range of $\pm 1.35\text{V}$ to $\pm 20\text{V}$. Applications for these amplifiers include precision payload instrumentation, data acquisition and precision power supply controls. The ISL7x444SEH is available in a 14 lead hermetic ceramic flatpack and in die form. The ISL7x444SEH offers guaranteed performance over the full -55°C to +125°C military temperature range. Key pre- and post-radiation specifications follow, with parametric limits shown for $\pm 18\text{V}$ supplies.

- Input offset voltage: $\pm 400\mu\text{V}$ post-irradiation
- Input offset voltage TC: 0.5 $\mu\text{V}/^\circ\text{C}$ typical
- Input bias current: 370nA post-irradiation
- Supply current, per channel: 2.4mA post-irradiation
- Gain-bandwidth product: 19MHz typical
- Slew rate: 60V/ μs post-irradiation
- Operating temperature range: -55°C to +125°C

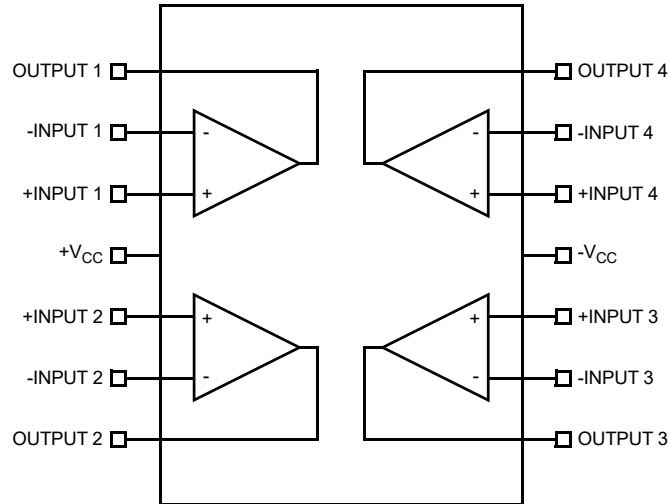


Figure 1. ISL7x444SEH Block Diagram

Reference Documents

- MIL-STD-883 test method 1019
- [ISL70444SEH, ISL73444SEH Datasheet](#)
- Standard Microcircuit Drawing (SMD) 5962–13214

Contents

1. Test Description	3
1.1 Irradiation Facilities	3
1.2 Test Fixturing	3
1.3 Characterization Equipment and Procedures	3
1.4 Experimental Matrix	3
1.5 Downpoints	3
2. Results	4
2.1 Test Results	4
2.2 Variables Data	4
2.3 Data Plots	5
3. Discussion and Conclusion	12
4. Appendix	13
5. Revision History	13

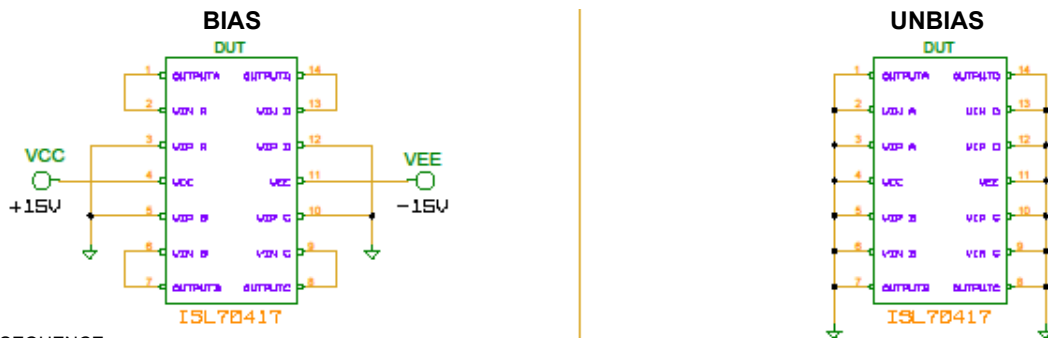
1. Test Description

1.1 Irradiation Facilities

HDR testing was performed at 69.7rad(Si)/s using a Gammacell 220 irradiator located in the Palm Bay, Florida Renesas facility. LDR testing was performed at 0.01rad(Si)/s using the Renesas Palm Bay N40 panoramic irradiator. The post-HDR biased anneal operation was performed in a small temperature chamber.

1.2 Test Fixturing

Figure 2 shows the configuration and power supply sequencing used for biased irradiation. The grounded irradiations were performed in the same fixture type with all pins hardwired to ground.



POWER-UP SEQUENCE:
Bring up -1V supply, then +15V supply with ±5% tolerance.

POWER DOWN SEQUENCE:
Bring down +1V supply, then -15V supply.

Figure 2. Biased and Unbiased (Grounded) Irradiation Bias Configurations for the ISL7x444SEH. The figure shown is for the ISL70417SEH quad operational amplifier, and the ISL7x444SEH uses the identical configuration.

1.3 Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using the production automated test equipment (ATE) with datalogging at each downpoint. Downpoint electrical testing was performed at room temperature. Three control units were used to improve repeatability.

1.4 Experimental Matrix

The experimental matrix consisted of five samples irradiated at LDR under bias, five samples irradiated at LDR with all pins grounded and five samples irradiated at HDR under bias. Samples of the ISL70444SEH were drawn from preproduction lot WW6XEH and were packaged in the hermetic 14-pin solder-sealed ceramic flatpack (K14.C) package. Samples were processed through the standard burn-in cycle before irradiation, as required by MIL-STD-883, and were screened to the ATE limits at room temperature prior to the test.

1.5 Downpoints

Downpoints for the LDR tests were zero, 25, 50, and 100krad(Si). Downpoints for the HDR tests were 0, 300, and 450krad(Si) followed by a 168 hour anneal under bias at 100°C.

2. Results

2.1 Test Results

Testing at low and HDR of the ISL7x444SEH is complete. [Table 1](#) shows the attributes data for the test.

Table 1. ISL70444SEH Total Dose Test Attributes Data

Dose Rate	Bias	Sample Size	Downpoint ^[1]	Bin 1 ^[2]	Rejects
0.01rad(Si)/s	Figure 2	5	0	5	0
			25krad(Si)	5	0
			50krad(Si)	5	0
			100krad(Si)	5	0
			Biased anneal, 168h at 100°C	5	0
0.01rad(Si)/s	Grounded	5	0	5	0
			25krad(Si)	5	0
			50krad(Si)	5	0
			100krad(Si)	5	0
			Biased anneal, 168h at 100°C	5	0
69.7rad(Si)/s	Figure 2	5	0	5	0
			300krad(Si)	5	0
			450krad(Si)	5	0
			Biased anneal, 168h at 100°C	5	0

1. The 168-hour anneal was performed at 100°C under bias as shown in [Figure 2](#).
2. Bin 1 indicates a device that passes all pre-irradiation specification limits.

2.2 Variables Data

The plots in [Figure 3](#) through [Figure 16](#) show data at all downpoints including the post-anneal data. The plots show the response for supply voltages of +18.0V and -18.0V as a function of total dose irradiation at LDR for the biased (per [Figure 2](#)) and unbiased (all pins grounded) cases and at HDR for the biased ([Figure 2](#)) case. In addition, the plots show the response of all samples to a post-irradiation anneal at 100°C for 168 hours. The plots have an unconventional scale for the x-axis in order to better show the LDR response of the parts. We chose to plot the median for these parameters due to the relatively small sample size of five or six per experimental cell. [Discussion and Conclusion](#) provides individual discussion of the figures. No differences in total dose response were noted between biased and grounded irradiation for any parameters. Additionally, no channel-to-channel differences were noted, either in the pre-irradiation data or in the total dose response of the parts.

2.3 Data Plots

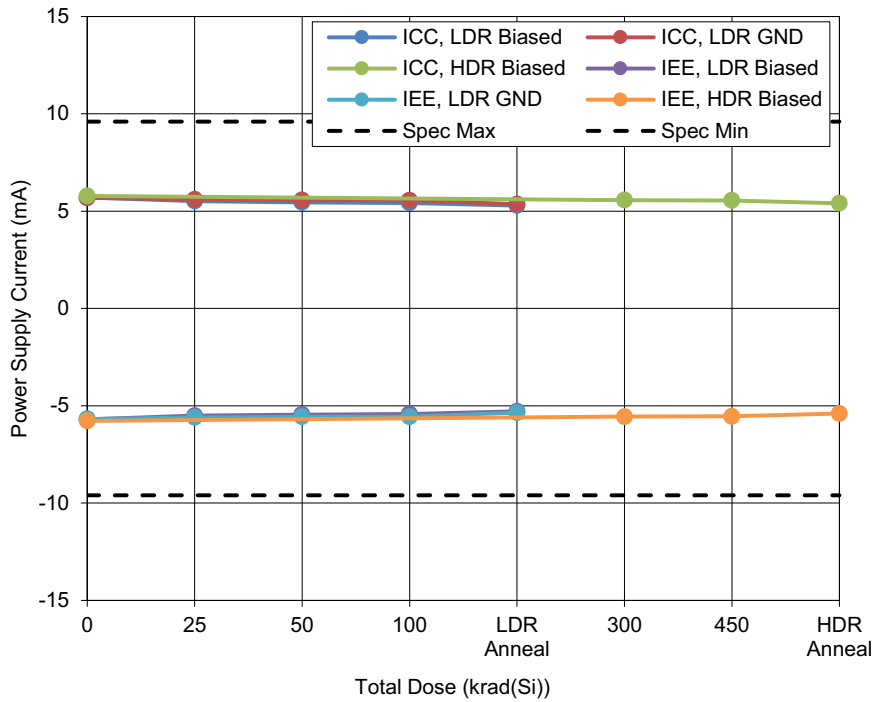


Figure 3. ISL7x444SEH power supply current, sum of all four channels at supply voltages of +18.0V and -18.0V, as a function of total dose irradiation at LDR for the biased (per Figure 2) and unbiased (all pins grounded) cases and at HDR for the biased (Figure 2) case. The LDR was 0.01rad(Si)/s and the HDR was 69.7rad(Si)/s. HDR and LDR irradiations were followed by a 168-hour biased anneal at 100°C. The sample size for the two LDR cells and the HDR cell was five for each cell. The SMD specification limits are +9.6mA (positive supply) and -9.6mA (negative supply).

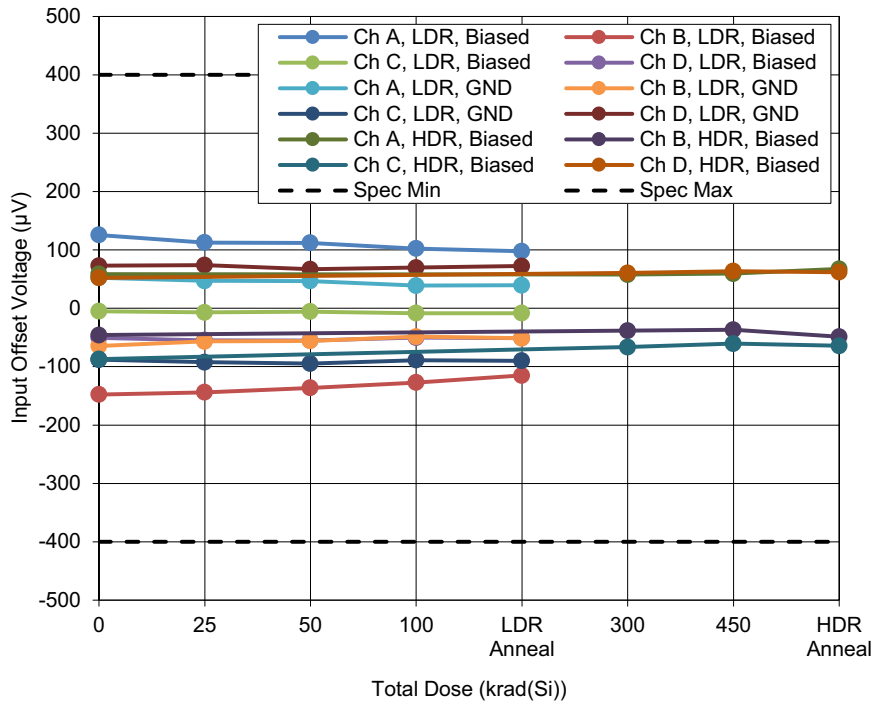


Figure 4. ISL7x444SEH input offset voltage, channels A through D, as a function of total dose irradiation at LDR for the biased (per Figure 2) and unbiased (all pins grounded) cases and at HDR for the biased (Figure 2) case. The LDR was 0.01rad(Si)/s and the HDR was 69.7rad(Si)/s. HDR and LDR irradiations were followed by a 168-hour biased anneal at 100°C. The sample size for the two LDR cells and the HDR cell was five for each cell. The SMD specification limits are -400µV to +400µV.

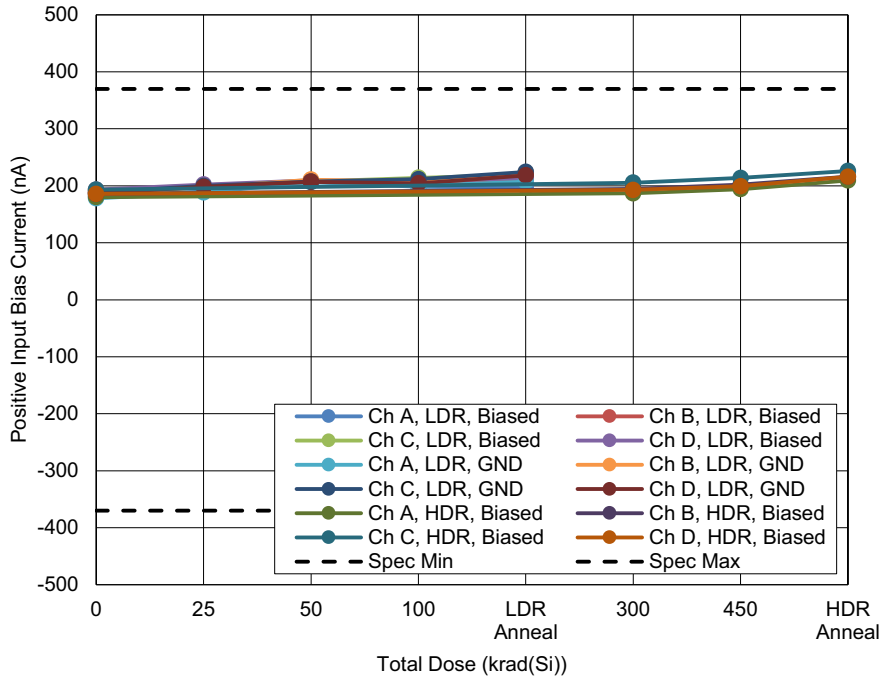


Figure 5. ISL7x444SEH positive input bias current, channels A through D, as a function of total dose irradiation at LDR for the biased (per Figure 2) and unbiased (all pins grounded) cases and at HDR for the biased (Figure 2) case. The LDR was 0.01rad(Si)/s and the HDR was 69.7rad(Si)/s. HDR and LDR irradiations were followed by a 168-hour biased anneal at 100°C. The sample size for the two LDR cells and the HDR cell was five for each cell. The SMD specification limits are -370nA to +370nA.

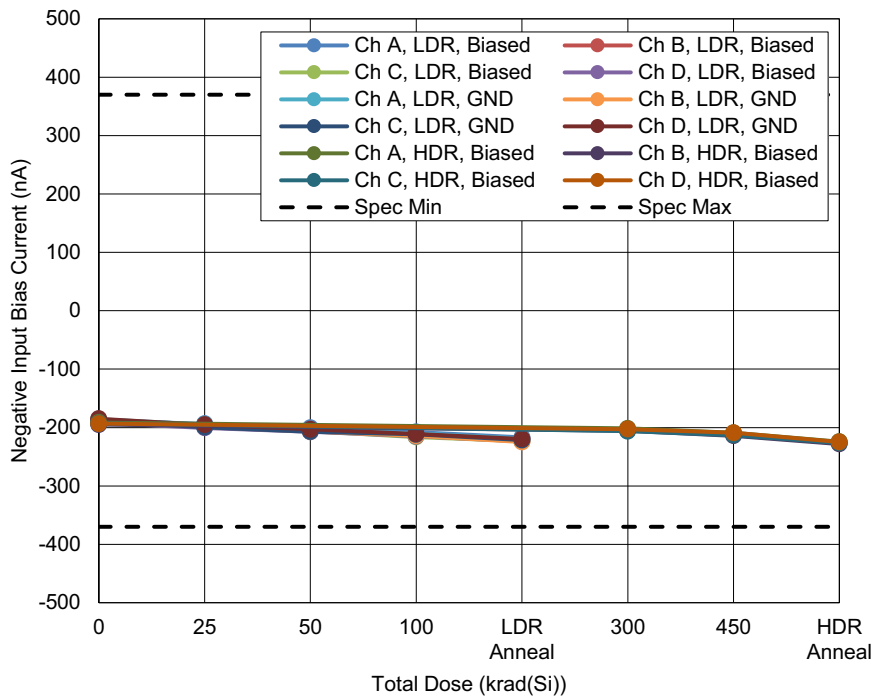


Figure 6. ISL7x444SEH negative input bias current, channels A through D, as a function of total dose irradiation at LDR for the biased (per Figure 2) and unbiased (all pins grounded) cases and at HDR for the biased (Figure 2) case. The LDR was 0.01rad(Si)/s and the HDR was 69.7rad(Si)/s. HDR and LDR irradiations were followed by a 168-hour biased anneal at 100°C. The sample size for the two LDR cells and the HDR cell was five for each cell. The SMD specification limits are -370nA to +370nA.

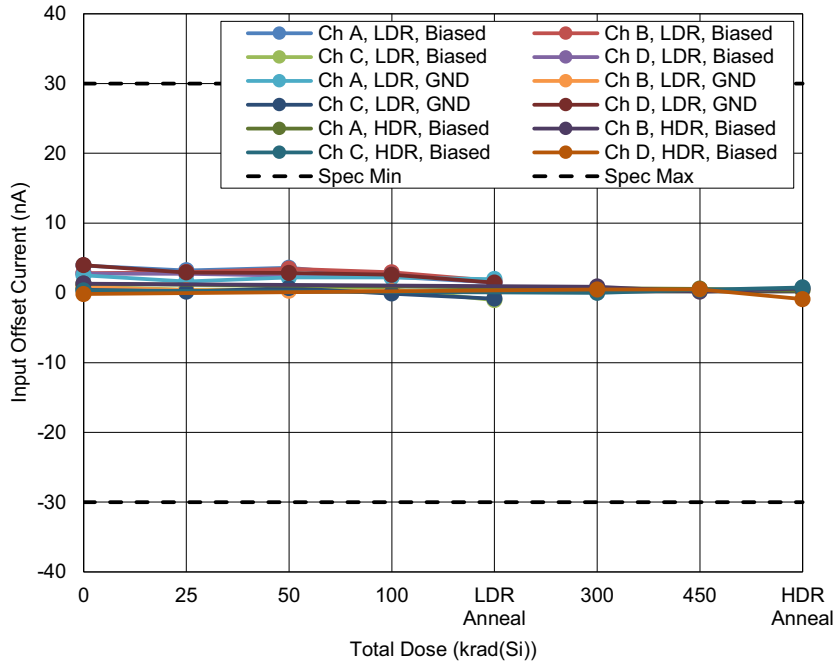


Figure 7. ISL7x444SEH input offset current, channels A through D, as a function of total dose irradiation at LDR for the biased (per Figure 2) and unbiased (all pins grounded) cases and at HDR for the biased (Figure 2) case. The LDR was 0.01rad(Si)/s and the HDR was 69.7rad(Si)/s. HDR and LDR irradiations were followed by a 168-hour biased anneal at 100°C. The sample size for the two LDR cells and the HDR cell was five for each cell. The SMD specification limits are -30nA to +30nA.

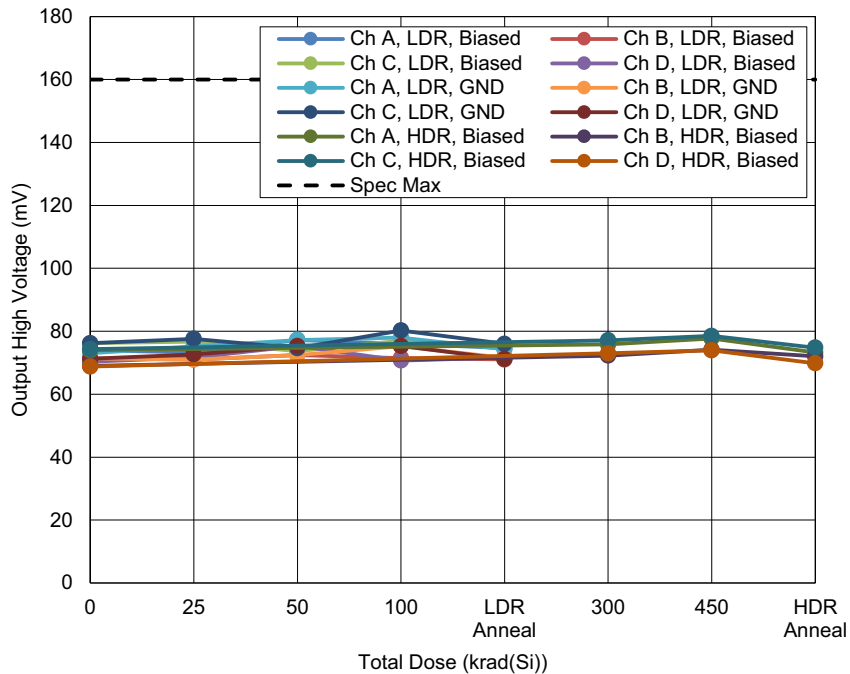


Figure 8. ISL7x444SEH output high voltage, channels A through D, as a function of total dose irradiation at LDR for the biased (per Figure 2) and unbiased (all pins grounded) cases and at HDR for the biased (Figure 2) case. The LDR was 0.01rad(Si)/s and the HDR was 69.7rad(Si)/s. HDR and LDR irradiations were followed by a 168-hour biased anneal at 100°C. The sample size for the two LDR cells and the HDR cell was five for each cell. The SMD specification limit is 160mV maximum.

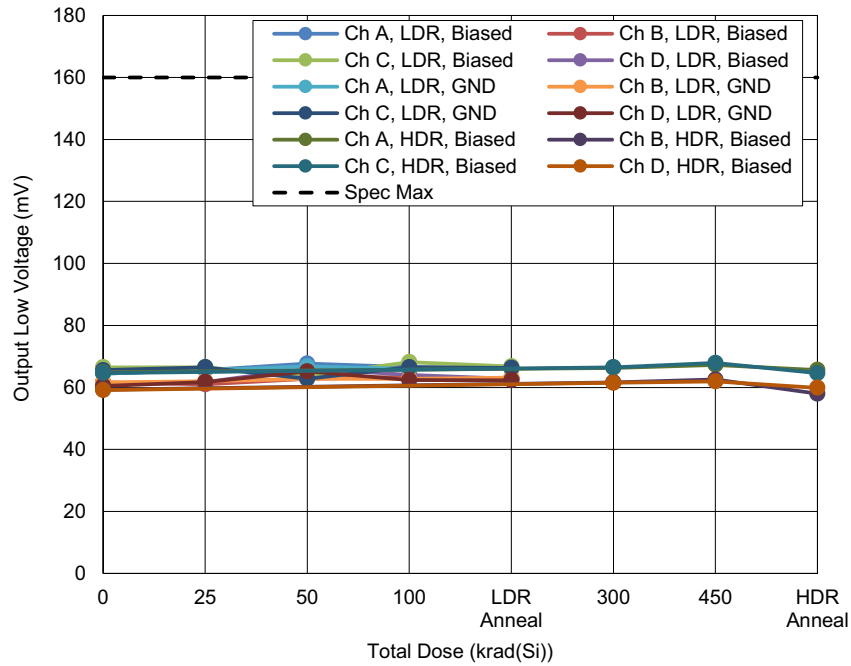


Figure 9. ISL7x444SEH output low voltage, channels A through D, as a function of total dose irradiation at LDR for the biased (per Figure 2) and unbiased (all pins grounded) cases and at HDR for the biased (Figure 2) case. The LDR was 0.01rad(Si)/s and the HDR was 69.7rad(Si)/s. HDR and LDR irradiations were followed by a 168-hour biased anneal at 100°C. The sample size for the two LDR cells and the HDR cell was five for each cell. The SMD specification limit is 160mV maximum.

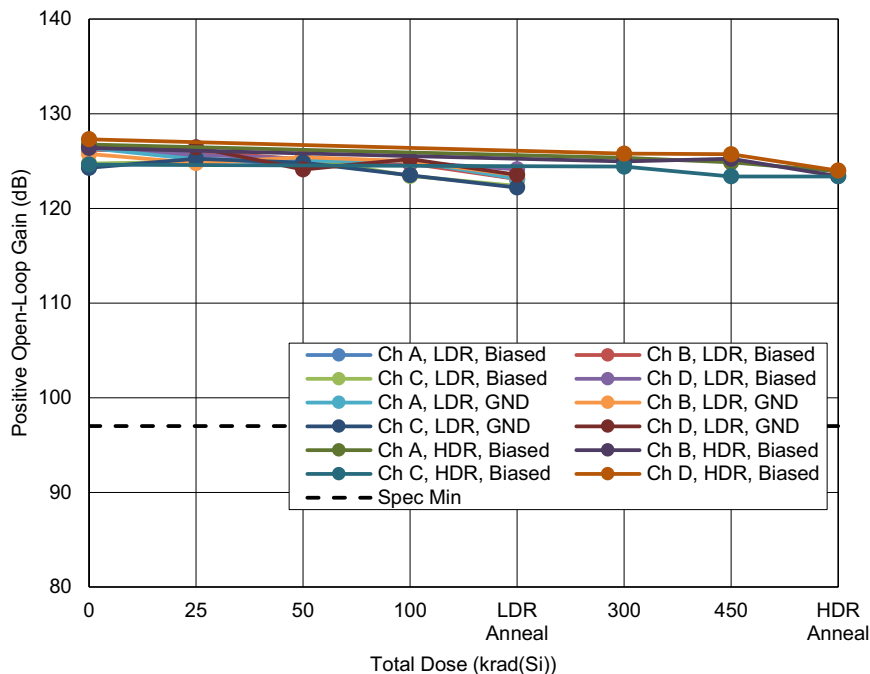


Figure 10. ISL7x444SEH positive open loop gain, channels A through D, as a function of total dose irradiation at LDR for the biased (per Figure 2) and unbiased (all pins grounded) cases and at HDR for the biased (Figure 2) case. The LDR was 0.01rad(Si)/s and the HDR was 69.7rad(Si)/s. HDR and LDR irradiations were followed by a 168-hour biased anneal at 100°C. The sample size for the two LDR cells and the HDR cell was five for each cell. The SMD specification limit is 97dB minimum.

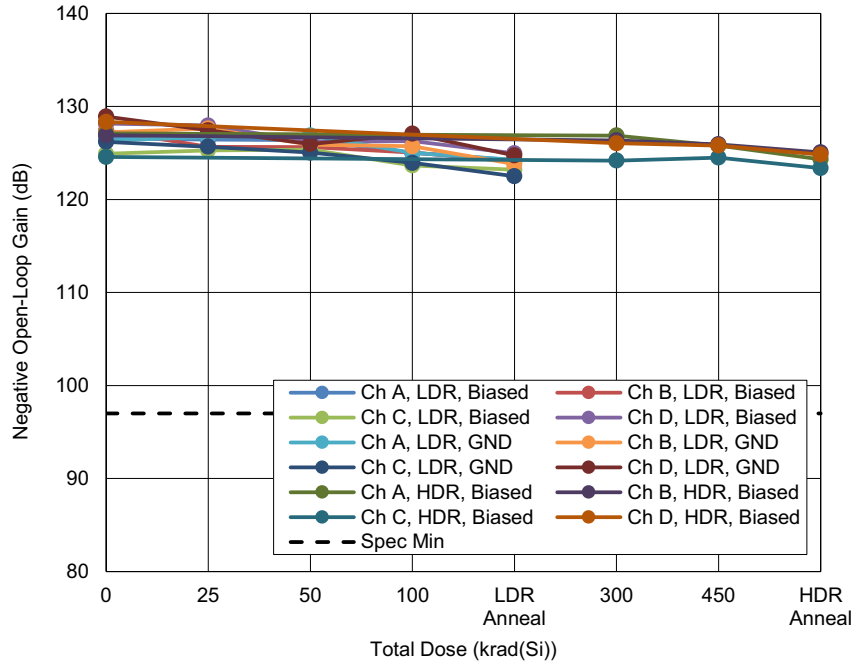


Figure 11. ISL7x444SEH negative open-loop gain, channels A through D, as a function of total dose irradiation at LDR for the biased (per Figure 2) and unbiased (all pins grounded) cases and at HDR for the biased (Figure 2) case. The LDR was 0.01rad(Si)/s and the HDR was 69.7rad(Si)/s. HDR and LDR irradiations were followed by a 168-hour biased anneal at 100°C. The sample size for the two LDR cells and the HDR cell was five for each cell. The SMD specification limit is 97dB minimum.

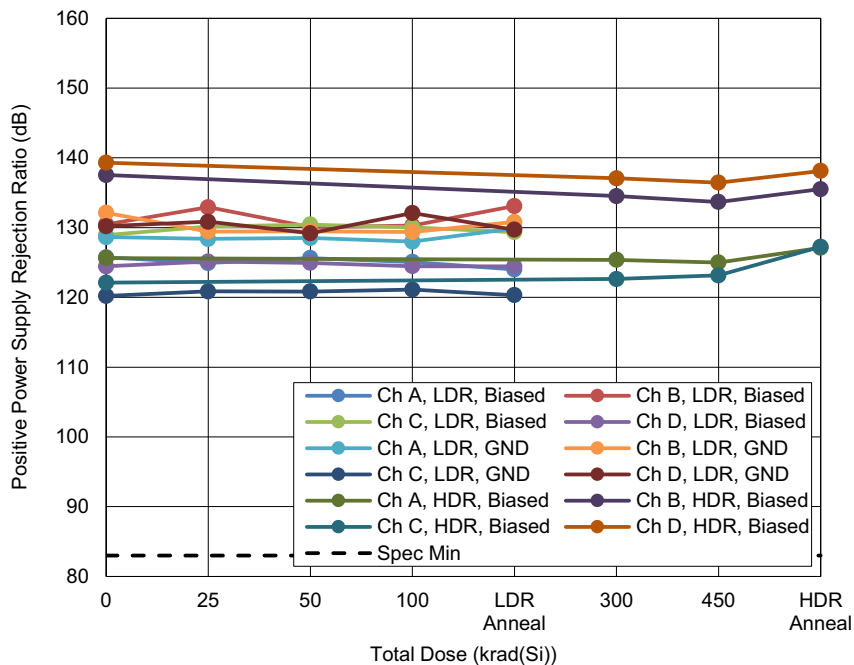


Figure 12. ISL7x444SEH positive power supply rejection ratio, channels A through D, as a function of total dose irradiation at LDR for the biased (per Figure 2) and unbiased (all pins grounded) cases and at HDR for the biased (Figure 2) case. The LDR was 0.01rad(Si)/s and the HDR was 69.7rad(Si)/s. HDR and LDR irradiations were followed by a 168-hour biased anneal at 100°C. The sample size for the two LDR cells and the HDR cell was five for each cell. The SMD specification limit is 83dB minimum.

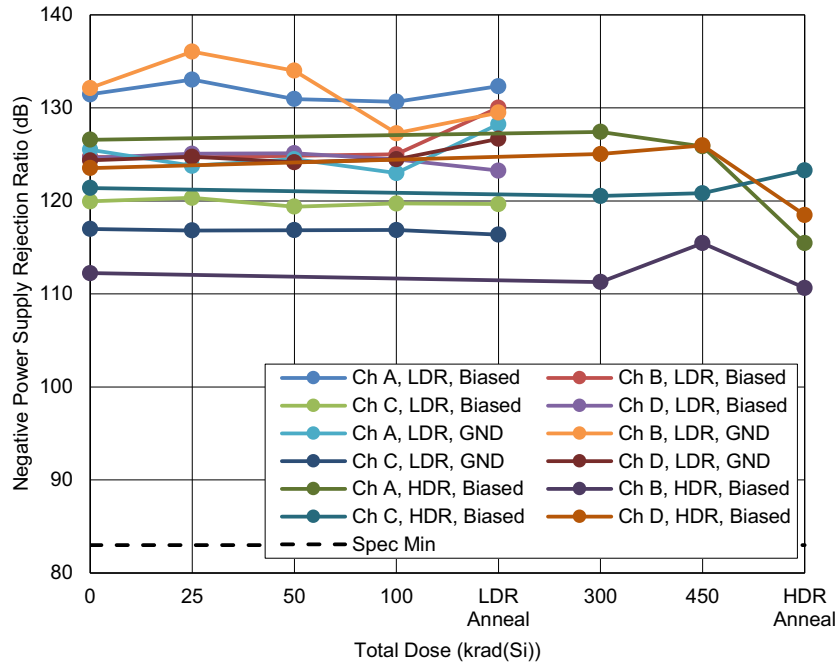


Figure 13. ISL7x444SEH negative power supply rejection ratio, channels A through D, as a function of total dose irradiation at LDR for the biased (per Figure 2) and unbiased (all pins grounded) cases and at HDR for the biased (Figure 2) case. The LDR was 0.01rad(Si)/s and the HDR was 69.7rad(Si)/s. HDR and LDR irradiations were followed by a 168-hour biased anneal at 100°C. The sample size for the two LDR cells and the HDR cell was five for each cell. The SMD specification limit is 83dB minimum.

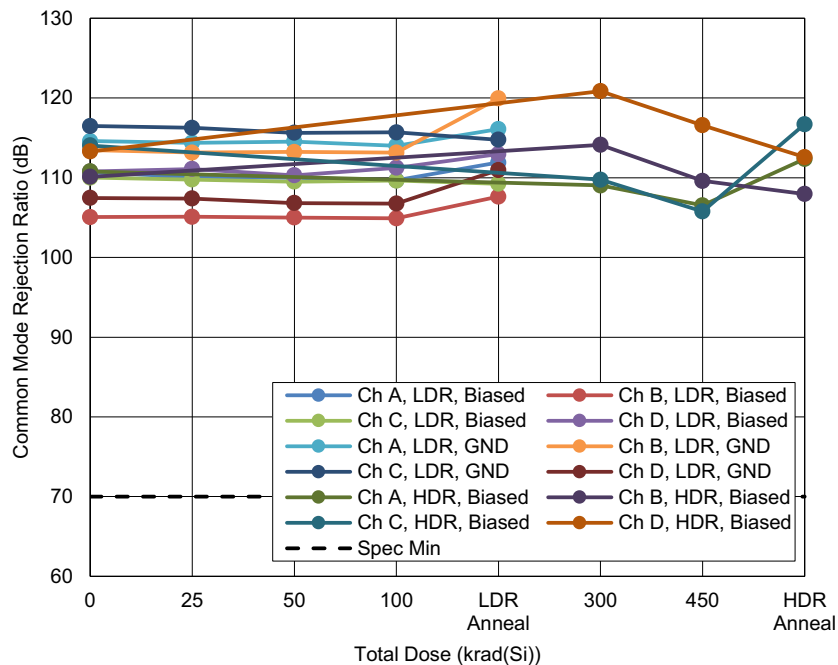


Figure 14. ISL7x444SEH common mode rejection ratio, channels A through D, as a function of total dose irradiation at LDR for the biased (per Figure 2) and unbiased (all pins grounded) cases and at HDR for the biased (Figure 2) case. The LDR was 0.01rad(Si)/s and the HDR was 69.7rad(Si)/s. HDR and LDR irradiations were followed by a 168-hour biased anneal at 100°C. The sample size for the two LDR cells and the HDR cell was five for each cell. The SMD specification limit is 70dB minimum.

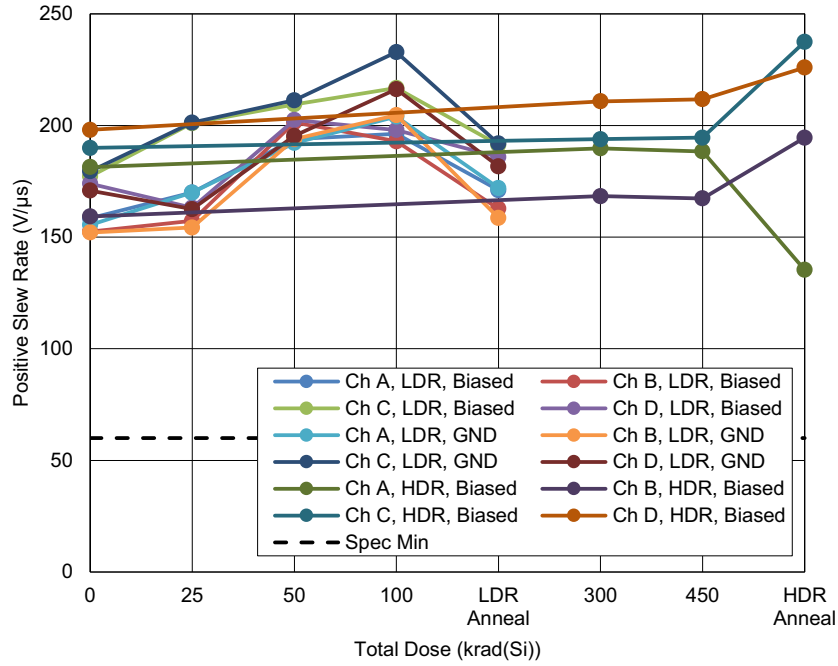


Figure 15. ISL7x444SEH positive slew rate, channels A through D, as a function of total dose irradiation at LDR for the biased (per Figure 2) and unbiased (all pins grounded) cases and at HDR for the biased (Figure 2) case. The LDR was 0.01rad(Si)/s and the HDR was 69.7rad(Si)/s. HDR and LDR irradiations were followed by a 168-hour biased anneal at 100°C. The sample size for the two LDR cells and the HDR cell was five for each cell. The SMD specification limit is 60V/μs minimum.

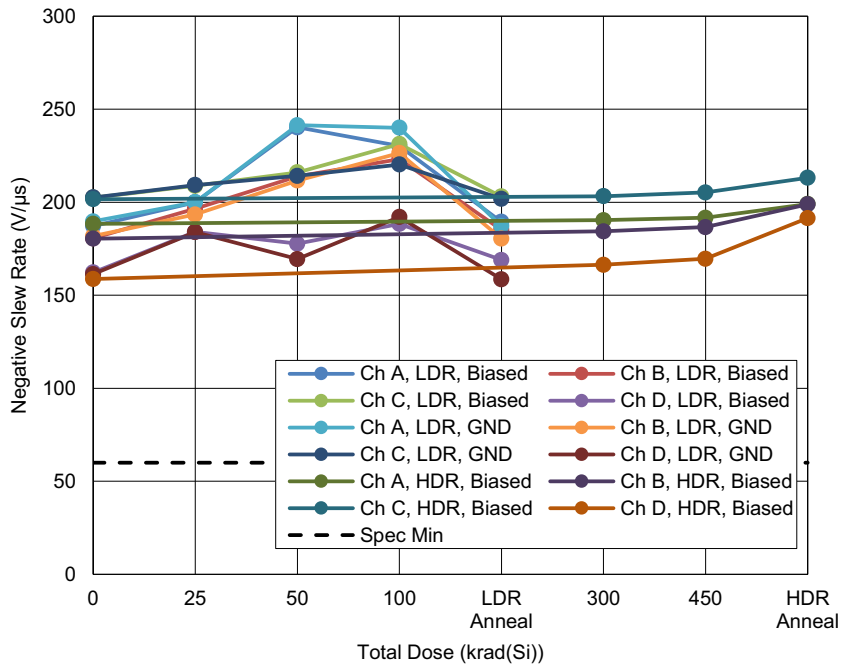


Figure 16. ISL7x444SEH negative slew rate, channels A through D, as a function of total dose irradiation at LDR for the biased (per Figure 2) and unbiased (all pins grounded) cases and at HDR for the biased (Figure 2) case. The LDR was 0.01rad(Si)/s and the HDR was 69.7rad(Si)/s. HDR and LDR irradiations were followed by a 168-hour biased anneal at 100°C. The sample size for the two LDR cells and the HDR cell was five for each cell. The SMD specification limit is 60V/μs minimum.

3. Discussion and Conclusion

This document reports the LDR and HDR testing results of the ISL7x444SEH quad operational amplifiers. Parts were irradiated under bias and with all pins grounded at LDR and under bias at HDR per MIL-STD-883 Test Method 1019.7, at 0.01rad(Si)/s and 50rad(Si)/s, respectively. The LDR test was run to 100krad(Si), and the HDR was run to 450krad(Si), reflecting the overtest protocol of Method 1019, with all samples subjected to a high temperature anneal under bias at 100°C for 168 hours. All parameters remained within the SMD and datasheet post-irradiation limits at all downpoints. The part has many measured parameters, so we have summarized the results in a table of attributes data (Appendix) and the above data plots. We will discuss each of the figures separately.

[Figure 3](#) shows both the positive and negative power supply current and plots the aggregate supply current for all four amplifiers, which is hard to avoid since all four channels have common VCC and VEE pins. Both parameters showed excellent stability, with the average supply current per amplifier at about 1.25mA. The anneals showed little effect.

[Figure 4](#), input offset voltage: As in other PR40 operational amplifiers tested previously, this parameter was remarkably stable over irradiation and annealed, with no discernible bias or dose rate sensitivity.

[Figure 5](#) and [Figure 6](#), positive and negative input bias current: This parameter is the standard indicator of LDR sensitivity. [Figure 5](#) and [Figure 6](#) show the response, and it is noted that the parameters were stable at all downpoints. The high-temperature anneals showed little effect. The data at all downpoints was well within the pre-irradiation datasheet specifications, so the part is not considered LDR sensitive.

[Figure 7](#), input offset current: This parameter was stable at all downpoints, including the anneals.

[Figure 8](#) and [Figure 9](#), output high and low voltage: The names of these parameters are perhaps a little misleading, as they are commonly used for digital parts but have an entirely different meaning in an analog context. The high or low output voltage measures how close the output can swing to the respective power supply rails, which are +18V and -18V for this plot. Both parameters were stable at all downpoints, including the anneals.

[Figure 10](#) and [Figure 11](#), positive and negative open loop gain: Both parameters were stable at all downpoints, including the anneals.

[Figure 12](#) and [Figure 13](#), positive and negative power supply rejection ratio: Both parameters were stable at all downpoints, including the anneal, with a slight increase in the positive power supply rejection ratio over anneal. The negative power supply rejection ratio for Channel B showed some variation, which indicates ATE repeatability issues.

[Figure 14](#), common mode rejection ratio: The parameter showed some variation for Channels A, C, and D for the HDR work, which is again considered artifactual and indicative of ATE repeatability issues but was stable overall.

[Figure 15](#) and [Figure 16](#), positive slew rate: Both parameters showed indications of ATE repeatability issues but were stable overall. The positive slew rate showed variation in both directions over the high-temperature anneal, and this response is also considered artifactual.

Given the excellent performance in these plots, particularly the stability shown by the key input bias current parameter, the ISL7x444SEH is not considered dose rate sensitive. The part is acceptance tested on a wafer-by-wafer basis to 300krad(Si) at HDR (50 - 300rad(Si)/s) and to 50krad(Si) at LDR (0.01rad(Si)/s), ensuring hardness to the specified level for both dose rates. The present test was run to 100krad(Si) at LDR and 450krad(Si) at HDR, reflecting the TM1019 overtest protocol. No significant differences in total dose response were noted between biased and grounded irradiation for any parameters. Additionally, no channel-to-channel differences were noted, either in the pre-irradiation data or in the total dose response of the parts

4. Appendix

Table 2. Reported Parameters and the Post-Irradiation Limits

Figure	Parameter	Low Limit	High Limit	Unit	Notes
3	Positive Power Supply Current	-	9.6	mA	Sum of all 4 channels
	Negative Power Supply Current	-	-9.6	mA	Sum of all 4 channels
4	Input Offset Voltage	-400	+400	μ V	Channels A through D
5	Positive Input Bias Current	-370	+370	nA	Channels A through D
6	Negative Input Bias Current	-370	+370	nA	Channels A through D
7	Input Offset Current	-30	+30	nA	Channels A through D
8	Output High Voltage	-	160	mV	Channels A through D
9	Output Low Voltage	-	160	mV	Channels A through D
10	Positive Open-Loop Gain	97	-	dB	Channels A through D
11	Negative Open-Loop Gain	97	-	dB	Channels A through D
12	Positive Power Supply Rejection Ratio	83	-	dB	Channels A through D
13	Negative Power Supply Rejection Ratio	83	-	dB	Channels A through D
14	Common Mode Rejection Ratio	70	-	dB	Channels A through D
15	Positive Slew Rate	60	-	V/ μ s	Channels A through D
16	Negative Slew Rate	60	-	V/ μ s	Channels A through D

5. Revision History

Revision	Date	Description
1.00	Mar 31, 2023	Updated to the latest template. Added ISL73444SEH information to the document. Updated Figures 3 through 16. Updated Discussion and Conclusion section.
0.00	Sep 20, 2013	initial release

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.