ISL705ARH

Total Dose Test Report

Introduction

This report details the results of a Low Dose Rate (LDR) and High Dose Rate (HDR) total dose test of the ISL705ARH microprocessor supervisory circuit. The test was conducted to determine the sensitivity of the part to the total dose environment and to determine if dose rate and bias sensitivity exist.

Renesas markets nine versions of the ISL705*RH (ISL705A/B/C and ISL735A/B/C) with the differences being limited to the operation of the reset pin (active high, active low, and active low open drain output). These are minor functional differences and the total dose data for the ISL705ARH applies to the other versions. The base ISL705*RH is acceptance tested on a wafer-by-wafer basis to 100krad(Si) at HDR, as defined in MIL-STD-883 test method 1019 (50 - 300rad(Si)/s). The ISL705*EH is acceptance tested on a wafer-by-wafer basis to 100krad(Si) at HDR, as defined in MIL-STD-883 test method 1019 (50 - 300rad(Si)/s), and to 50krad(Si) at LDR, also as defined in method 1019 (0.01rad(Si)/s maximum). The ISL735*EH is acceptance tested on a wafer-by-wafer basis to 50krad(Si) at LDR, as defined in method 1019 (0.01rad(Si)/s maximum).The ISL705*RH, ISL705*EH, and ISL735*EH are identical parts.

These total dose test results are intended to apply to the following devices:

- ISL705ARH, ISL705AEH, and ISL735AEH - Reset pin is an active high
- ISL705BRH, ISL705BEH, and ISL735BEH - Reset pin is an active low
- ISL705CRH, ISL705CEH, and ISL735CEH - Reset pin is an active low open drain output

Product Description

The ISL705ARH is a radiation hardened 5.0V supervisory circuit that reduces the complexity required to monitor supply voltages in microprocessor systems. The device significantly improves accuracy and reliability relative to discrete solutions. Each IC provides four key functions:

- A reset output during power-up, power-down, and brownout conditions.
- An independent watchdog output that goes low if the watchdog input has not been toggled within 1.6s.
- A precision threshold detector for monitoring a power supply other than VDD.
- An active-low manual-reset input.

The ISL705ARH has been specifically designed and manufactured to provide reliable performance in harsh radiation environments. It is total dose hardened to 100krad(Si) at HDR and offers guaranteed performance across the full -55°C to +125°C military temperature range.

Specifications for radiation hardened QML devices are controlled by the Defense Logistics Agency (Land and Maritime) in Columbus, OH (DLA). The SMD number must be used when ordering. Detailed electrical specifications for the ISL705ARH are contained in SMD 5962-11213. A link is provided on the Renesas Web site for downloading this document.

Related Literature

For a full list of related documents, visit our website:

- ISL705ARH, ISL705AEH, ISL735AEH, ISL705BRH, ISL705BEH, ISL735BEH, ISL705CRH, ISL705CEH, and ISL735CEH device pages
- MIL-STD-883H test method 1019.8

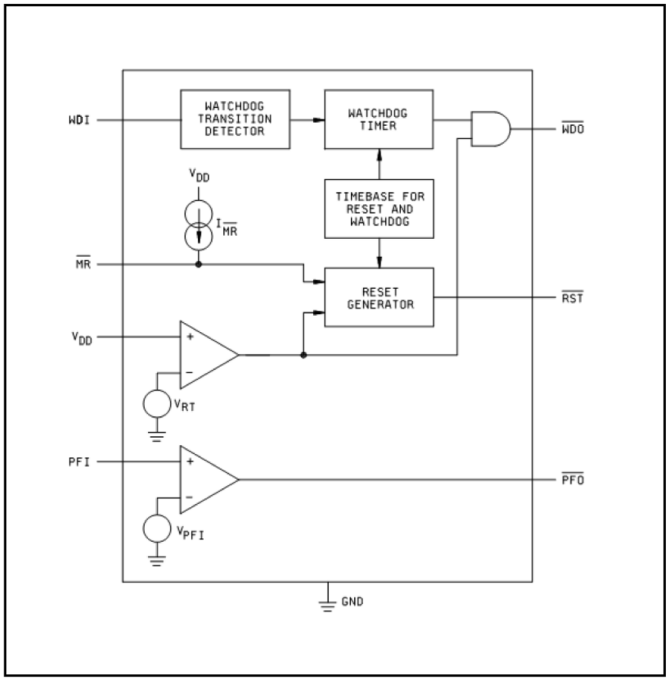


Figure 1. ISL705ARH Block Diagram

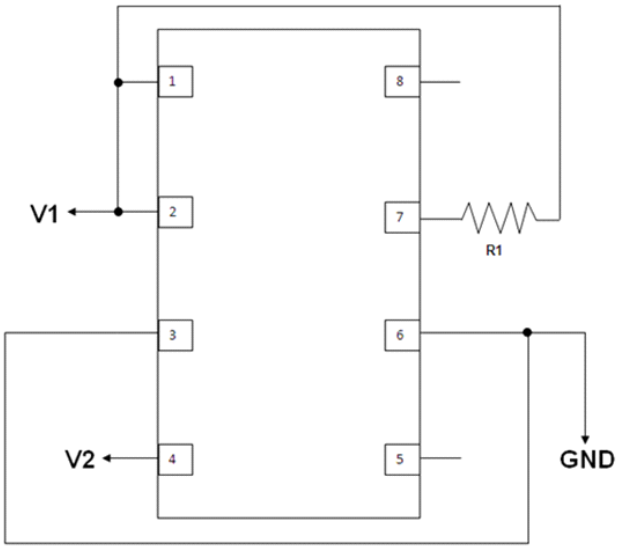
1. Test Description

1.1 Irradiation Facilities

HDR testing of the ISL705ARH was performed using a Gammacell 220 irradiator located in the Palm Bay, Florida Renesas facility. LDR testing was performed using a J. L. Shepherd model 484 irradiator. The HDR irradiations were done at 85rad(Si)/s and the LDR work was performed at 0.010rad(Si)/s, both per MIL-STD-883 Method 1019.

1.2 Test Fixturing

Figure 2 shows the electrical configuration used for biased irradiation in conformance with Standard Microcircuit Drawing (SMD) 5962-11213.



NOTES:

V1 = 5.5 V ±5%

V2 = 1.4 V ±5%

R1 = OPEN for this device.

Figure 2. Irradiation Bias Configuration for the ISL705ARH per SMD 5962-11213.

1.3 Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using the production Automated Test Equipment (ATE) with data logging at each downpoint. Downpoint electrical testing was performed at room temperature.

1.4 Experimental Matrix

Total dose irradiations proceeded in accordance with the guidelines of MIL-STD-883 Test Method 1019.7. The experimental matrix consisted of eight samples irradiated at HDR with all pins grounded, eight samples irradiated at HDR under bias, eight samples irradiated at LDR with all pins grounded and eight samples irradiated at LDR under bias. Four control units were used.

Samples of the ISL705ARH die were drawn from production lot WMA4H and were packaged in the standard hermetic 8 Ld solder-sealed flatpack (CDFP4-F16) production package. Samples were processed through the standard burn-in cycle before irradiation, as required by MIL-STD-883, and were screened to the SMD 5962-11213 limits at room, low and high temperatures prior to the test.

1.5 Downpoints

Downpoints for the tests were zero, 10krad(Si), 25krad(Si), 50krad(Si), 100krad(Si), and 150krad(Si) for the high and LDR tests.

2. Results

2.1 Results and Conclusions

Testing at both dose rates to 150krad(Si) of the ISL705ARH is complete. All samples showed excellent stability and remained within the SMD limits at all downpoints, and no dose rate sensitivity or bias sensitivity was observed in any parameter. The control units indicated good repeatability of the ATE hardware, fixturing and software at all downpoints. The part is not considered LDR or bias sensitive.

A rebound test after the HDR irradiation was not performed, as the P6 process has been characterized for this effect using the ISL75051SRH as a test vehicle. The process was shown to display no rebound effects after a post-irradiation anneal under bias at +100°C for 168 hours. These conditions are as specified in MIL-STD-883. A similar anneal of the samples was performed after the LDR irradiation for informational purposes only; no rebound was observed.

2.2 Variables Data

The plots in Figures 3 through 25 show data at all downpoints. The plots show the median of key parameters as a function of total dose for each of the four irradiation conditions, as well as the control unit data and the applicable SMD limits. We chose to plot the median for these parameters due to the relatively small sample sizes involved.

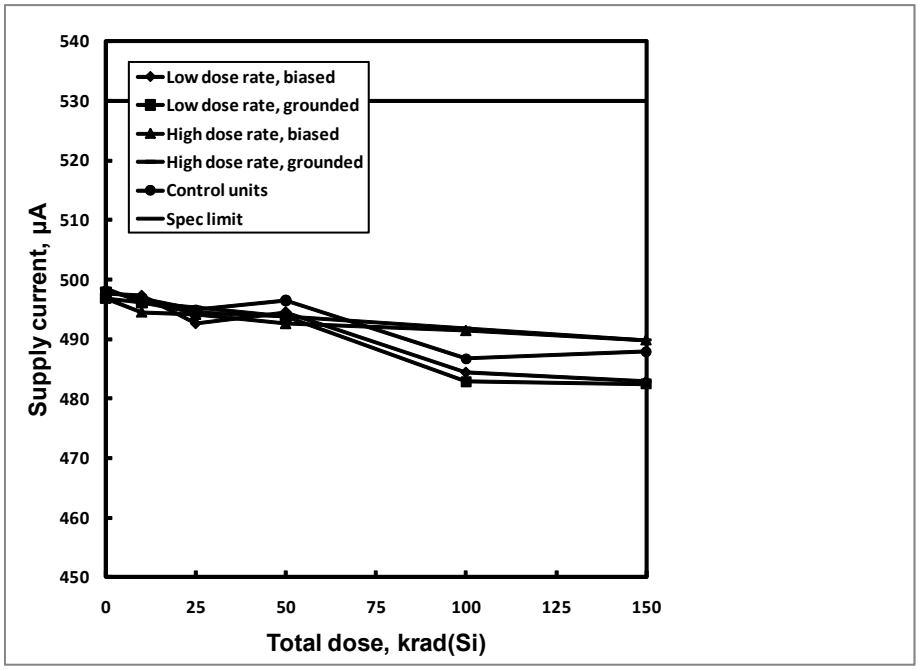


Figure 3. ISL705ARH power supply current as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limit is 530µA maximum.

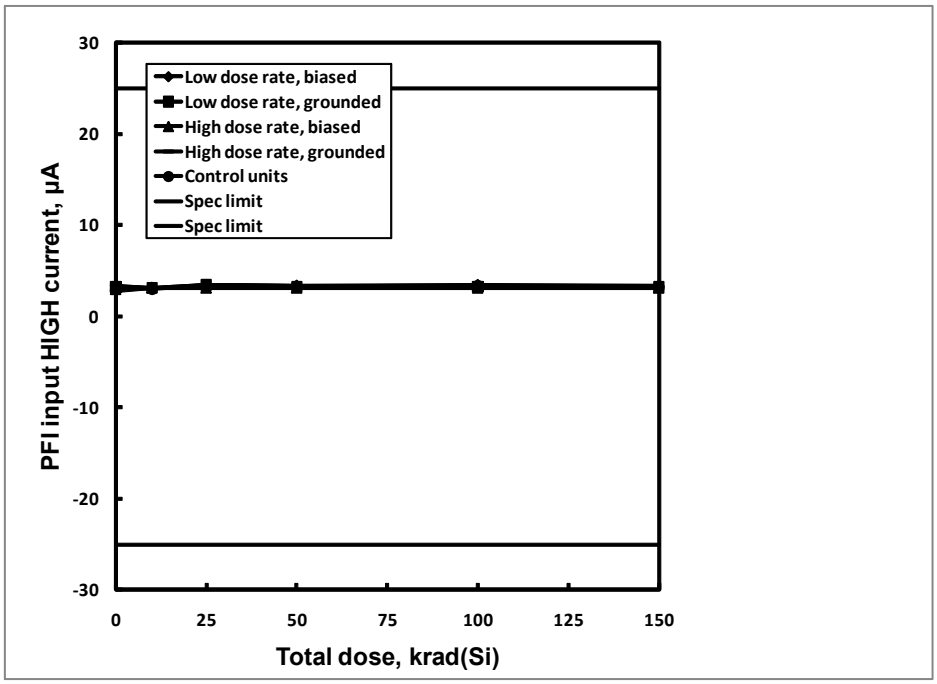


Figure 4. ISL705ARH power fail input (PFI) input high current as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limits are -25.0µA to 25.0µA.

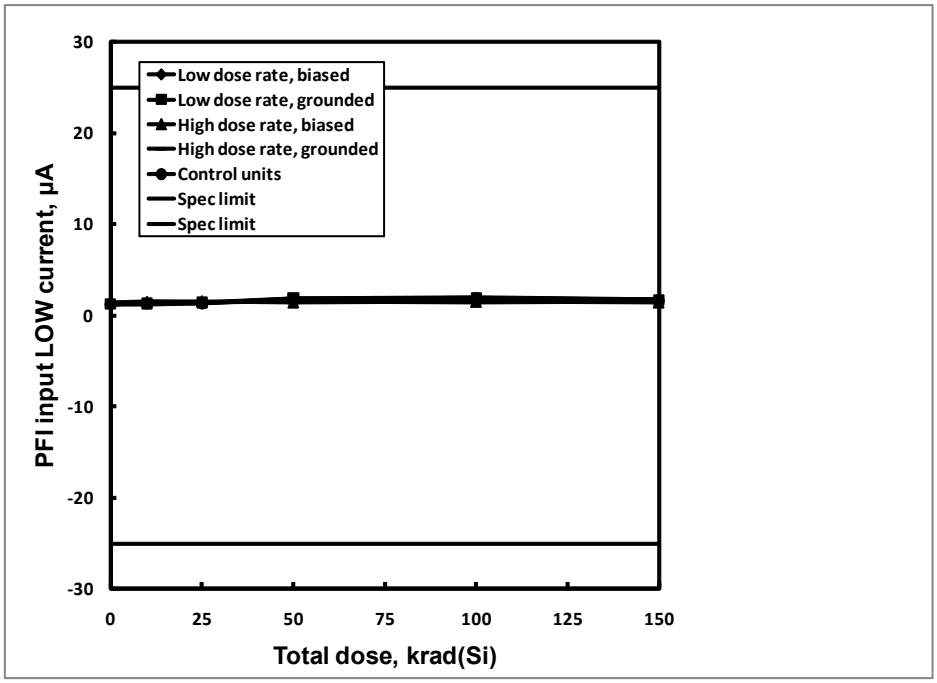


Figure 5. ISL705ARH power fail input (PFI) input low current as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limits are -25.0µA to 25.0µA.

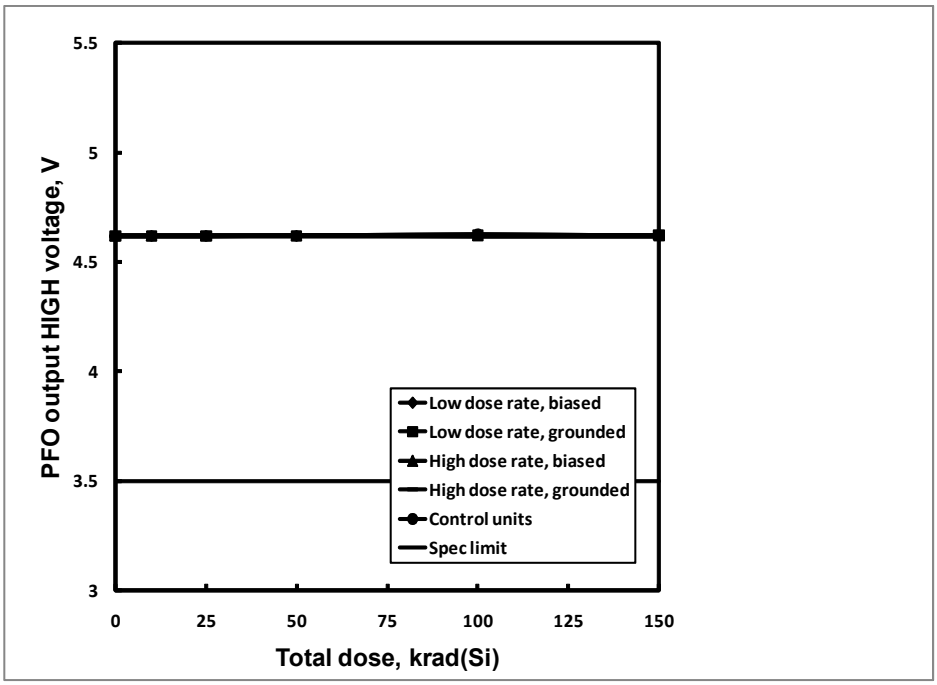


Figure 6. ISL705ARH power fail output (PFO) output high voltage as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limit is 3.5V minimum.

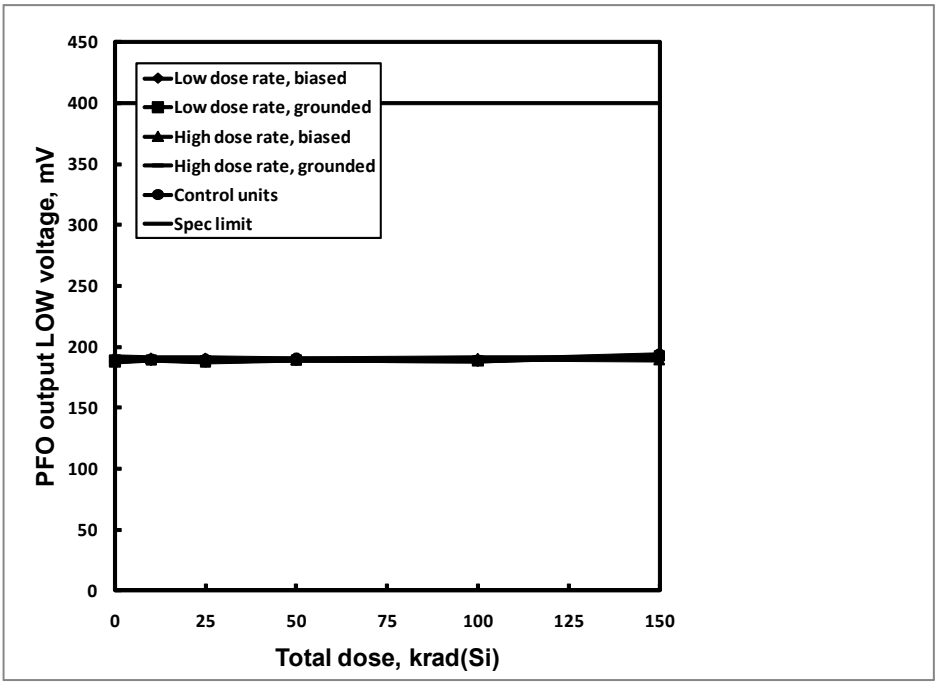


Figure 7. ISL705ARH power fail output (PFO) output low voltage as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limit is 400.0mV maximum.

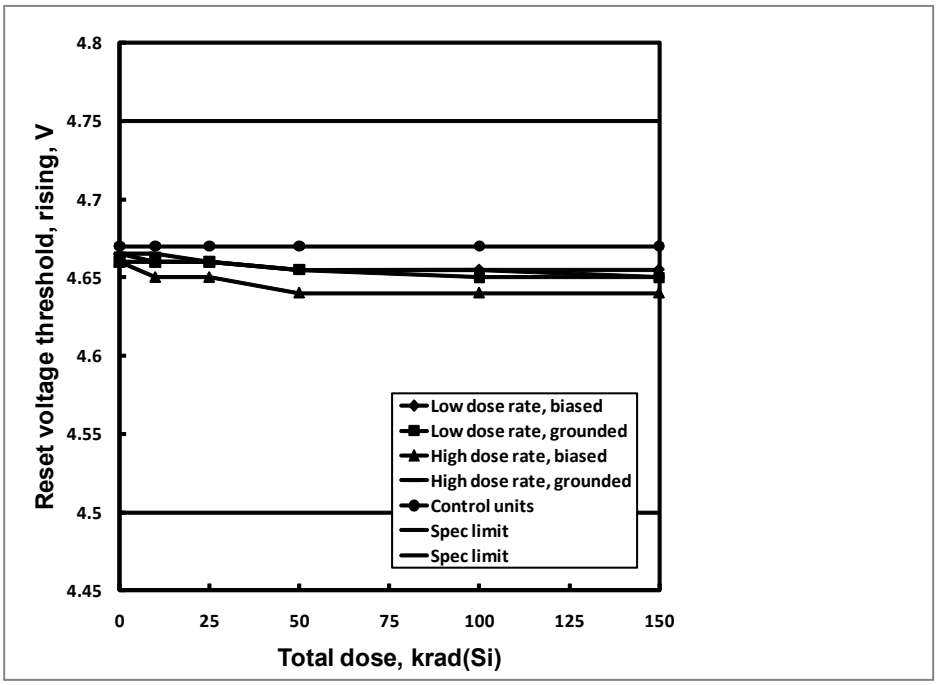


Figure 8. ISL705ARH reset threshold voltage, rising, as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limits are 4.50V to 4.75V.

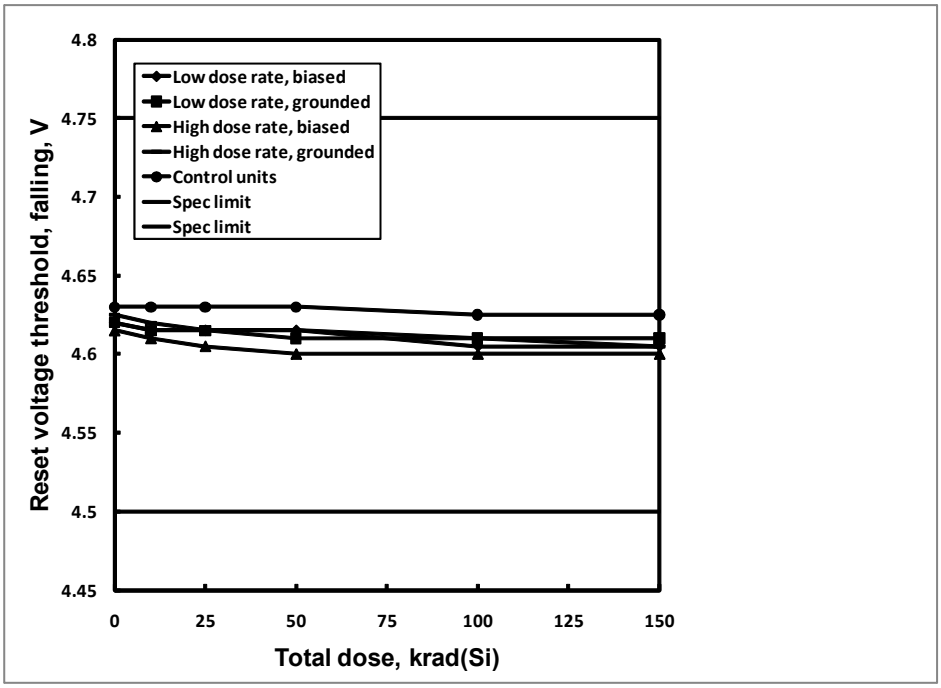


Figure 9. ISL705ARH reset threshold voltage, falling, as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limits are 4.50V to 4.75V.

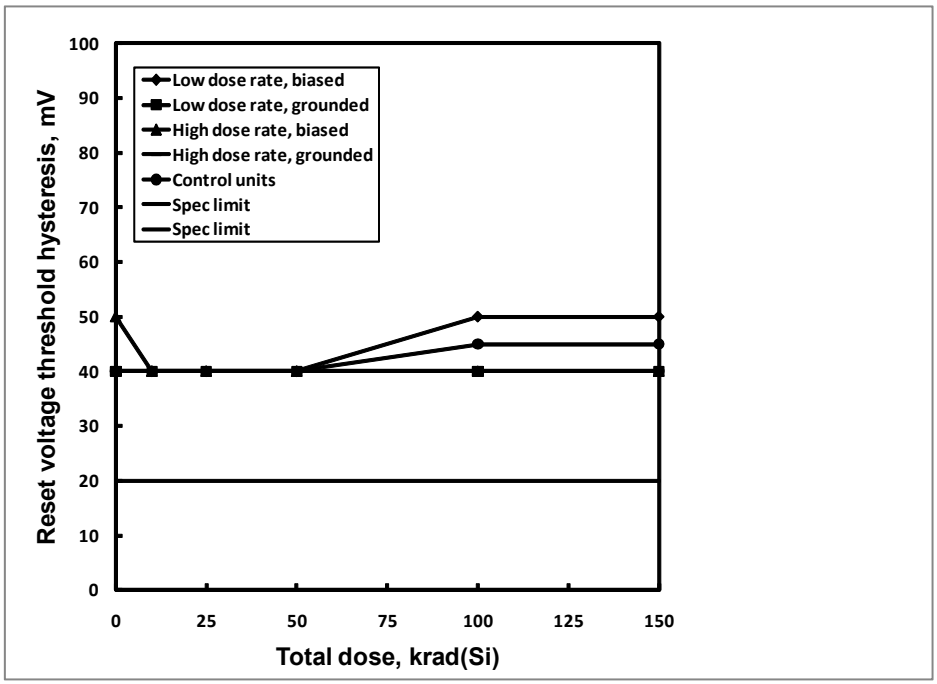


Figure 10. ISL705ARH reset threshold voltage hysteresis as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limit is 20mV minimum.

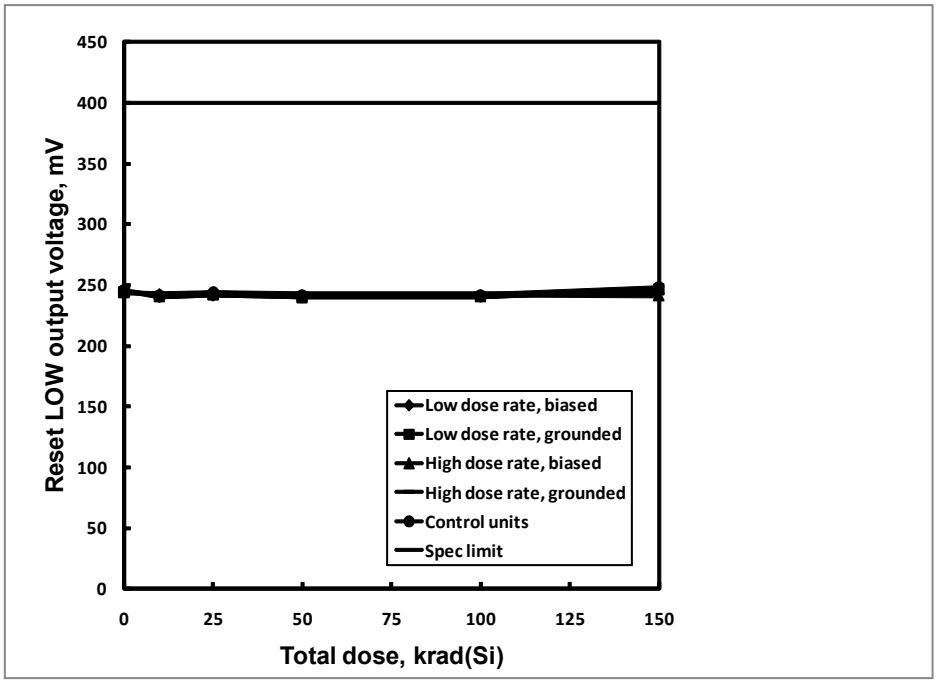


Figure 11. ISL705ARH reset low output voltage as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limit is 400.0mV maximum.

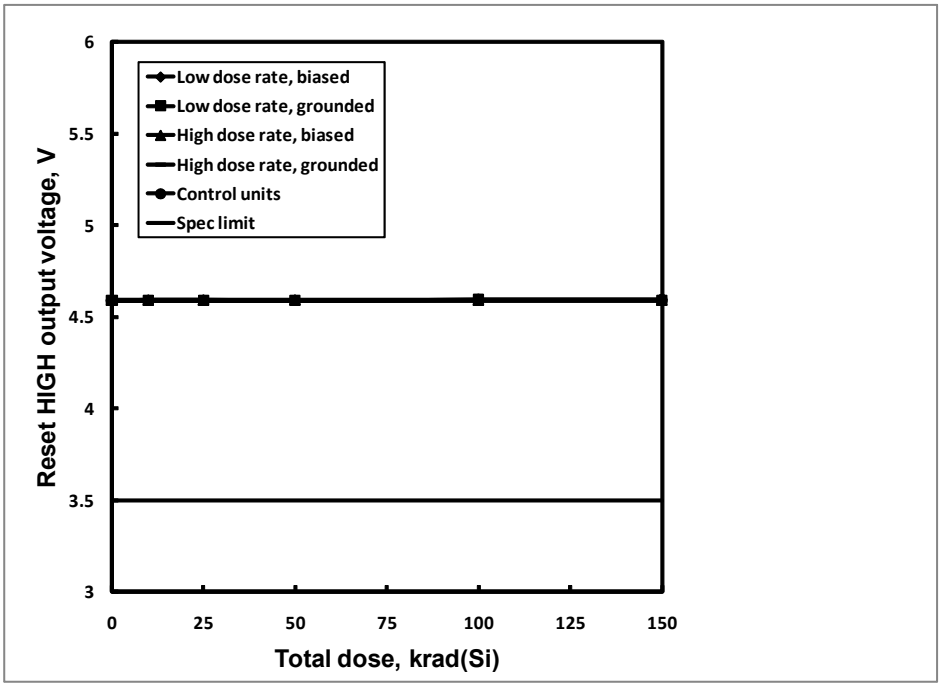


Figure 12. ISL705ARH reset high output voltage as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limit is 3.5V minimum.

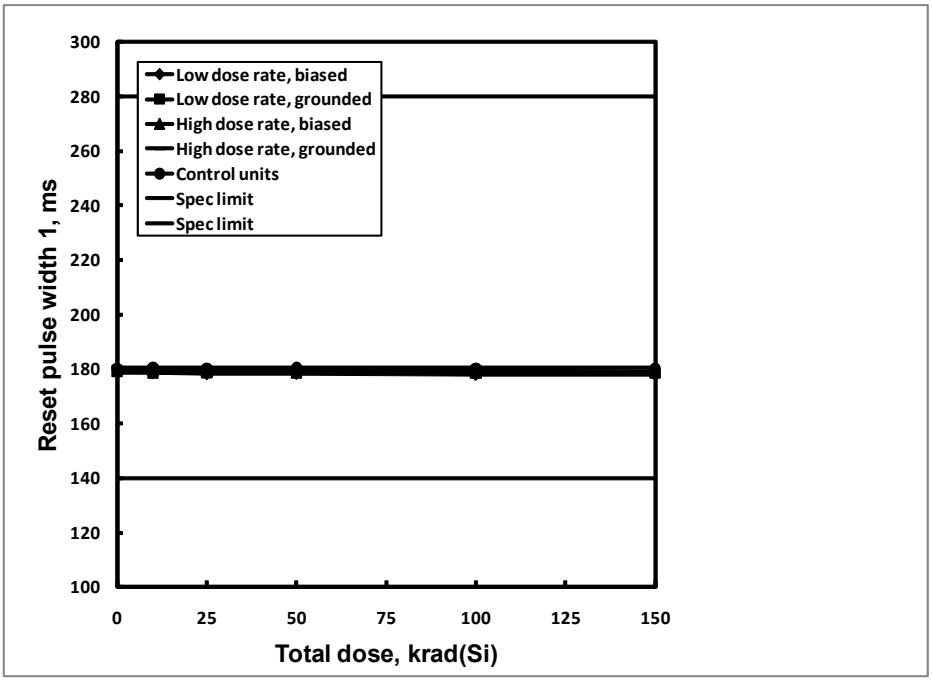


Figure 13. ISL705ARH reset pulse width 1 as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limits are 140.0ms to 280.0ms.

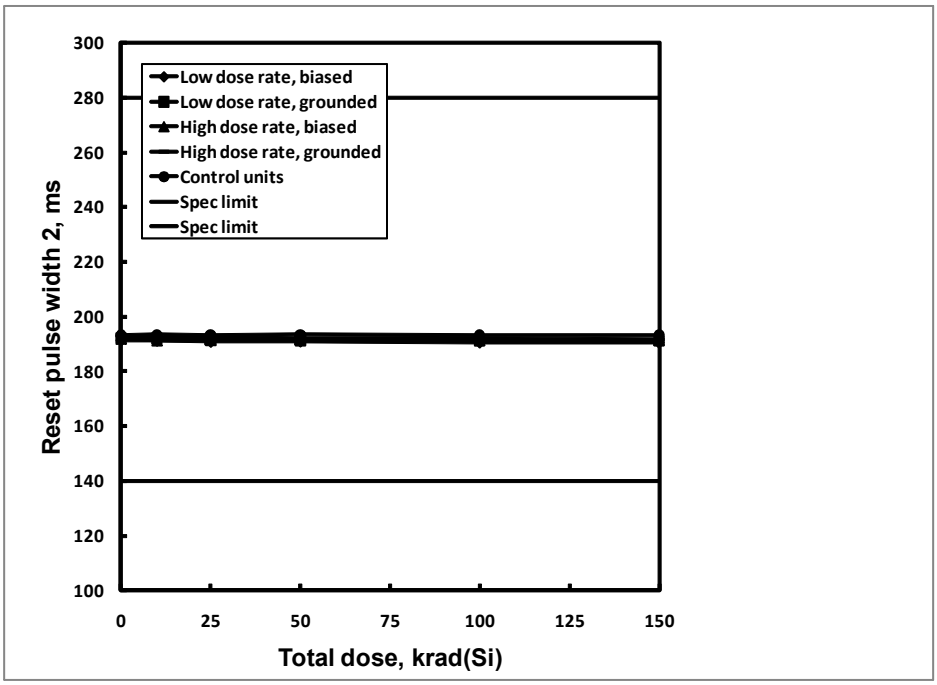


Figure 14. ISL705ARH reset pulse width 2 as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limits are 140.0ms to 280.0ms.

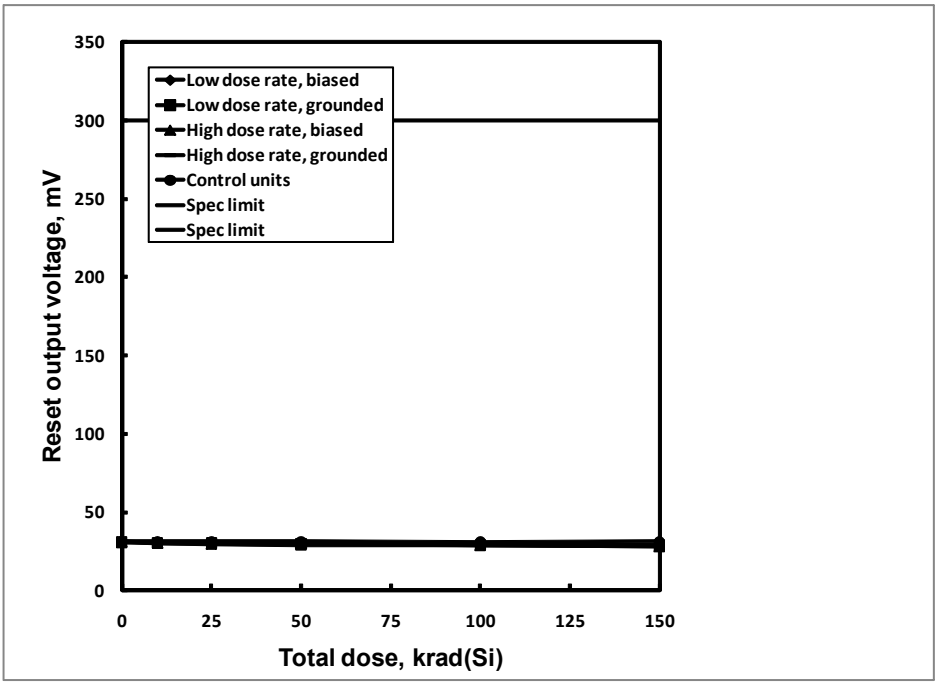


Figure 15. ISL705ARH reset output voltage as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limit is 300.0mV maximum.

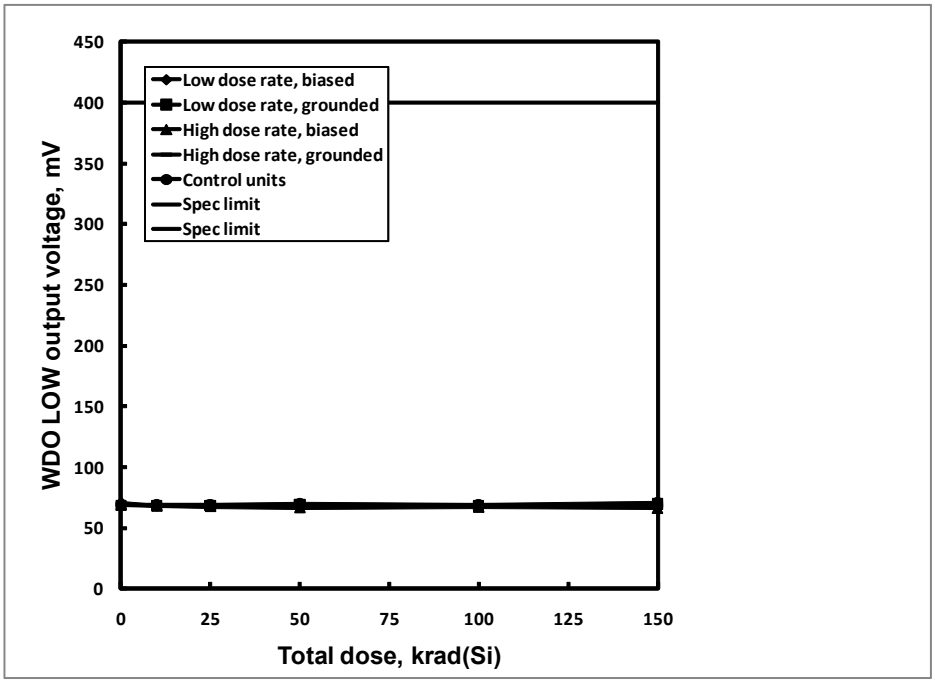


Figure 16. ISL705ARH watchdog output (WDO) low voltage as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limit is 400.0mV maximum.

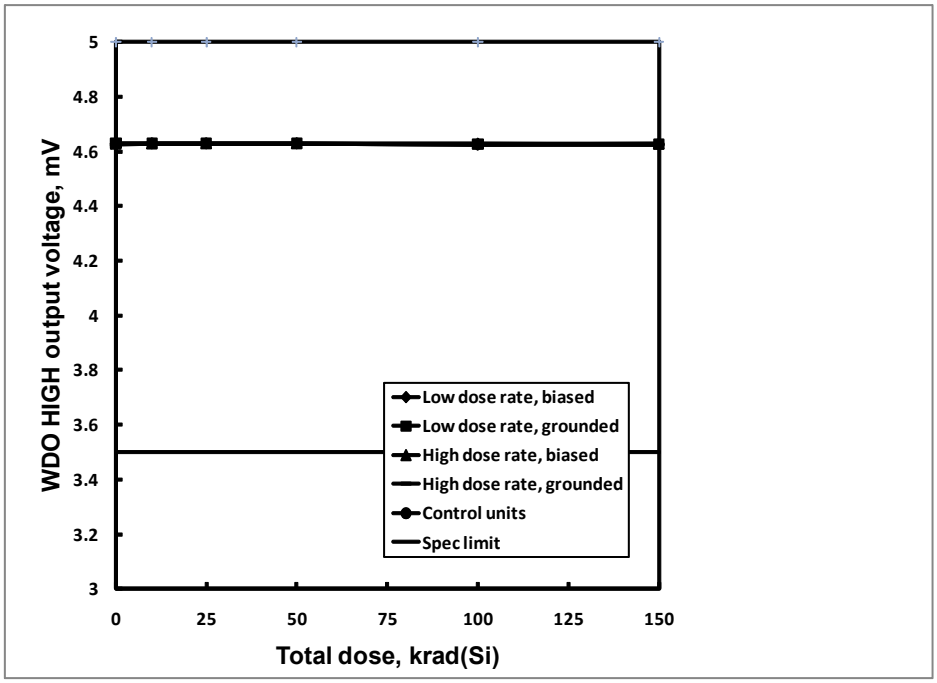


Figure 17. ISL705ARH watchdog output (WDO) high voltage as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limit is 3.5V minimum.

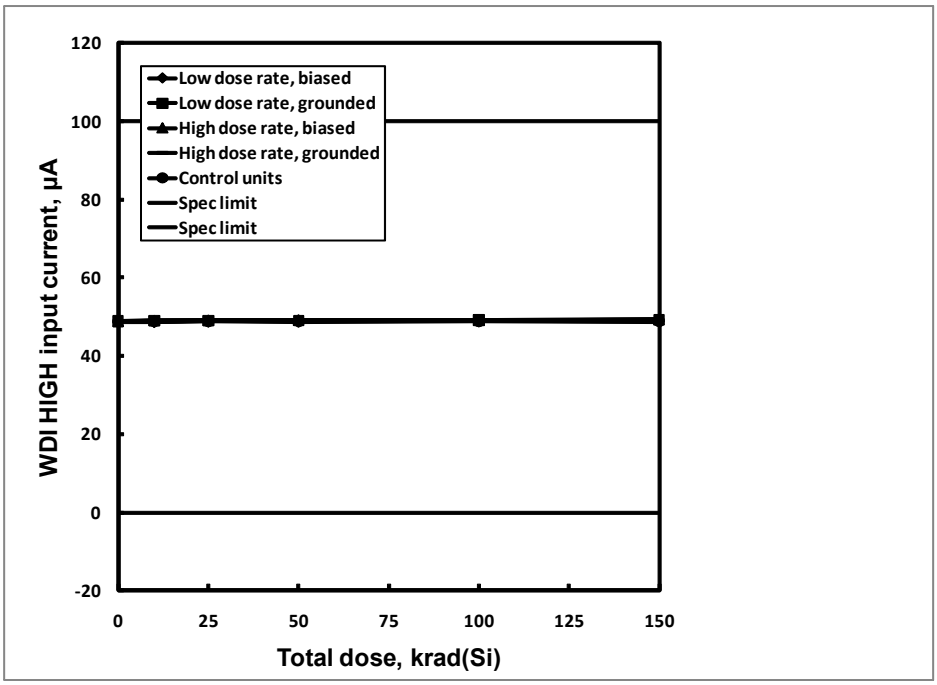


Figure 18. ISL705ARH watchdog input (WDI) input high current as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limit is 100µA maximum.

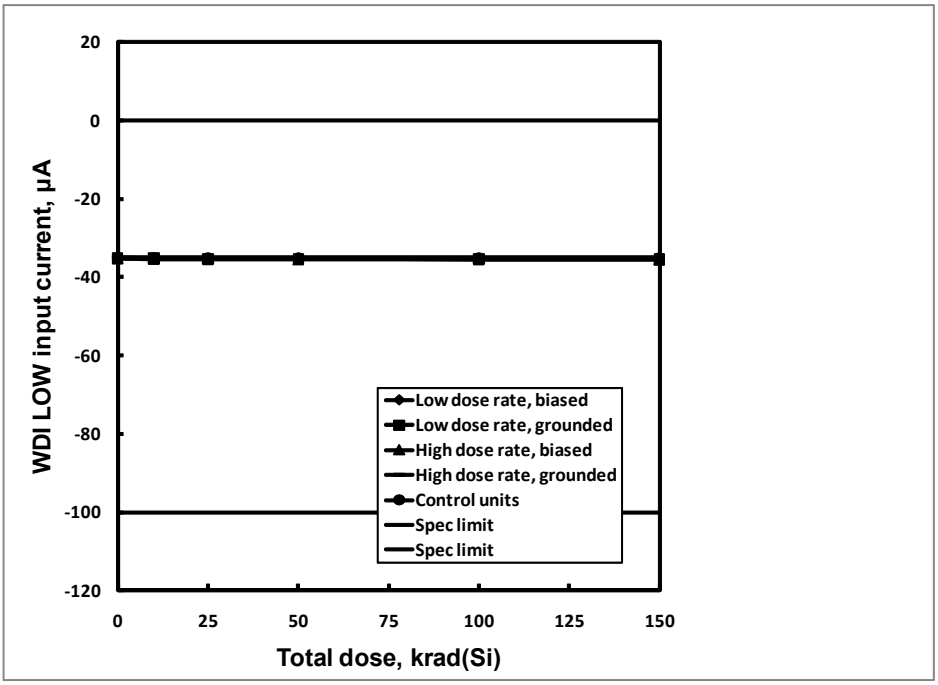


Figure 19. ISL705ARH watchdog input (WDI) input low current as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limit is -100µA maximum.

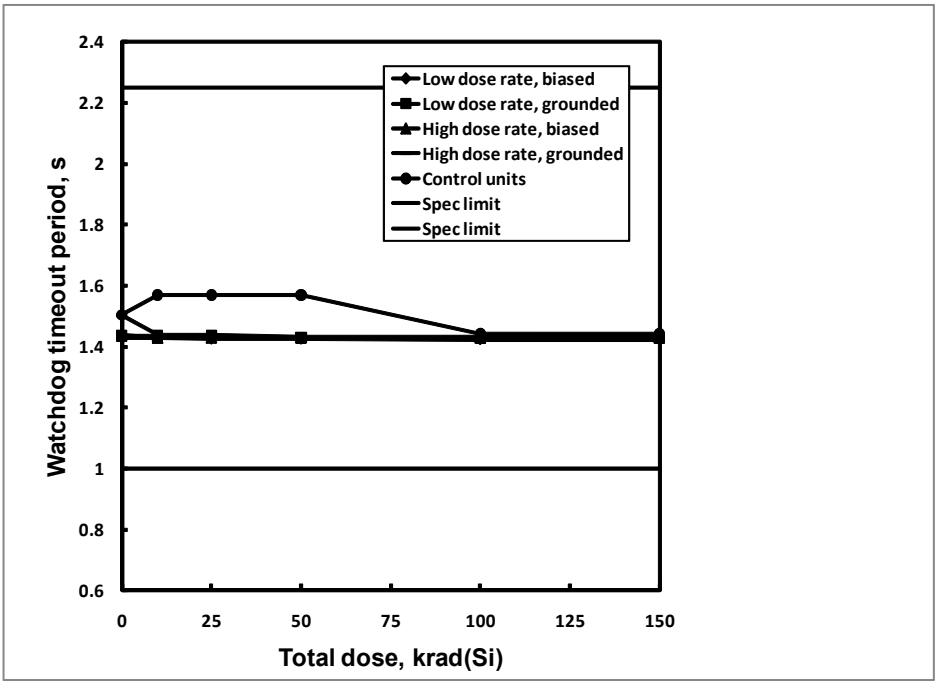


Figure 20. ISL705ARH watchdog timeout period as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limits are 1.00s to 2.25s.

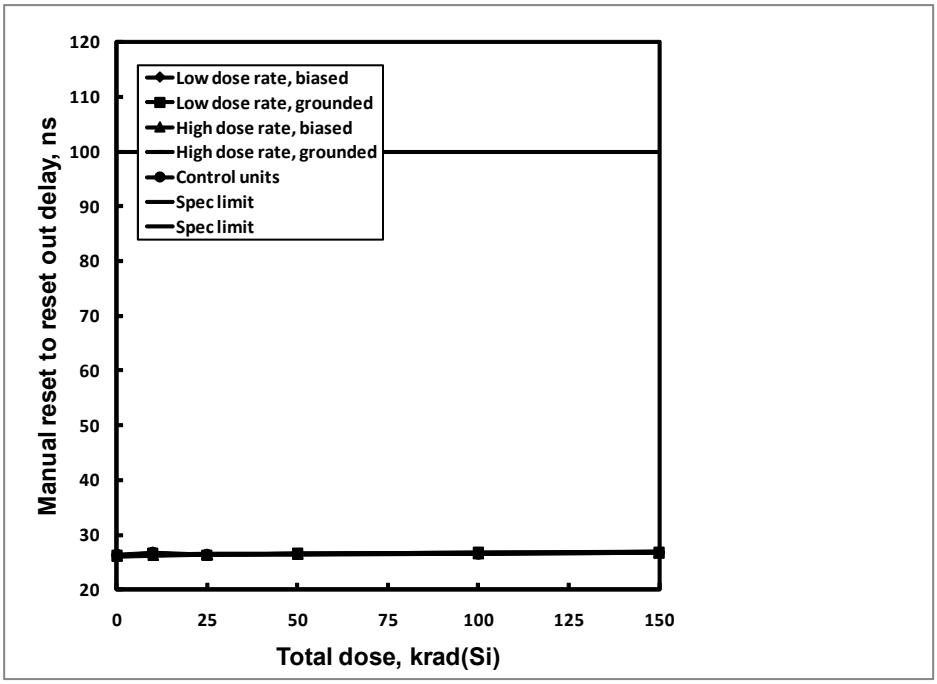


Figure 21. ISL705ARH manual reset to reset out delay as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limit is 100ns maximum.

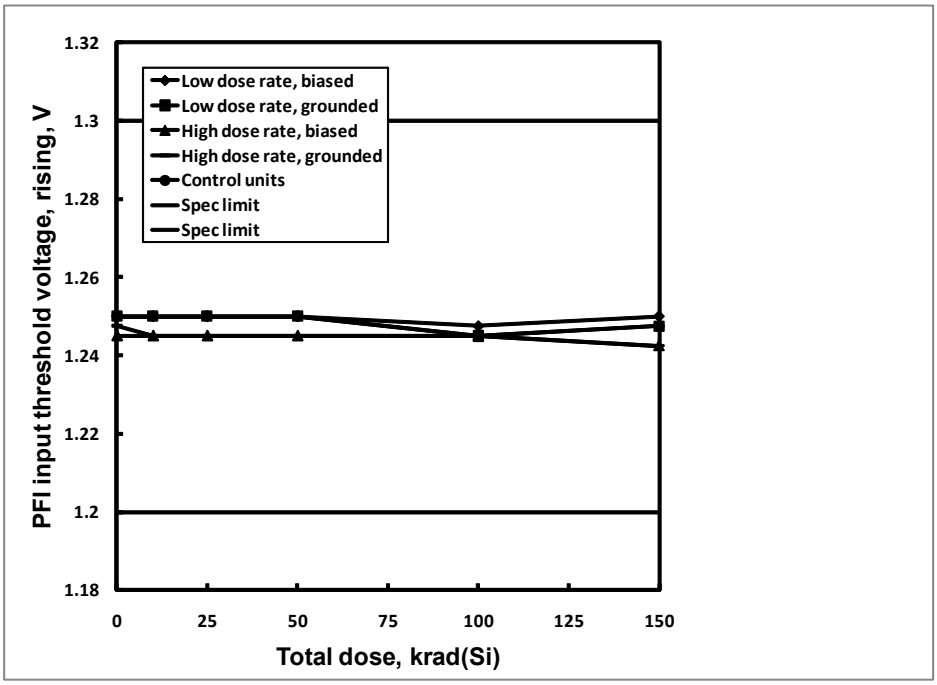


Figure 22. ISL705ARH power fail input (PFI) threshold voltage, rising, as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limits are 1.2V to 1.3V.

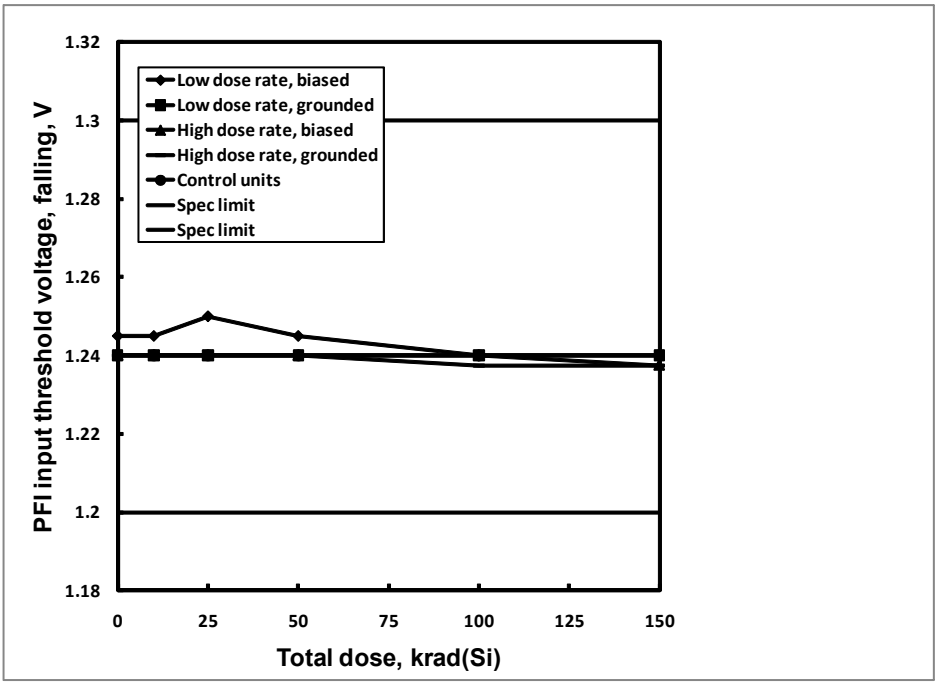


Figure 23. ISL705ARH power fail input (PFI) threshold voltage, falling, as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limits are 1.2V to 1.3V.

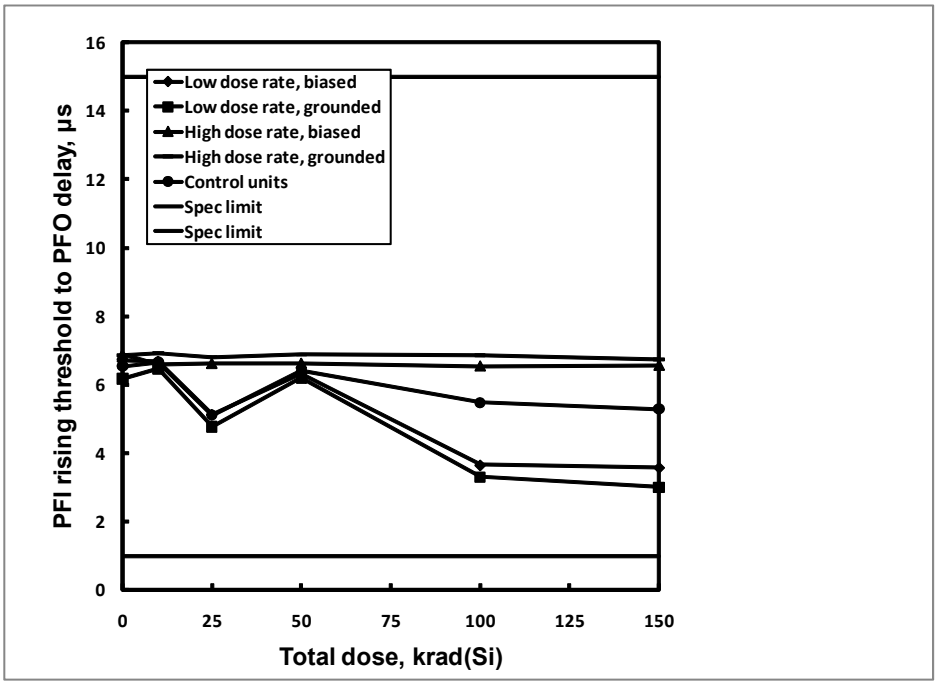


Figure 24. ISL705ARH power fail input (PFI) rising threshold voltage to PFO delay as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limit is 15µs maximum.

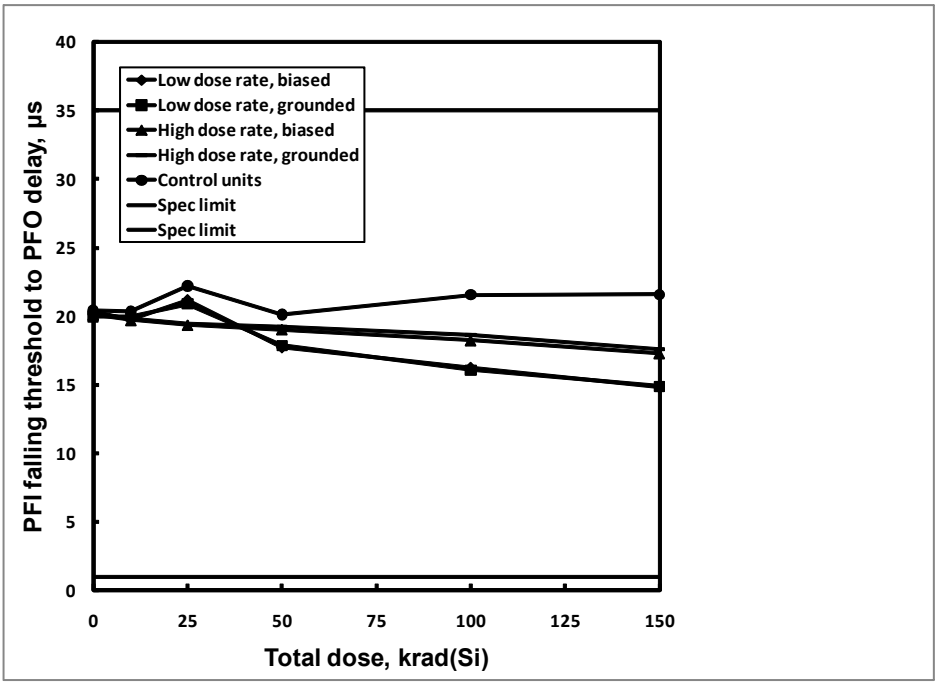


Figure 25. ISL705ARH power fail input (PFI) falling threshold voltage to PFO delay as a function of total dose irradiation at LDR and HDR for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The LDR was 0.01rad(Si)/s and the HDR 85rad(Si)/s. Sample size for each cell was 8, and 4 control units were used. The post-irradiation SMD limit is 35µs maximum.

3. Appendices

Table 1. Reported Parameters

Figure	Parameter	Low Limit	High Limit	Units
3	Power supply current	-	530	µA
4	Power fail input (PFI) input high current	-25.0	25.0	µA
5	Power fail input (PFI) input low current	-25.0	25.0	µA
6	Power fail output (PFO) output high voltage	3.5	-	V
7	Power fail output (PFO) output low voltage	-	400.0	mV
8	Reset threshold voltage, rising	4.5	4.75	V
9	Reset threshold voltage, falling	4.5	4.75	V
10	Reset threshold voltage hysteresis	20	-	mV
11	Reset low output voltage	-	400.0	mV
12	Reset high output voltage	3.5	-	V
13	Reset pulse width 1	140	280	ms
14	Reset pulse width 2	140	280	ms
15	Reset output voltage	-	300	mV
16	Watchdog output (WDO) low voltage		400.0	mV
17	Watchdog output (WDO) high voltage	3.5	-	V
18	Watchdog input (WDI) input high current	-	-100.0	µA
19	Watchdog input (WDI) input low current	-	-100.0	µA
20	Watchdog timeout period	1.0	2.25	s
21	Manual reset to reset out delay	-	100	ns
22	Power fail input (PFI) threshold voltage, rising	1.2	1.3	V

Table 1. Reported Parameters (Continued)

Figure	Parameter	Low Limit	High Limit	Units
23	Power fail input (PFI) threshold voltage, falling	1.2	1.3	V
24	PFI rising threshold voltage to PFO delay	-	15	µs
25	PFI falling threshold voltage to PFO delay		35	µs

Note: Limits are taken from Standard Microcircuit Drawing (SMD) 5962-11213.

4. Revision History

Rev.	Date	Description
2.00	Dec.4.19	Assigned file number and applied new formatting. Added 735 series for LDR products.
1.00	Feb.5.12	Add ISL705B/C text
0.00	Jan.5.12	Initial release

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