ISL71710M, ISL71710SLHM

Neutron Test Results of the ISL71710x, Radiation Hardened Active-Input High Speed Digital Isolator

Introduction

This report summarizes results of 1MeV equivalent neutron testing of the ISL71710M and ISL71710SLHM (ISL71710x), an active input digital signal isolator with CMOS output, using Giant Magnetoresistive (GMR) technology. The test was conducted to determine the sensitivity of the part to displacement damage (DD) caused by neutron or proton environments. Neutron fluences ranged from 5×10^{11}n/cm^2 to 1×10^{13}n/cm^2.

Product Description

The Radiation Hardened ISL71710x is an active input digital signal isolator with CMOS output, using Giant Magnetoresistive (GMR) technology for small size, high speed, and low power. The ISL71710x is the fastest isolator of its type, with a 150Mbps typical data rate. The symmetric magnetic coupling barrier provides a typical propagation delay of only 10ns and a pulse-width distortion as low as 0.3ns.

The ISL71710x has unsurpassed common-mode transient immunity of 50kV/µs. It is ideal for isolating applications such as PROFIBUS, RS-485, and RS-422.

The ISL71710x is offered in an 8 Ld 5mm×4mm SOIC package and is fully specified across the military ambient temperature range of -55°C to +125°C. The functional block diagram is shown in Figure 1.

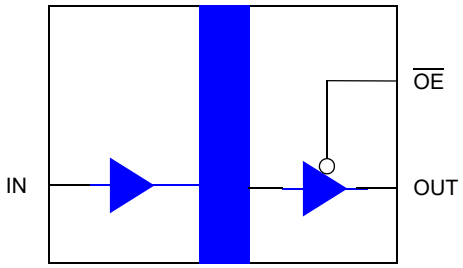

Figure 1. ISL71710x Functional Block Diagram

The package outline and pin assignments for the ISL71710x are shown in Figure 2 with the pin descriptions given in Table 1.

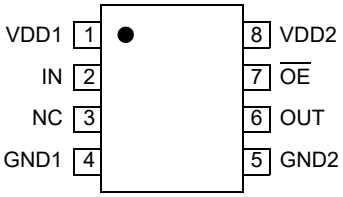

Figure 2. ISL71710x Pin Assignments - Top View (8 Ld NSOIC)

Table 1. ISL71710x Pin Descriptions

Pin Number	Pin Name	Description
1	VDD1	Supply voltage
2	IN	Data in
3	NC	No internal connection. Leave this pin floating or connect it to VDD1 or GND1
4	GND1	Ground return for VDD1
5	GND2	Ground return for VDD2
6	OUT	Data output
7	$\overline{OE}$	Output enable, active low. Internally pulled low with 100kΩ to enable the output when this pin is not connected.
8	VDD2	Supply voltage

Contents

1. Test Description

1.1 Irradiation Facilities

Neutron fluence irradiations were performed on the test samples on March 29, 2023, at the University of Massachusetts, Lowell (UMASS Lowell) fast neutron irradiator per Mil-STD-883G, Method 1017.2, with each part unpowered during irradiation. The target irradiation levels were 5×10^{11}n/cm^2, 2×10^{12}n/cm^2, and 1×10^{13}n/cm^2. As neutron irradiation activates many of the heavier elements found in a packaged integrated circuit, the parts exposed at the higher neutron levels required (as expected) some cooldown time before being shipped back to Renesas (Palm Bay, FL) for electrical testing.

1.2 Test Fixturing

No formal irradiation test fixturing is involved, as these DD tests are bag tests in the sense that the parts are irradiated with all leads unbiased.

1.3 Radiation Dosimetry

Table 2 shows dosimetry from UMASS Lowell, indicating the total accumulated gamma dose and actual neutron fluence exposure levels for each set of samples.

Table 2. ISL71610x Neutron Fluence Dosimetry Data

Irradiation	Requested Fluence (n/cm^2)	Reactor Power (kW)	Time (s)	Flux (n/cm^2-s)[1][2]	Gamma Dose (rad(Si))[3]	Measured Fluence (n/cm^2)[4]
CRF#77981-B	5.00E+11	50	131	3.83E+09	75	5.30E+11
CRF#77981-C	2.00E+12	80	327	6.12E+09	298	2.33E+12
CRF#77981-D	1.00E+13	1000	131	7.65E+10	1492	1.04E+13

1. Dosimetry method: ASTM E-265
2. The neutron fluence rate is determined from *Initial Testing of the New Ex-Core Fast Neutron Irradiator at UMass Lowell* (6/18/02). Validated on 6/07/2011 under the Trident II D5LE neutron facility study by Navy Crane.
3. Based on reactor power at 1000kW, the gamma dose is 41 ±5.3%krad(Si)/hr as mapped by TLD-based dosimetry.
4. Validated by S-32 flux monitors.

1.4 Characterization Equipment and Procedures

Electrical testing was performed before and after irradiation using the Renesas production automated test equipment (ATE). All electrical testing was performed at room temperature.

1.5 Experimental Matrix

Testing proceeded in general accordance with the guidelines of MIL-STD-883 TM 1017. The experimental matrix consisted of six samples to be irradiated at 5×10^{11}n/cm^2, six at 2×10^{12}n/cm^2, and six at 1×10^{13}n/cm^2. The actual levels achieved, shown in Table 2, were 5.3×10^{11}n/cm^2, 2.3×10^{12}n/cm^2, and 1×10^{13}n/cm^2. Two control units were used.

The 18 ISL71710x samples were drawn from Lot 224201. Samples were packaged in the standard 8 Ld 5mm×4mm SOIC package. Samples were processed through burn-in before irradiation and screened to the datasheet limits at room, low, and high temperatures before neutron testing.

2. Test Results

2.1 Attributes Data

Neutron testing of the ISL71710x is complete, and the results, summarized in Table 3, are reported in the balance of this report. It should be understood when interpreting the data that each neutron irradiation was performed on a different set of samples; this is not total dose testing, where the damage is cumulative.

Table 3. ISL71710x Attributes Data

1MeV Fluence, (n/cm^2)		Sample Size	Pass[1]	Fail	Notes
Planned	Actual				
5×10^{11}	5.30×10^{11}	6	6	0	All passed
2×10^{12}	2.33×10^{12}	6	6	0	All passed
1×10^{13}	1.04×10^{13}	6	6	0	All passed

1. A Pass indicates a sample that passes all post-irradiation datasheet limits.

2.2 Key Parameter Variables Data

The plots in Figure 3 through Figure 17 show data plots for key parameters before and after irradiation to each level. The plots show the mean of each parameter as a function of neutron irradiation. The plots also include error bars at each down-point, representing the minimum and maximum measured values of the samples. However, in some plots, the error bars might not be visible due to their values compared to the scale of the graph. While the applicable electrical limits taken from the datasheet are also shown, it should be noted that these limits are provided for guidance only as the ISL71710x is not specified for the neutron environment.

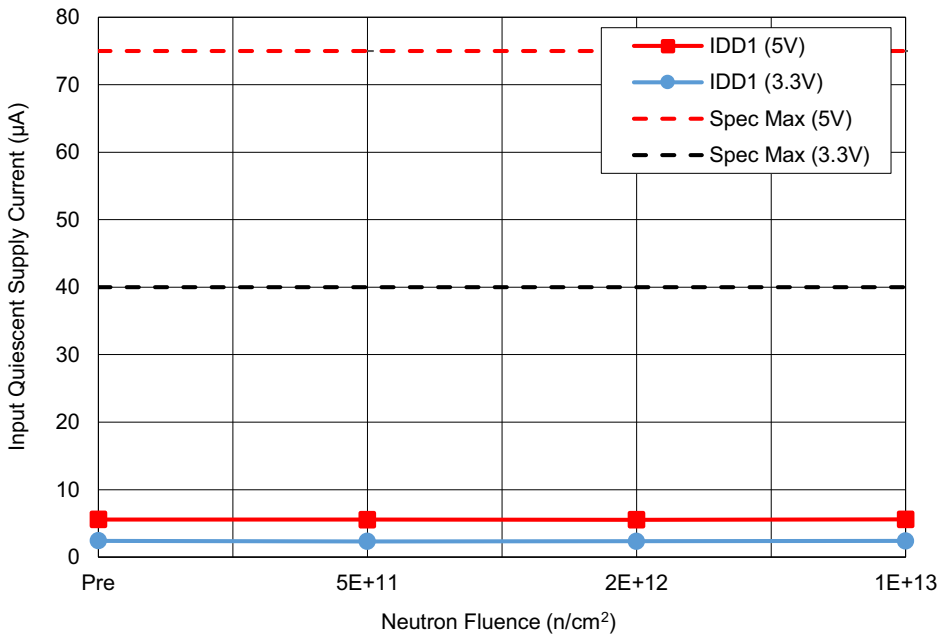

Figure 3. ISL71710x input quiescent supply current (I_{DD1}) with $V_{DD1} = V_{DD2} = 3.3V$ and 5V as a function of neutron fluence. The error bars represent the minimum and maximum measured values. The datasheet limits are 40µA maximum at 3.3V and 75µA maximum at 5V.

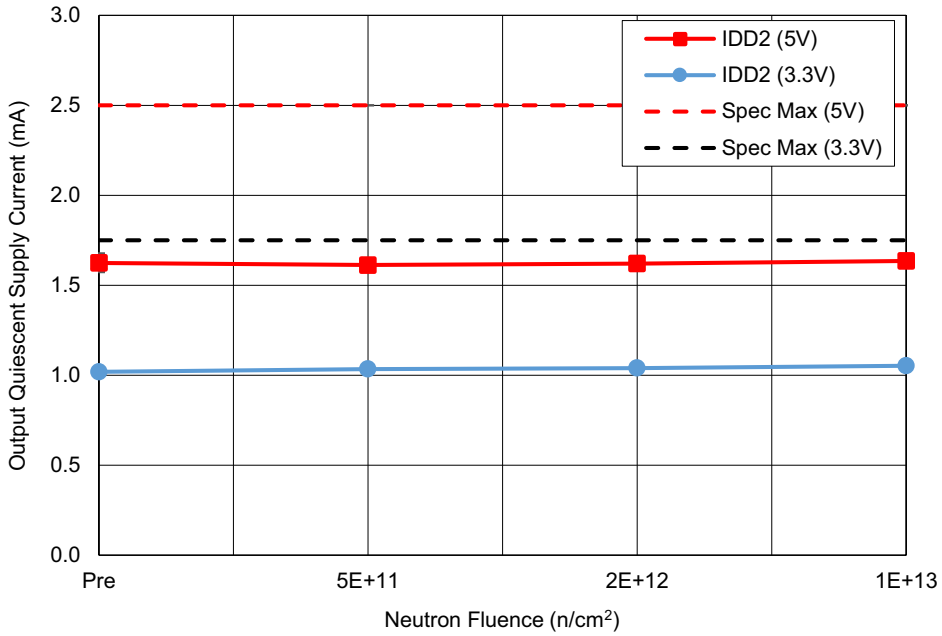

Figure 4. ISL71710x average output quiescent supply current (I_{DD2}) with V_{DD1} = V_{DD2} = 3.3V and 5V as a function of neutron fluence. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limits are 1.75mA maximum at 3.3V and 2.5mA maximum at 5V.

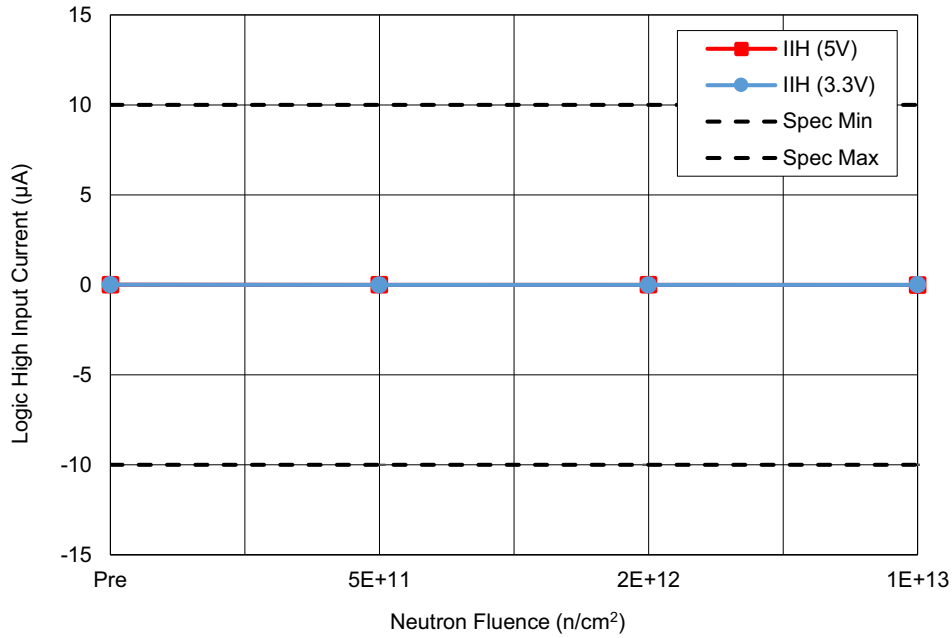

Figure 5. ISL71710x logic input current (I_I) with V_{DD1} = V_{DD2} = 3.3V and 5V as a function of neutron fluence. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limits are -10µA minimum and 10µA maximum.

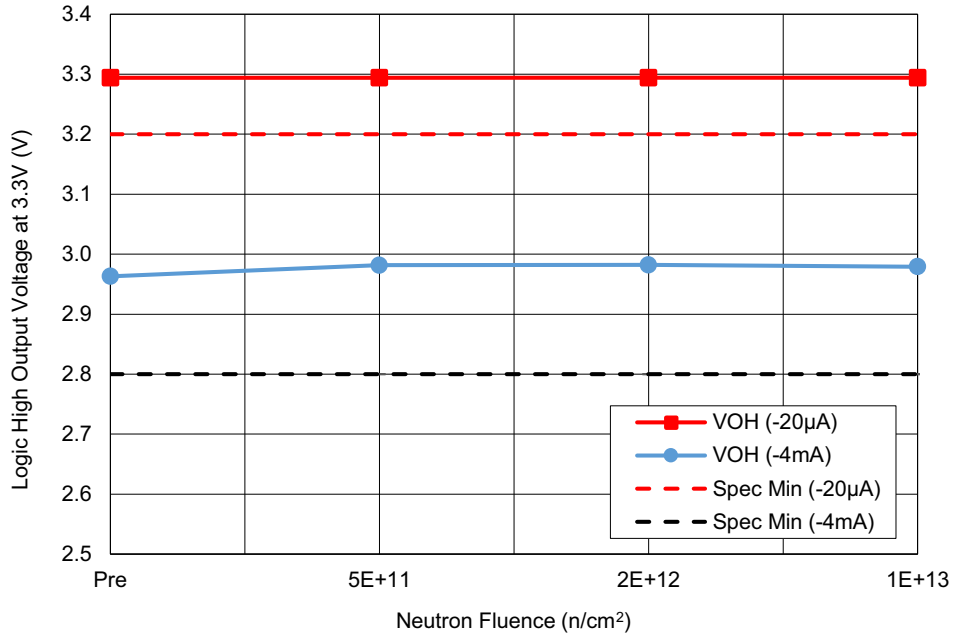

Figure 6. ISL71710x average logic high output voltage (V_{OH}) with V_{DD1} = V_{DD2} = 3.3V and I_O = -20µA and -4mA as a function of neutron fluence. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limits are 3.2V minimum for -20µA and 2.8V minimum for -4mA.

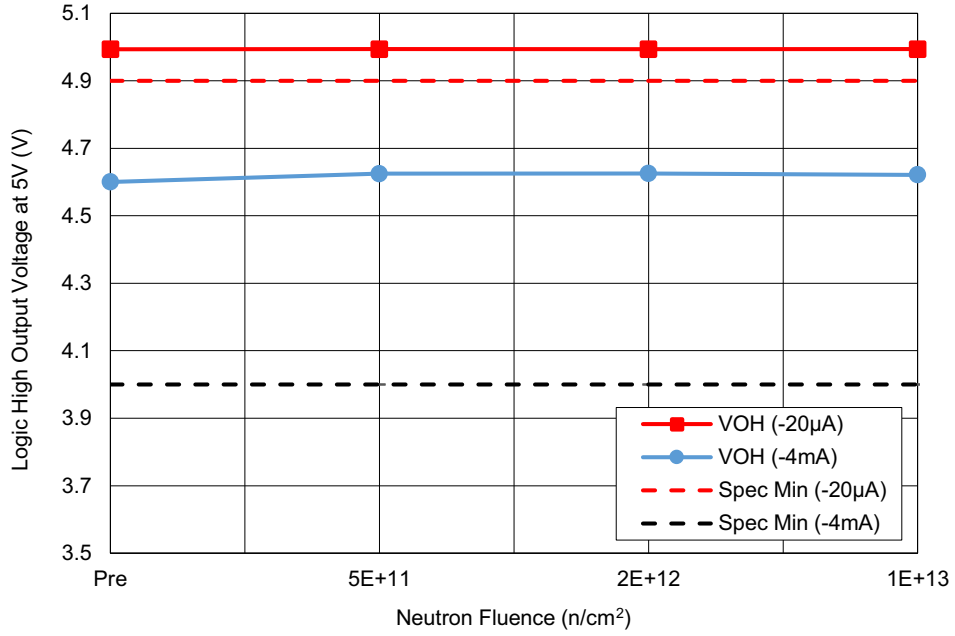

Figure 7. ISL71710x average logic high output voltage (V_{OH}) with V_{DD1} = V_{DD2} = 5V and I_O = -20µA and -4mA as a function of neutron fluence. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limits are 4.9V minimum for -20µA and 4V minimum for -4mA.

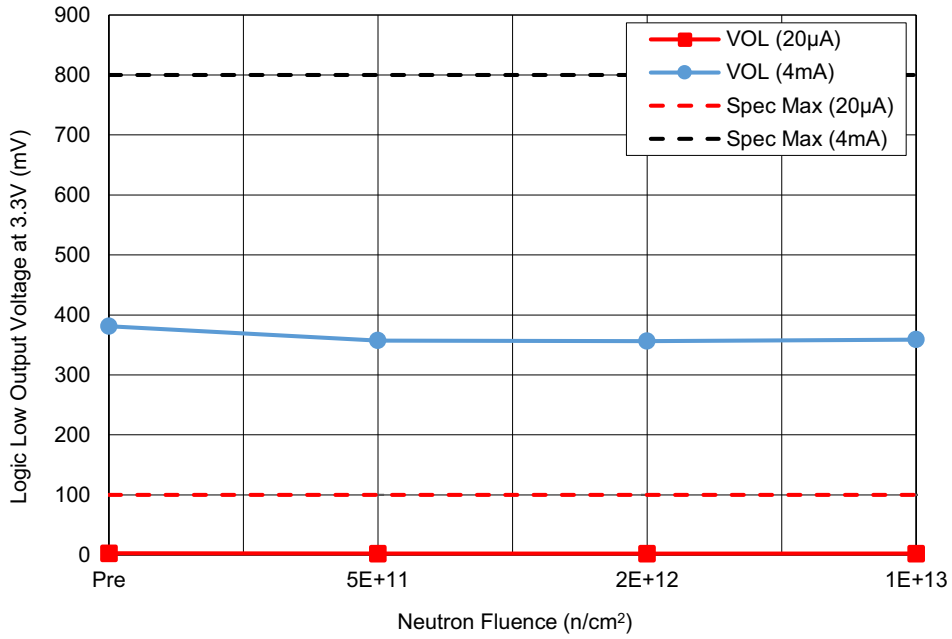

Figure 8. ISL71710x average logic low output voltage (V_{OL}) with V_{DD1} = V_{DD2} = 3.3V and I_O = 20µA and 4mA as a function of neutron fluence. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limits are 800mV maximum for 20µA and 100mV maximum for 4mA.

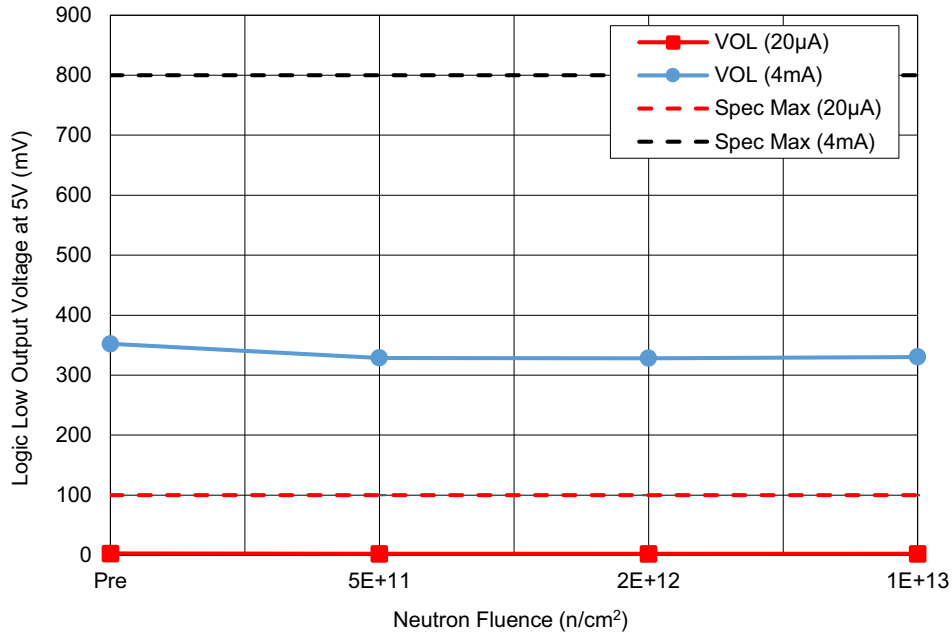

Figure 9. ISL71710x average logic low output voltage (V_{OL}) with V_{DD1} = V_{DD2} = 5V and I_O = 20µA and 4mA as a function of neutron fluence. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limits are 800mV maximum for 20µA and 100mV maximum for 4mA.

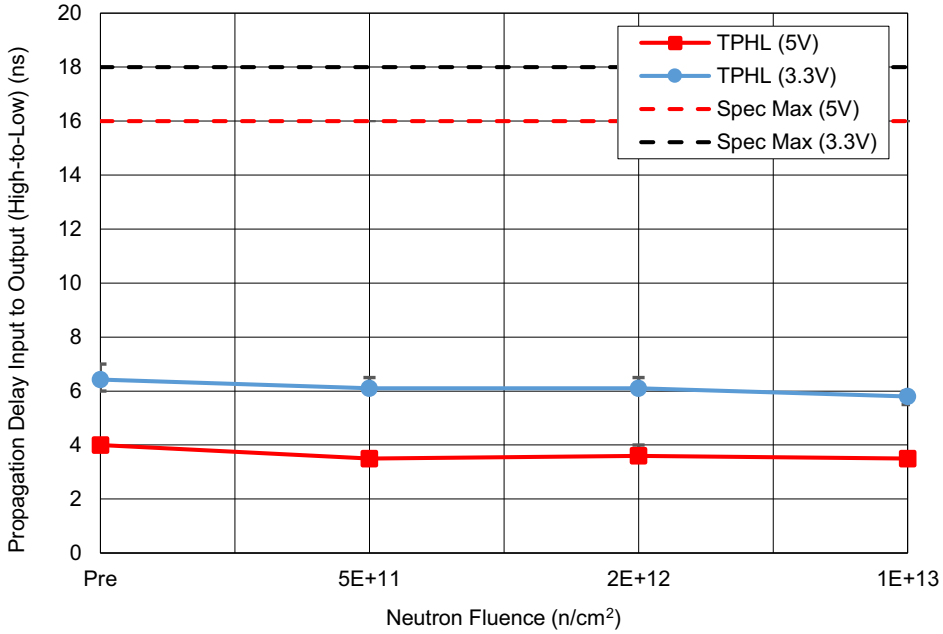

Figure 10. ISL71710x average propagation delay, input to output, high to low (t_{PHL}) with V_{DD1} = V_{DD2} = 3.3V and 5V, C_L = 15pF as a function of neutron fluence. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limits are 18ns maximum for 3.3V and 16ns maximum for 5V.

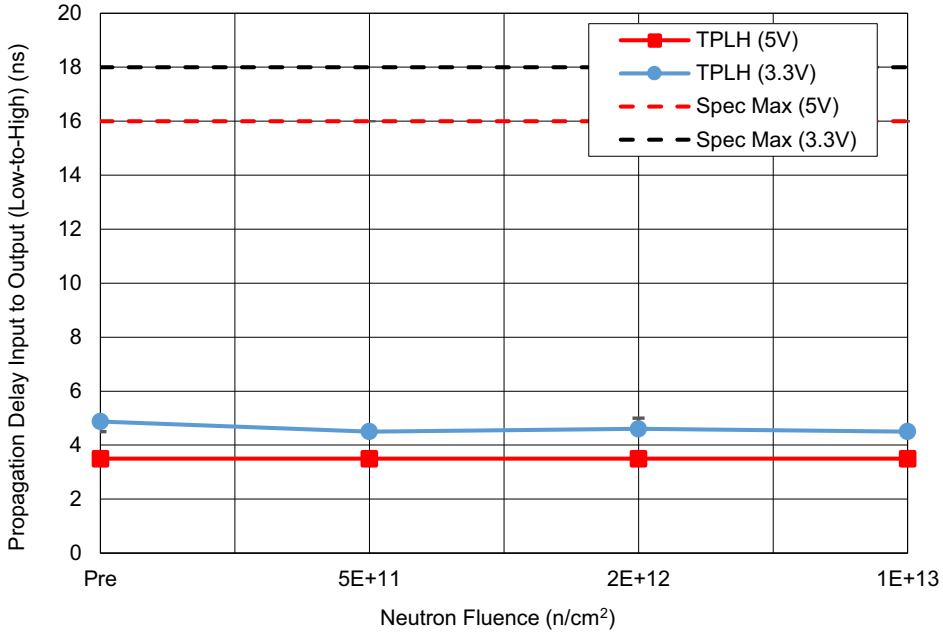

Figure 11. ISL71710x average propagation delay, input to output, low to high (t_{PLH}) with V_{DD1} = V_{DD2} = 3.3V and 5V, C_L = 15pF as a function of neutron fluence. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limits are 18ns maximum for 3.3V and 16ns maximum for 5V.

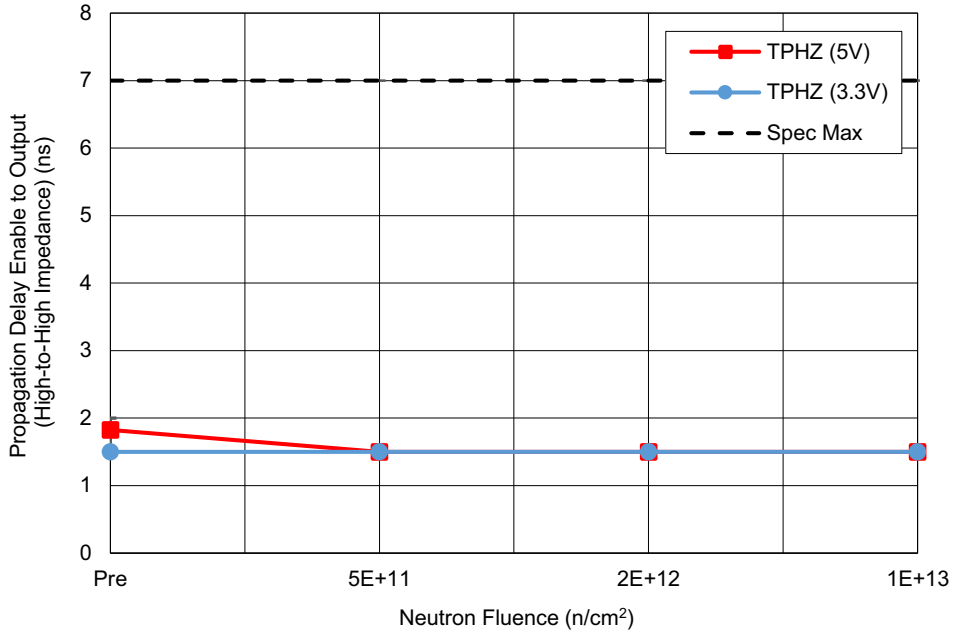

Figure 12. ISL71710x average propagation delay, enable to output, high-to-high impedance (t_{PHZ}) with V_{DD1} = V_{DD2} = 3.3V and 5V, C_L = 15pF as a function of neutron fluence. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limit is 7ns maximum.

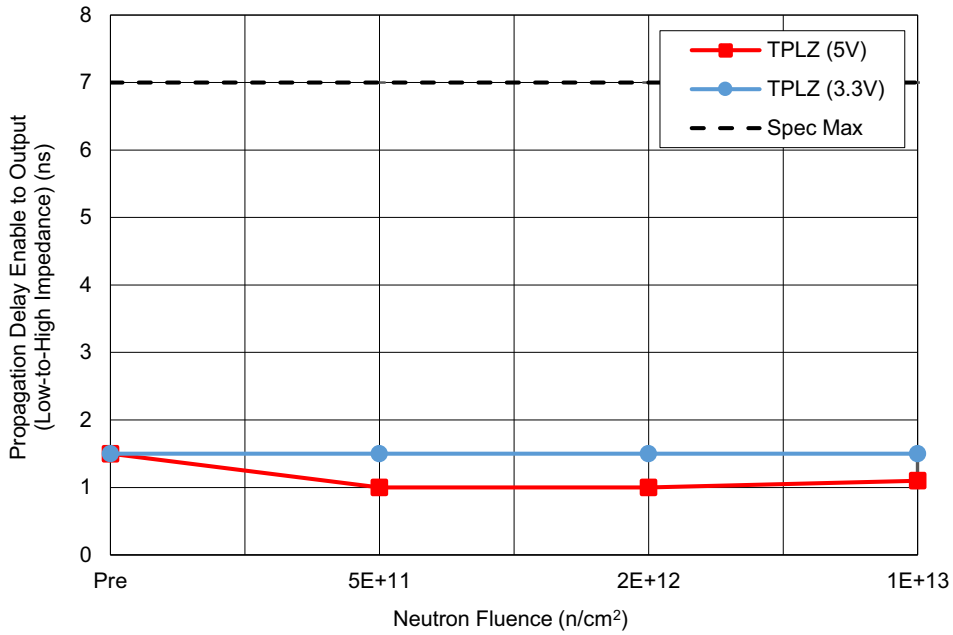

Figure 13. ISL71710x average propagation delay, enable to output, low-to-high impedance (t_{PLZ}) with V_{DD1} = V_{DD2} = 3.3V and 5V, C_L = 15pF as a function of neutron fluence. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limit is 7ns maximum.

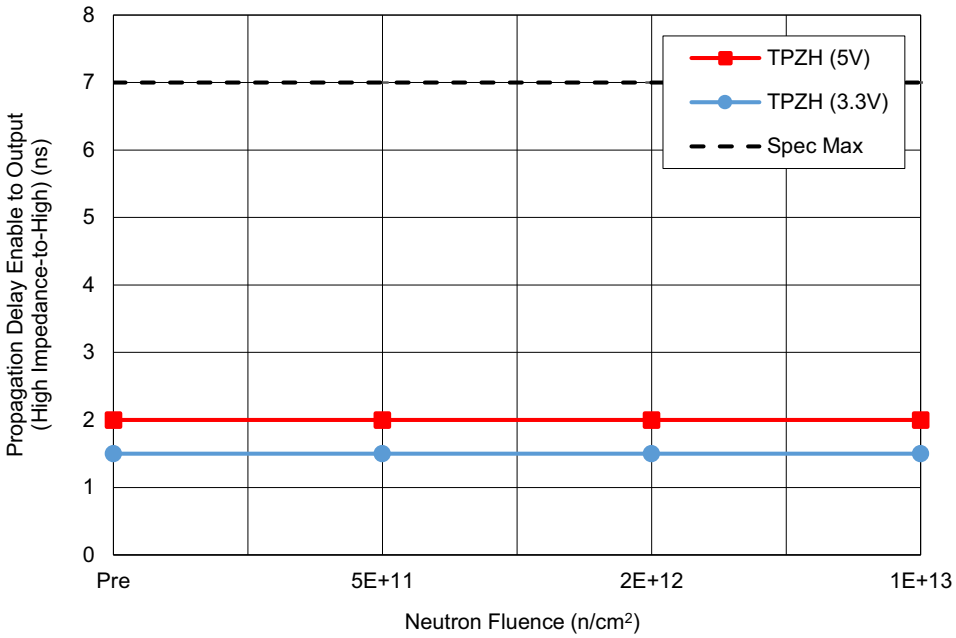

Figure 14. ISL71710x average propagation delay, enable to output, high impedance-to-high (t_{PZH}) with V_{DD1} = V_{DD2} = 3.3V and 5V, C_L = 15pF as a function of neutron fluence. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limit is 7ns maximum.

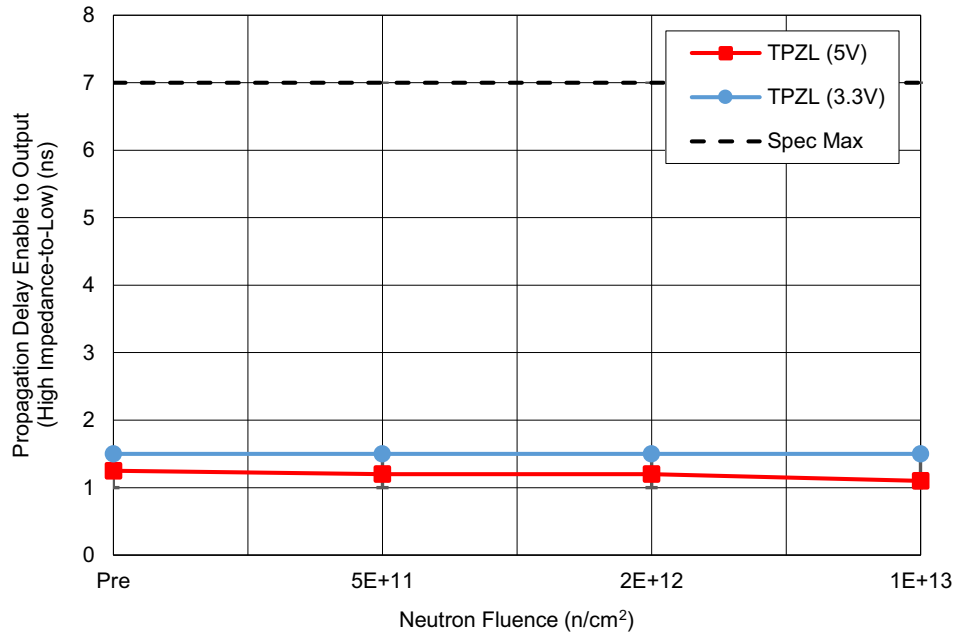

Figure 15. ISL71710x average propagation delay, enable to output, high impedance-to-low (t_{PZL}) with V_{DD1} = V_{DD2} = 3.3V and 5V, C_L = 15pF as a function of neutron fluence. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limit is 7ns maximum.

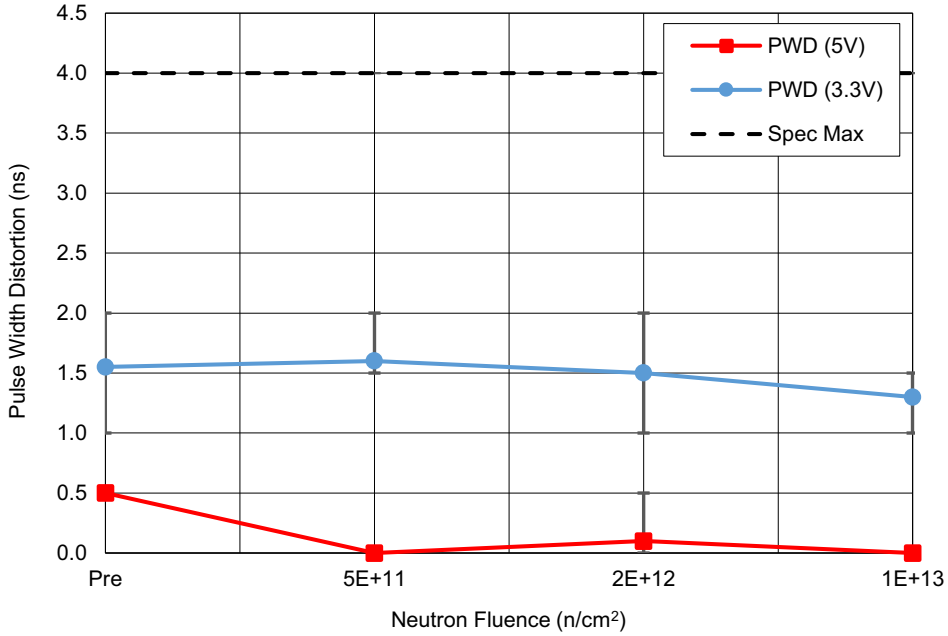

Figure 16. ISL71710x average pulse width distortion (PWD) with V_{DD1} = V_{DD2} = 3.3V and 5V, C_L = 15pF as a function of neutron fluence. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limit is 4ns maximum.

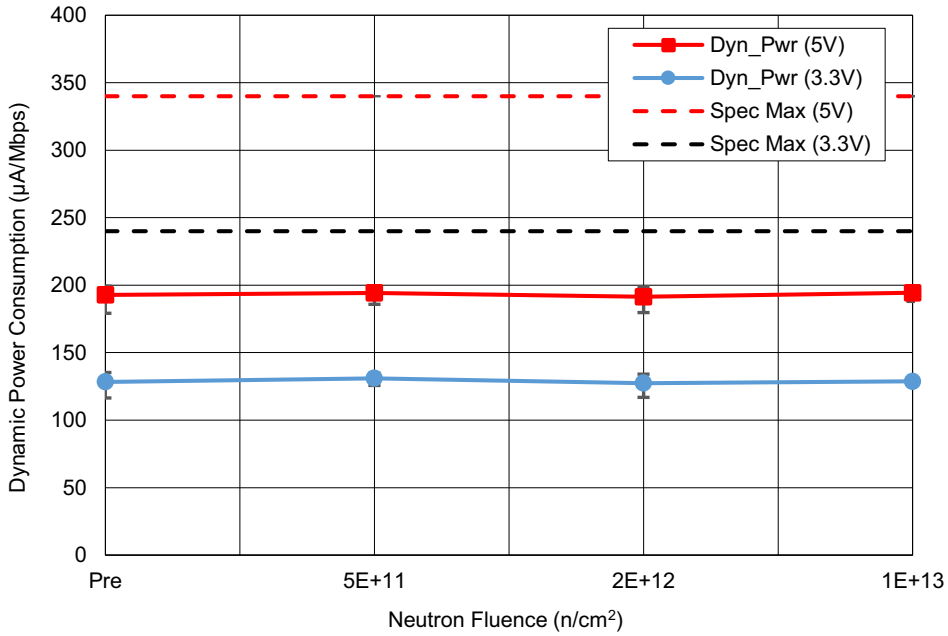

Figure 17. ISL71710x average dynamic power consumption with V_{DD1} = V_{DD2} = 3.3V and 5V as a function of neutron fluence. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limits are 240µA/Mbps maximum for 3.3V and 340µA/Mbps maximum for 5V.

3. Discussion and Conclusion

We report the 1MeV equivalent neutron testing of the ISL71710x radiation tolerant passive-input digital isolator. Parts were tested at actual fluences of 5.30×10^{11}n/cm^2, 2.33×10^{12}n/cm^2, and 1.04×10^{13}n/cm^2. The results of key parameters before and after irradiation to each level are plotted in Figure 3 through Figure 17. The plots show the mean of each parameter as a function of neutron irradiation, with error bars that represent the minimum and maximum measured values. The figures also show the applicable electrical limits taken from the datasheet, but it should be noted that these limits are provided for guidance only as the ISL71710x is not specified for the neutron environment.

All samples passed the datasheet limits with little to no degradation after all exposures up to and including 1.04×10^{13}n/cm^2.

4. Revision History

Revision	Date	Description
1.00	Jun 2, 2023	Initial release.

A. Appendix

A.1 Reported Parameters

Table 4 lists the key parameters that are considered indicative of part performance. These parameters are plotted in Figure 3 through Figure 17. All limits are taken from the ISL71710x datasheet.

Table 4. ISL71710x Key Parameters (T_A = 25°C)

Figure	Parameter	Symbol	Conditions	Low Limit	High Limit	Unit
3	Input Quiescent Supply Current	I_{DD1}	$V_{DD1} = V_{DD2} = 3.3V$	-	40	µA
			$V_{DD1} = V_{DD2} = 5V$	-	75	µA
4	Output Quiescent Supply Current	I_{DD2}	$V_{DD1} = V_{DD2} = 3.3V$	-	1.75	mA
			$V_{DD1} = V_{DD2} = 5V$	-	2.5	mA
5	Logic Input Current	I_I	$V_{DD1} = V_{DD2} = 3.3V$ and 5V	-10	10	µA
6	Logic High Output Voltage ($V_{DD1} = V_{DD2} = 3.3V$)	V_{OH}	I_O = -20µA	3.2	-	V
			I_O = -4mA	2.8	-	V
7	Logic High Output Voltage ($V_{DD1} = V_{DD2} = 5V$)		I_O = -20µA	4.9	-	V
			I_O = -4mA	4	-	V
8	Logic Low Output Voltage ($V_{DD1} = V_{DD2} = 3.3V$)	V_{OL}	I_O = 20µA	-	100	mV
			I_O = 4mA	-	800	mV
9	Logic Low Output Voltage ($V_{DD1} = V_{DD2} = 5V$)		I_O = 20µA	-	100	mV
			I_O = 4mA	-	800	mV
10	Propagation Delay Input to Output (High-to-Low)	t_{PHL}	$V_{DD1} = V_{DD2} = 3.3V$, C_L = 15pF	-	18	ns
			$V_{DD1} = V_{DD2} = 5V$, C_L = 15pF	-	16	ns
11	Propagation Delay Input to Output (Low-to-High)	t_{PLH}	$V_{DD1} = V_{DD2} = 3.3V$, C_L = 15pF	-	18	ns
			$V_{DD1} = V_{DD2} = 5V$, C_L = 15pF	-	16	ns
12	Propagation Delay Enable to Output (High-to-High Impedance)	t_{PHZ}	$V_{DD1} = V_{DD2} = 3.3V$ and 5V, C_L = 15pF	-	7	ns
13	Propagation Delay Enable to Output (Low-to-High Impedance)	t_{PLZ}	$V_{DD1} = V_{DD2} = 3.3V$ and 5V, C_L = 15pF	-	7	ns
14	Propagation Delay Enable to Output (High Impedance-to-High)	t_{PZH}	$V_{DD1} = V_{DD2} = 3.3V$ and 5V, C_L = 15pF	-	7	ns
15	Propagation Delay Enable to Output (High Impedance-to-Low)	t_{PZL}	$V_{DD1} = V_{DD2} = 3.3V$ and 5V, C_L = 15pF	-	7	ns
16	Pulse-Width Distortion	PWD	$V_{DD1} = V_{DD2} = 3.3V$ and 5V, C_L = 15pF	-	4	ns
17	Dynamic Power Consumption	-	$V_{DD1} = V_{DD2} = 3.3V$	-	240	µA/Mbps
			$V_{DD1} = V_{DD2} = 5V$	-	340	µA/Mbps

A.2 Related Information

For a full list of related documents, visit our website:

- ISL71710SLHM and ISL71710M device pages
- MIL-STD-883 Test Method 1017

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.