ISL71831SEH

Total Dose Testing

TR021
Rev 0.00
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Introduction

This report provides interim results of a total dose test of the ISL71831SEH 32-channel low voltage analog multiplexer. The test was conducted in order to determine the sensitivity of the part to the total dose environment. Irradiation under bias and with all pins grounded and subsequent high temperature anneals are complete.

Part Description

The ISL71831SEH is a radiation tolerant 32-channel analog multiplexer that is fabricated using Intersil's proprietary P6SOI process technology to provide excellent latch-up performance. The part operates over a single supply range from 3V to 5.5V and has five digital address inputs plus an enable pin that can be driven with adjustable logic thresholds to select one of 32 available channels. Inactive channels are isolated from the active channel by high impedance which inhibits any interaction between them.

The ISL71831SEH's low switch ON-resistance allows for improved signal integrity and reduced power losses. The part is also designed for cold sparing, making it compatible with redundancy techniques in high reliability applications. It is designed to provide a high impedance to the analog source in a powered OFF condition, making it easy to add additional backup devices without incurring extra power dissipation. The ISL71831SEH also has analog overvoltage protection on the switch inputs that disables the switch during an overvoltage event to protect upstream and downstream devices. All inputs are electrostatic discharge (ESD) protected to 5kV Human Body Model (HBM).

The ISL71831SEH is available in a 48 Ld ceramic Quad Flatpack (CQFP) and operates across the extended temperature range of -55°C to +125°C. The ISL71830SEH is a 16-channel version of the ISL71831SEH and is available in a 28 Ld Ceramic Dual Flatpack (CDFP); please refer to the ISL71830SEH datasheet for further information.

Reference Documents

- ISL71831SEH datasheet
- Standard Microcircuit Drawing (SMD): 5962-15248
- MIL-STD-883 test method 1019

Test Description

Irradiation Facilities

Irradiation was performed using a Hopewell Designs N40 panoramic low dose rate ^{60}Co irradiator located in the Intersil Palm Bay, FL facility. The irradiations were performed at 8.554mrad(Si)/s to 9.322mrad(Si)/s in accordance with MIL-STD-883 test method 1019. A PbAl box was used to shield the test board and devices under test against low energy secondary gamma radiation. The high temperature anneal was performed under bias at +100°C for 168 hours.

Test Fixturing

Figure 1 on page 2 shows the configuration and power supply sequencing used for biased irradiation.

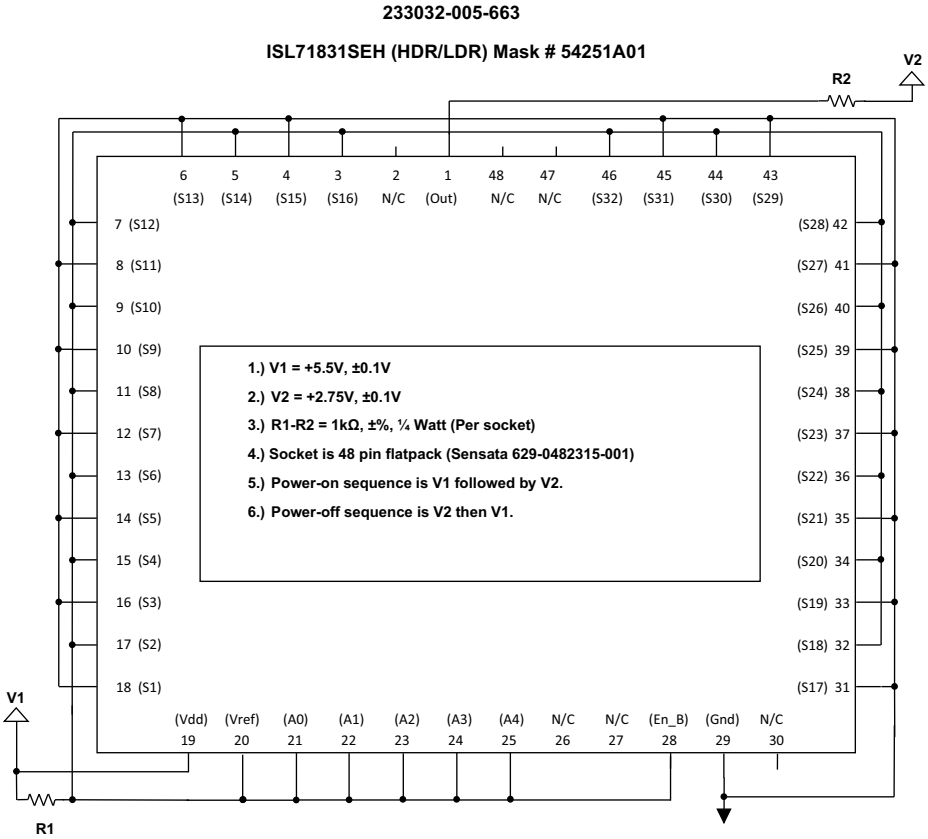

FIGURE 1. IRRADIATION BIAS CONFIGURATION AND POWER SUPPLY SEQUENCING FOR THE ISL71831SEH

Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using production automated test equipment (ATE) with data logging of all parameters at each downpoint. All downpoint electrical testing was performed at room temperature.

Experimental Matrix

Testing proceeded in accordance with the guidelines of MIL-STD-883 test method 1019. The experimental matrix consisted of 16 samples irradiated at low dose rate with all pins grounded and 16 samples irradiated at low dose rate under bias. Four control units were used.

Samples of the ISL71831SEH were drawn from development lot J69526 wafers 2, 3, 4 and 5 as part of the routine wafer-by-wafer acceptance testing procedure and were packaged in the production hermetic 48 Ld ceramic quad flatpack (package outline R48.A). The samples were processed through the standard burn-in cycle and were screened to the SMD 5962-15248 limits at room, low and high temperature before irradiation.

Downpoints

Downpoints were zero, 10krad(Si), 30krad(Si), 50krad(Si) and 75krad(Si). All samples were subjected to a high temperature biased anneal for 168 hours at +100°C following irradiation.

Results

Attributes Data

Total dose testing of the ISL71831SEH is complete and showed no reject devices after irradiation up to 75krad(Si) or after the post-75krad(Si) irradiation anneal. Table 1 summarizes the results.

TABLE 1. ISL71831SEH TOTAL DOSE TEST ATTRIBUTES DATA

DOSE RATE	BIAS	SAMPLE SIZE	DOWNPOINT	BIN 1 (Note 1)	REJECTS
8.554mrad(Si)/s to 9.322mrad(Si)/s	Figure 1	16	Pre-irradiation	16	
			10krad(Si)	16	0
			30krad(Si)	16	0
			50krad(Si)	16	0
			75krad(Si)	16	0
			Anneal, 168h at +100°C (Note 2)	16	0
8.554mrad(Si)/s to 9.322mrad(Si)/s	Grounded	16	Pre-irradiation	16	
			10krad(Si)	16	0
			30krad(Si)	16	0
			50krad(Si)	16	0
			75krad(Si)	16	0
			Anneal, 168h at +100°C (Note 2)	16	0

NOTES:

1. Bin 1 indicates a device that passes all pre-irradiation specification limits.
2. The 168-hour anneal was performed at +100°C using the bias configuration shown in Figure 1.

Variables Data

The plots in Figures 2 through 22 show data at all downpoints. The plots show the average of key parameters as a function of total dose for each of the two irradiation conditions. Many of the plots show the total dose response of the average of these parameters, such as ON-resistance and the various leakage parameters, for each of the 32 channels in order to facilitate the interpretation of the results as well as managing the length of this report. All samples showed excellent stability over irradiation. See "Conclusion" on page 14 for further discussion.

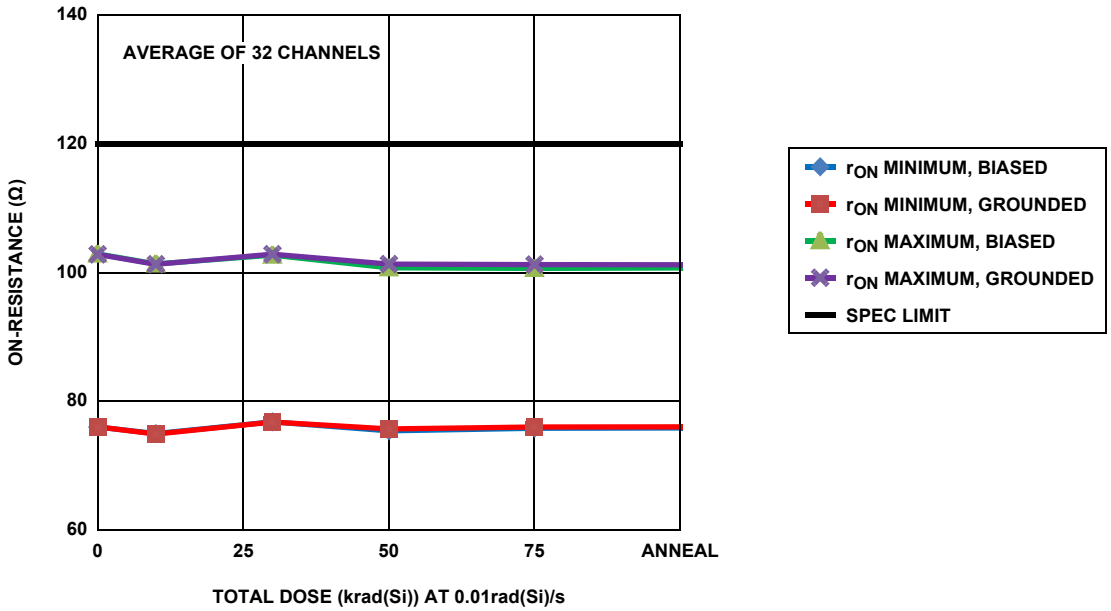

FIGURE 2. ISL71831SEH minimum and maximum switch ON-resistance, average of all 32 channels, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is 120Ω maximum.

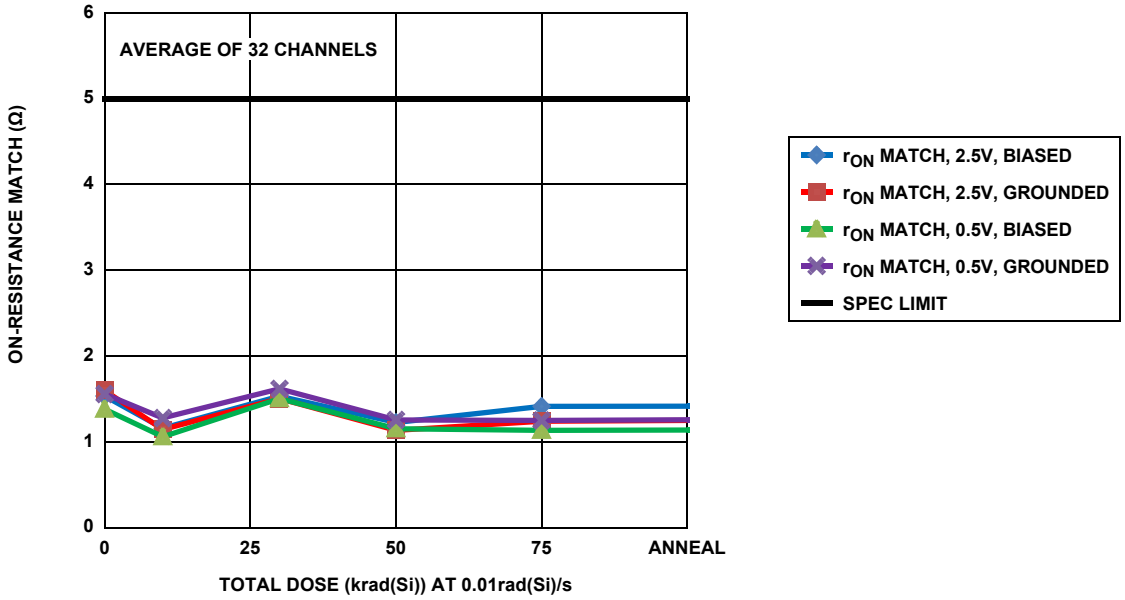

FIGURE 3. ISL71831SEH switch ON-resistance match, average of all 32 channels, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is 5Ω maximum.

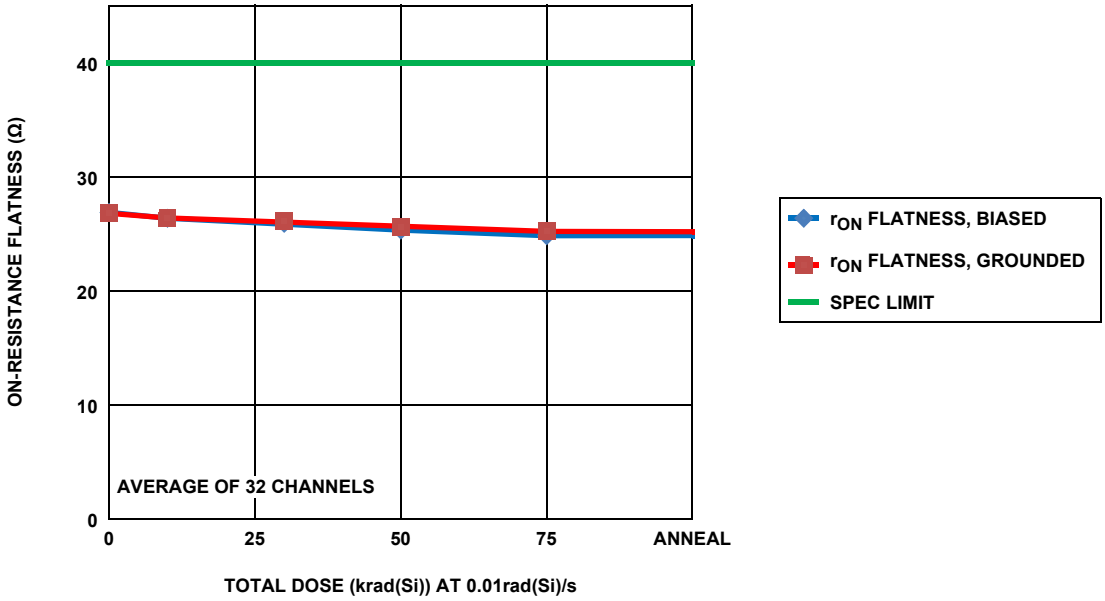

FIGURE 4. ISL71831SEH ON resistance flatness, average of all 32 channels, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is 40Ω maximum.

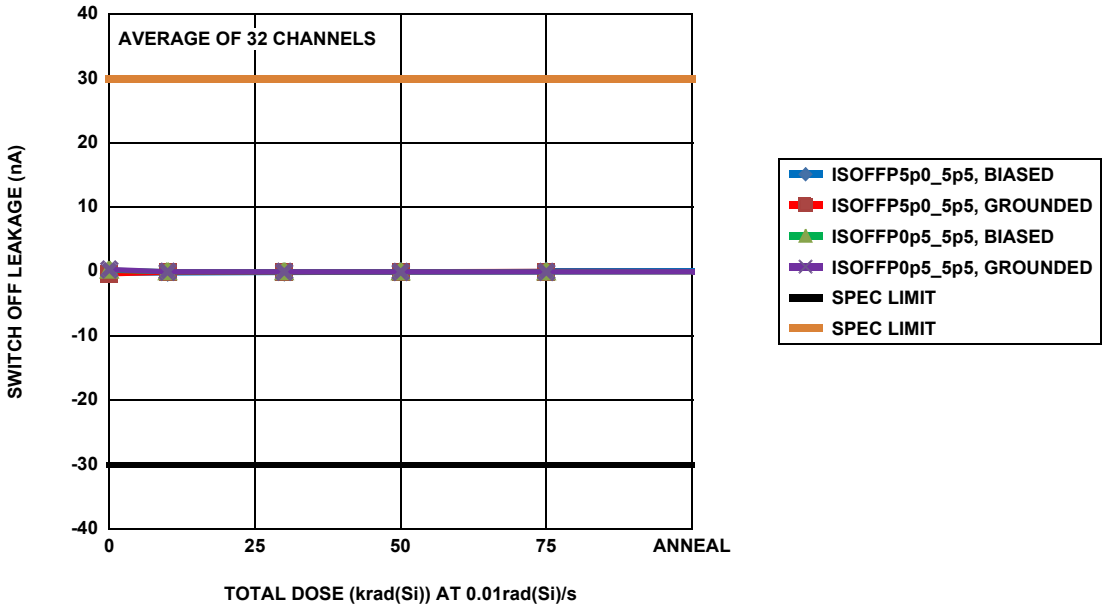

FIGURE 5. ISL71831SEH switch input OFF leakage, average of all 32 channels, 5.5V supply, input voltage to selected switch 5V or 0.5V, output and all unselected inputs at 0.5V, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is -30nA to 30nA.

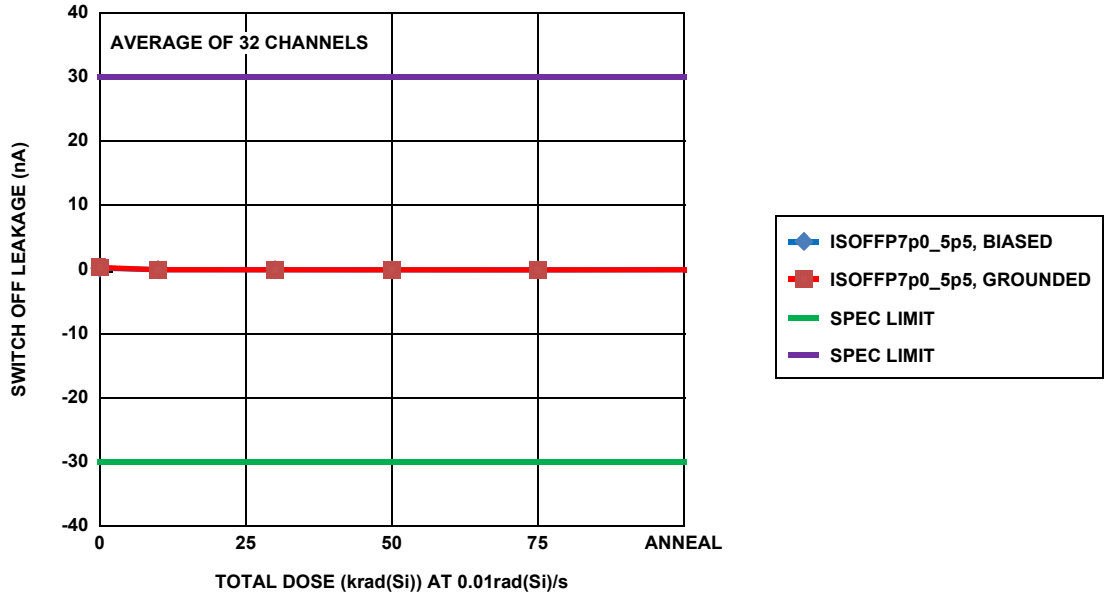

FIGURE 6. ISL71831SEH switch input overvoltage OFF leakage, average of all 32 channels, 5.5V supply, input voltage to selected switch 7V, output and all unselected inputs at 0V, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is -30nA to 30nA.

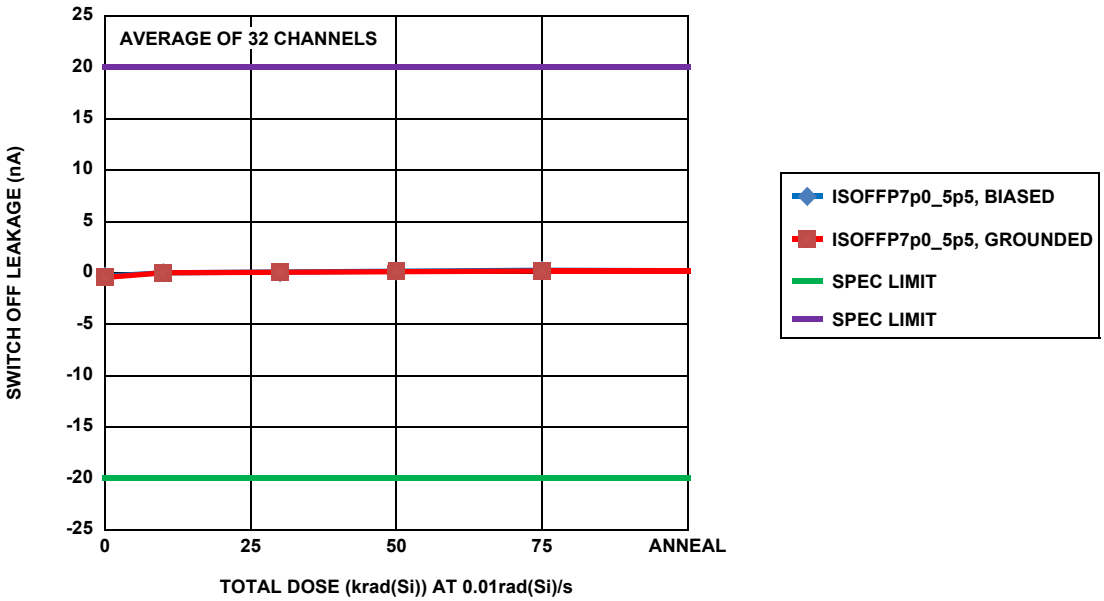

FIGURE 7. ISL71831SEH 'supplies off' switch OFF leakage into the input of an unselected channel, average of all 32 channels, supplies, address pins, enable pin and unselected inputs grounded, input voltage to selected switch 7V, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is -20nA to 20nA.

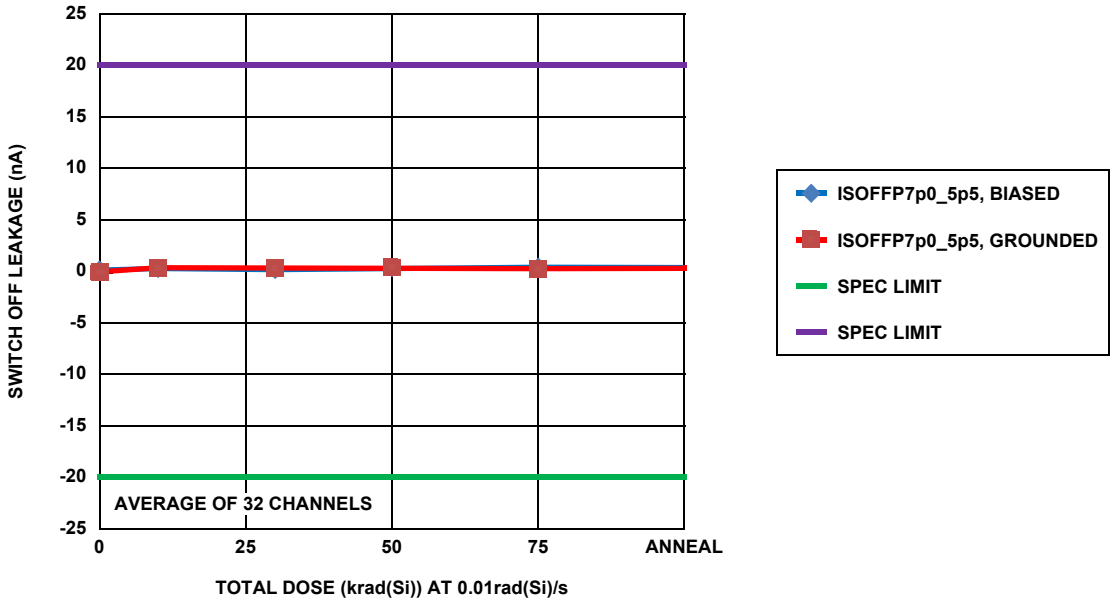

FIGURE 8. ISL71831SEH 'supplies open' switch OFF leakage into the input of an unselected channel, supplies, address pins, enable pin and unselected inputs grounded, input voltage to selected switch 7V, average of all 32 channels, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is -20nA to 20nA.

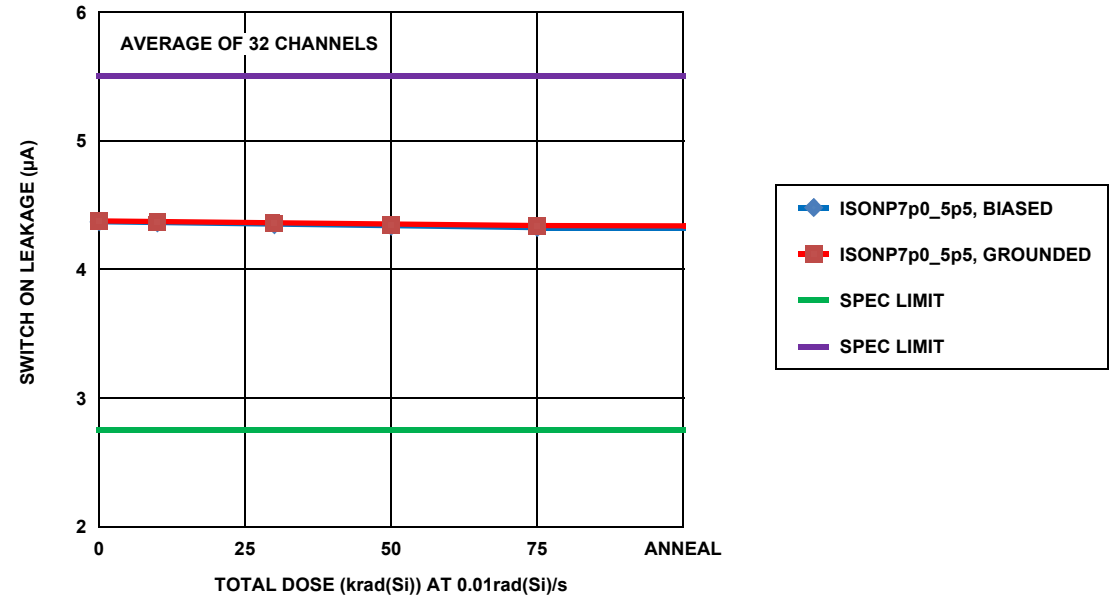

FIGURE 9. ISL71831SEH 'overvoltage' switch ON leakage into a selected channel, average of all 32 channels, 5.5V supply, input voltage to selected switch 7V, output open, unselected inputs at 0.0V, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is 2.75µA to 5.5µA.

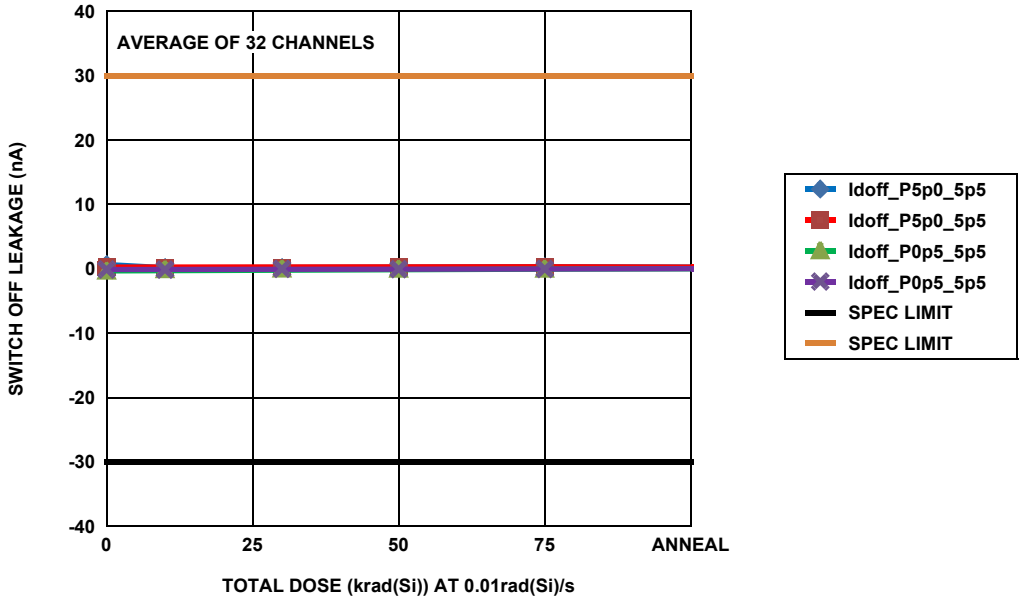

FIGURE 10. ISL71831SEH switch OFF leakage into the multiplexer output, average of all 32 channels, 5.5V supply, input voltage 0.5V or 5V, output voltage 5V or 0.5V, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is -30nA to 30nA.

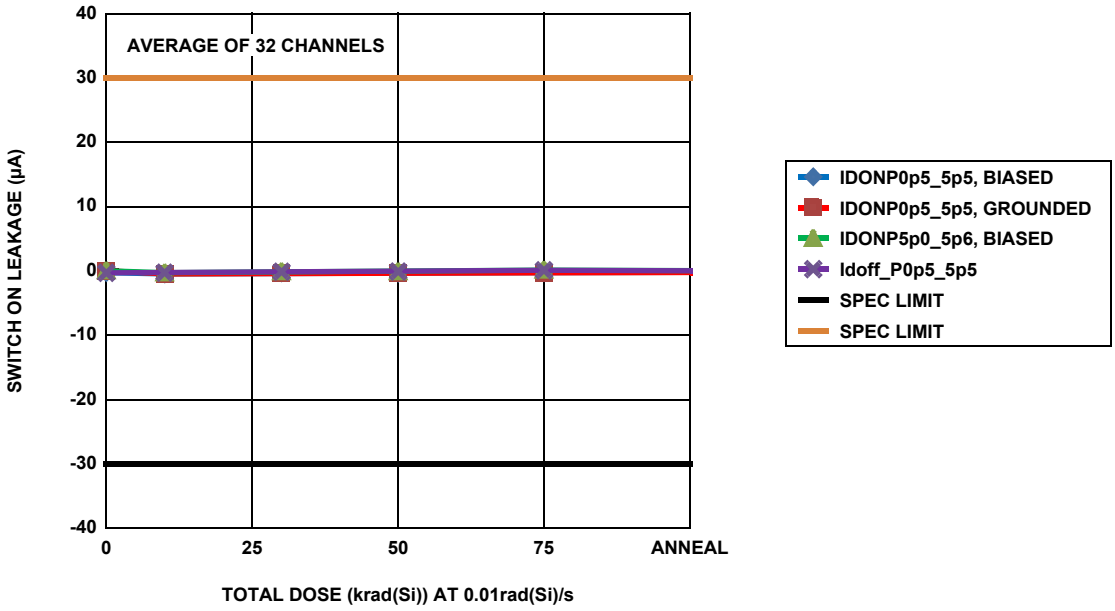

FIGURE 11. ISL71831SEH switch ON leakage into the input and output for a selected switch, average of all 32 channels, 5.5V supply, selected input and output at 0.5V or 5V, unselected inputs at 5V or 0.5V, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is -30nA to 30nA.

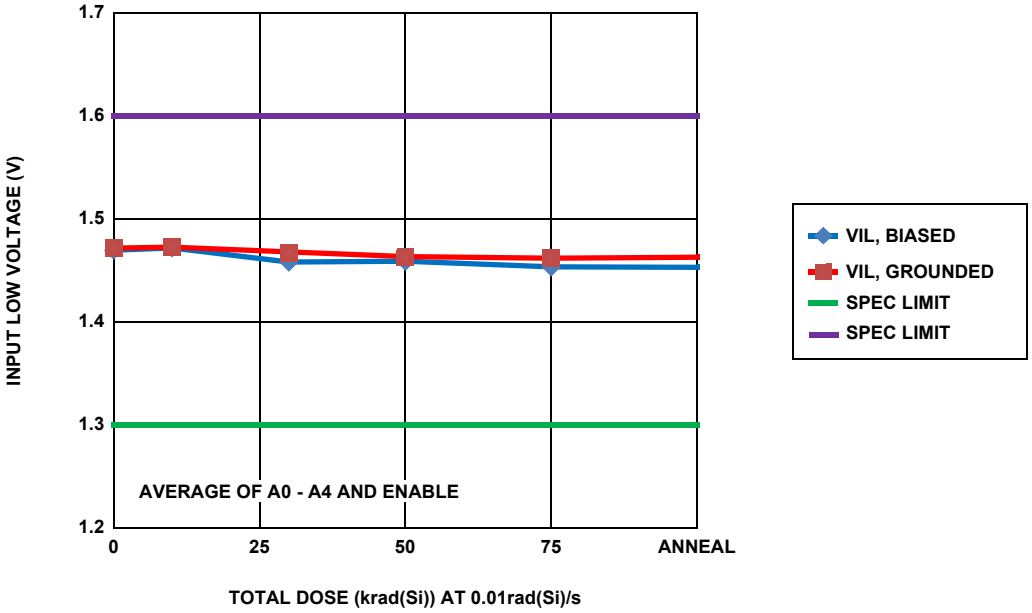

FIGURE 12. ISL71831SEH input LOW voltage, average of address pins A0 through A4 and Enable pin, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limits are 1.3V to 1.6V.

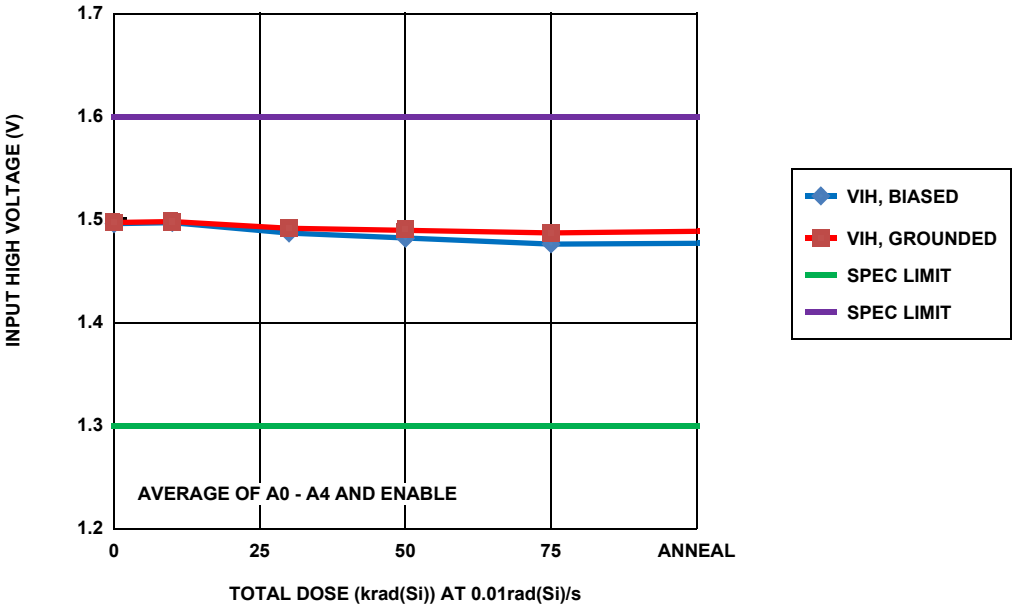

FIGURE 13. ISL71831SEH input HIGH voltage, average of address pins A0 through A4 and Enable pin, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limits are 1.3V to 1.6V.

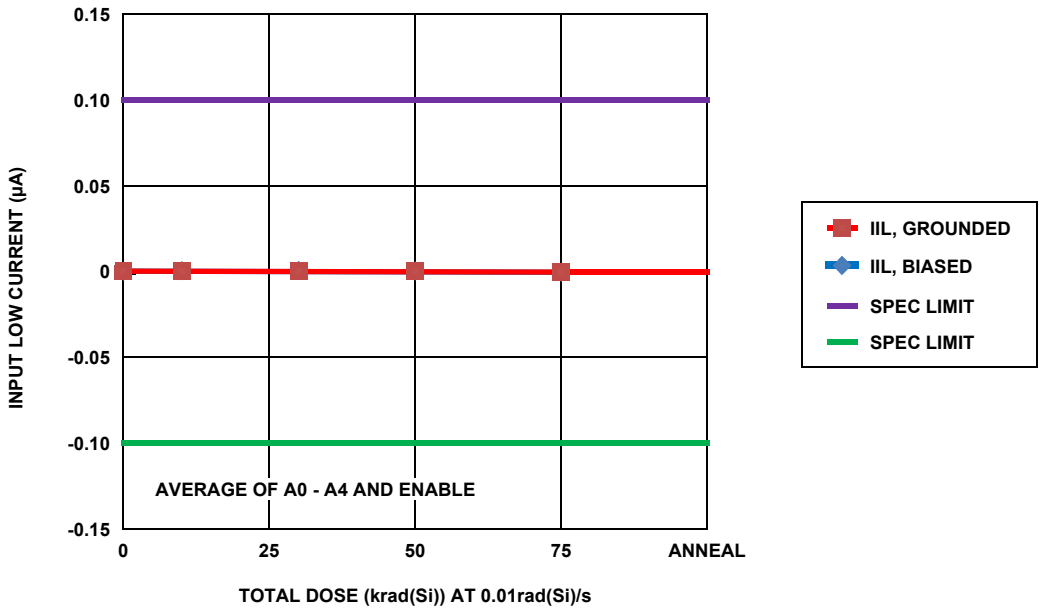

FIGURE 14. ISL71831SEH input LOW current, average of address pins A0 through A4 and Enable pin, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limits are -0.1µA to 0.1µA.

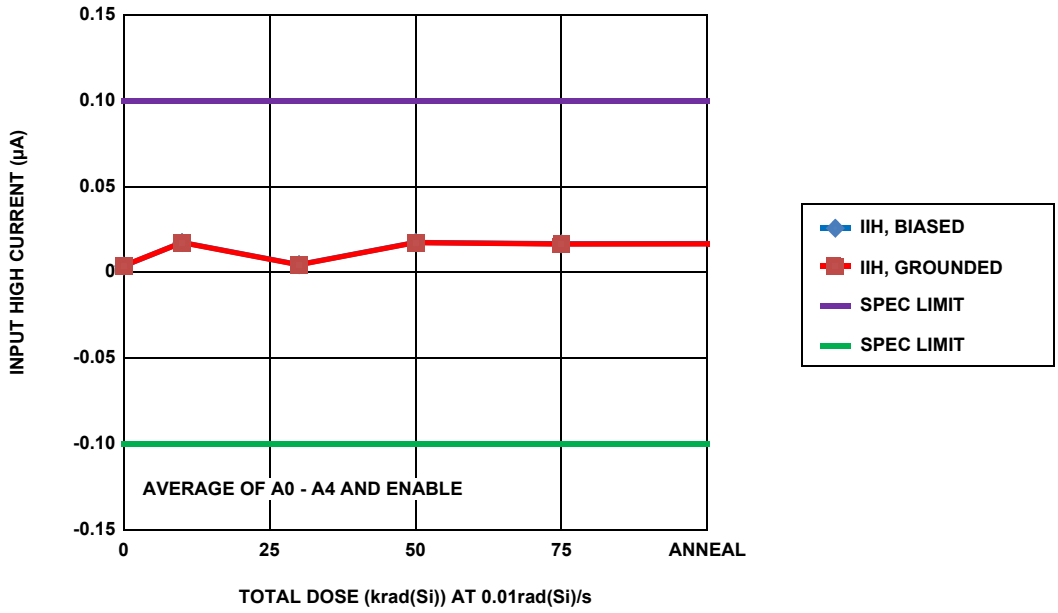

FIGURE 15. ISL71831SEH input HIGH current, average of address pins A0 through A4 and Enable pin, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limits are -0.1µA to 0.1µA.

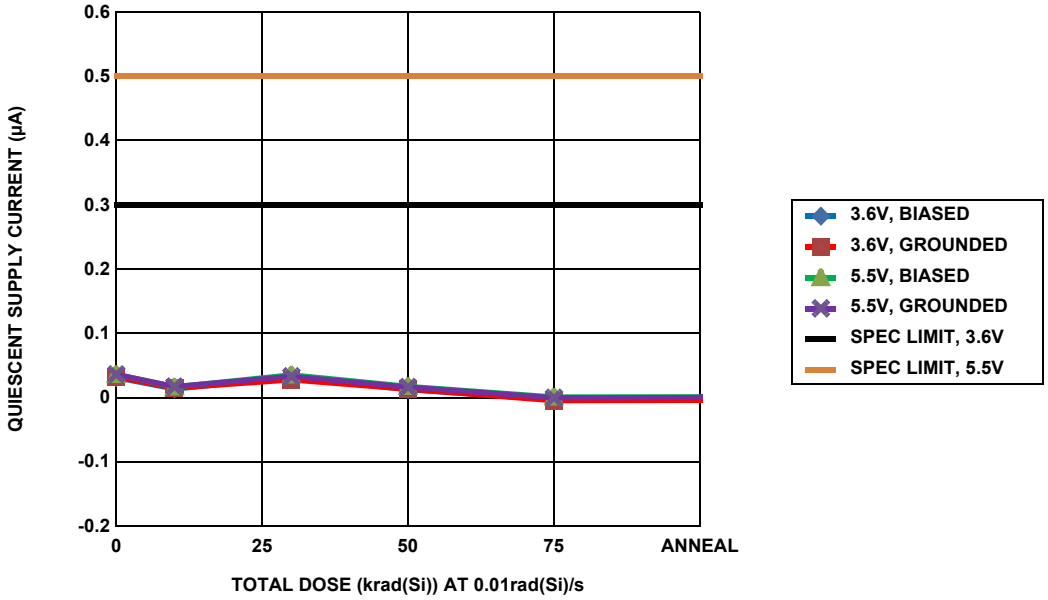

FIGURE 16. ISL71831SEH quiescent supply current, 3.6V and 5.5V supply and VREF voltage, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limits are 0.3µA maximum (3.6V) and 0.5µA (5.5V).

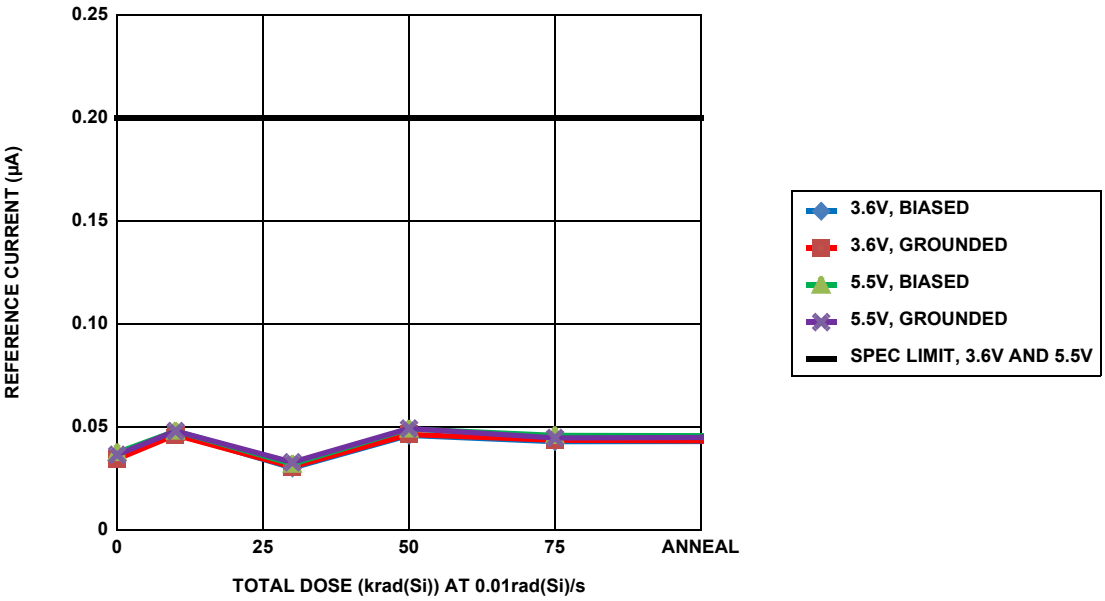

FIGURE 17. ISL71831SEH reference supply current, 3.6V and 5.5V supply and VREF voltage, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is 0.2µA maximum for both voltages.

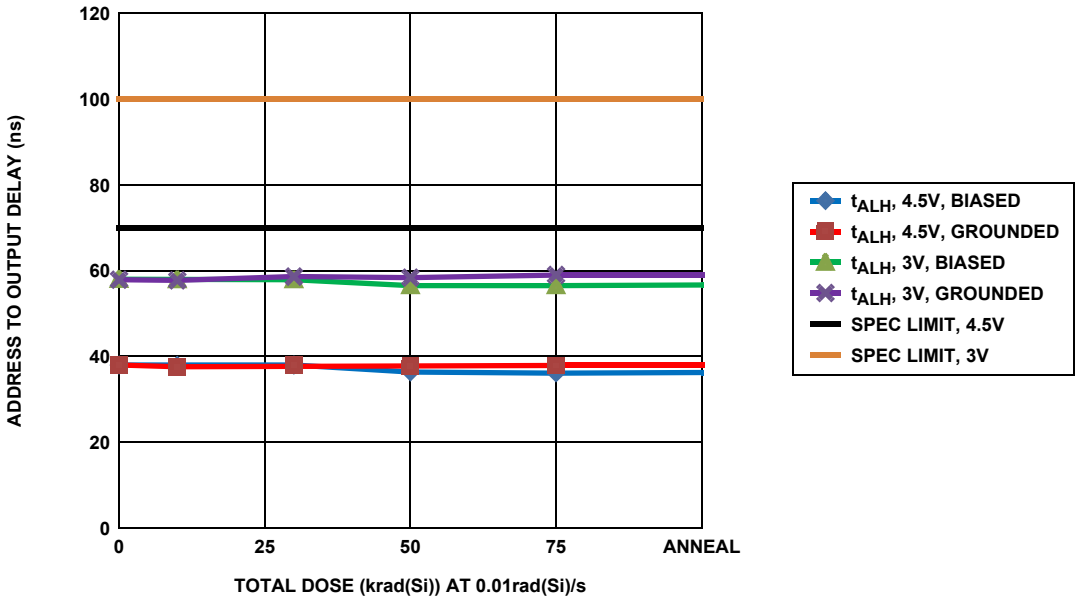

FIGURE 18. ISL71831SEH address input to multiplexer output delay, LOW to HIGH, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limits are 70ns maximum (4.5V) and 100ns maximum (3V).

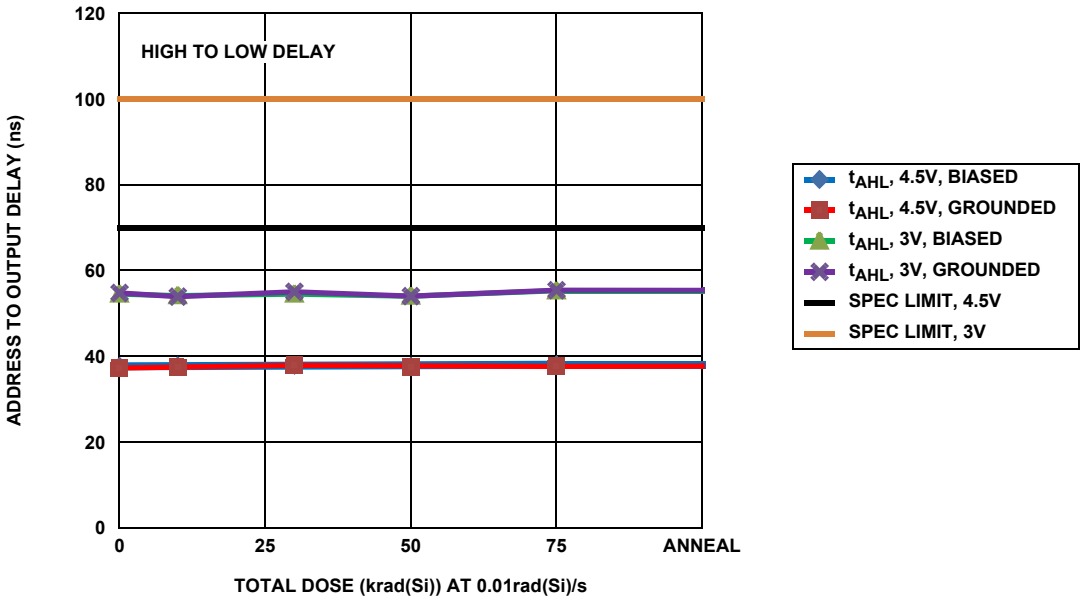

FIGURE 19. ISL71831SEH address input to multiplexer output delay, HIGH to LOW, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limits are 70ns maximum (4.5V) and 100ns maximum (3V).

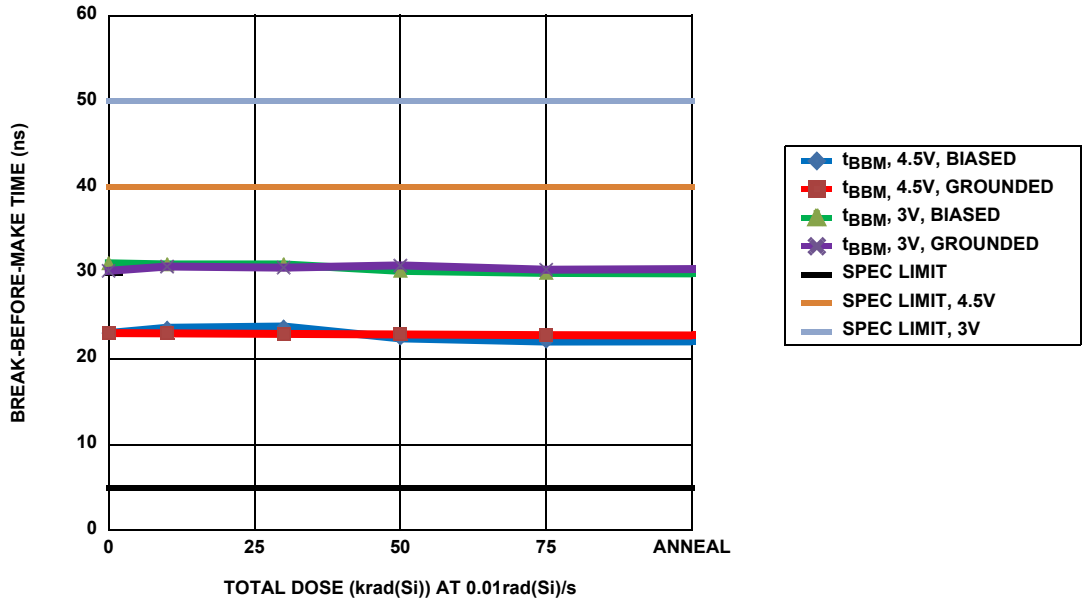

FIGURE 20. ISL71831SEH Break-Before-Make (BBM) delay as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limits are 5ns to 40ns (5.5V) and 5ns to 50ns (3V).

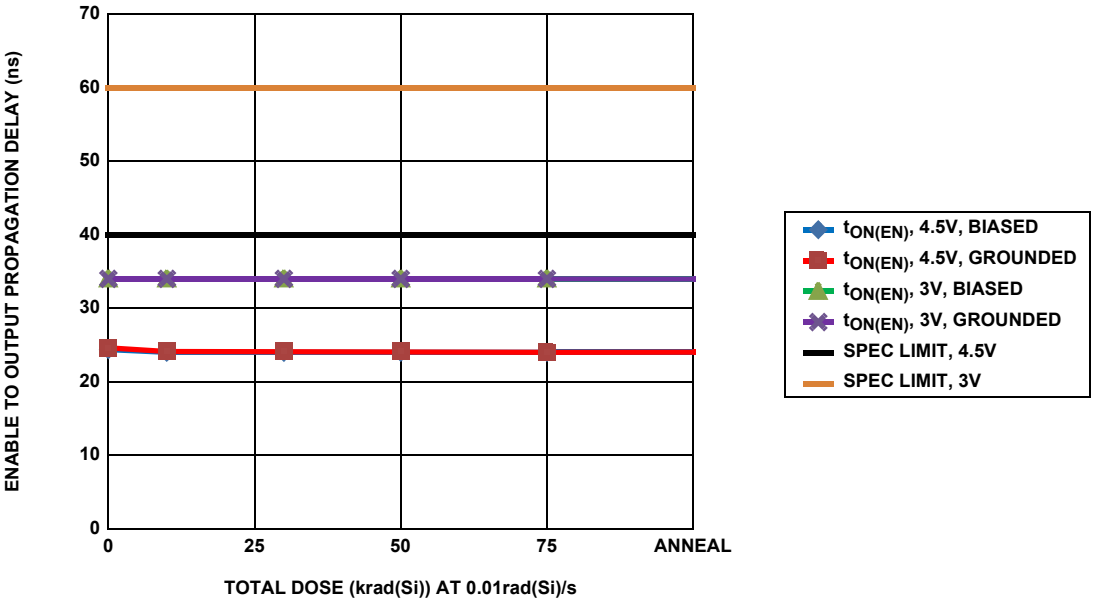

FIGURE 21. ISL71831SEH enable ON to multiplexer output propagation delay as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limits are 40ns maximum (4.5V) and 60ns maximum (3V).

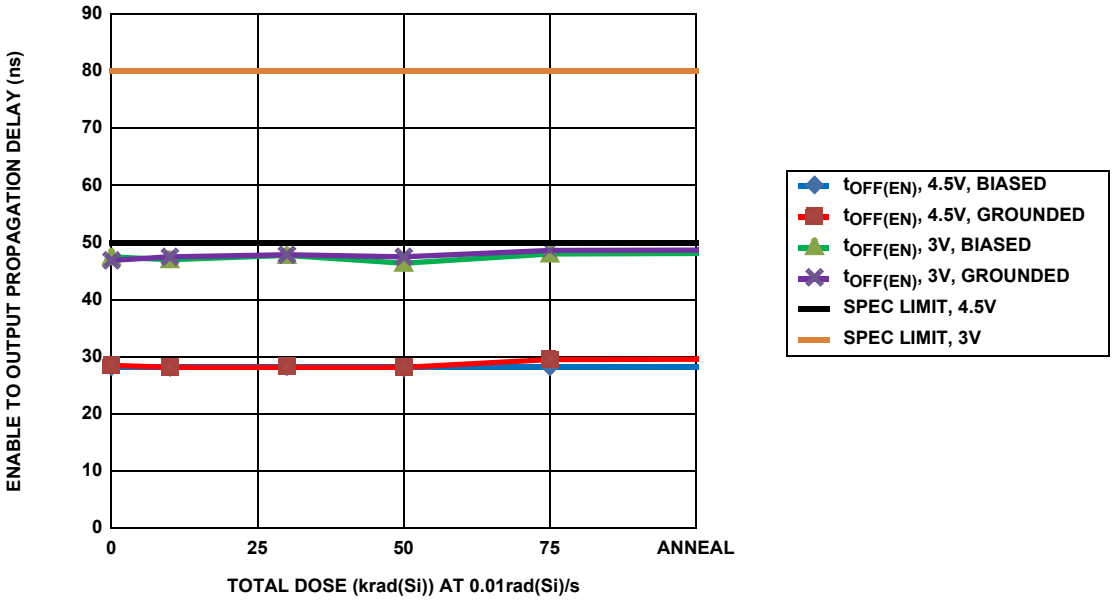

FIGURE 22. ISL71831SEH enable OFF to multiplexer output propagation delay as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limits are 50ns maximum (4.5V) and 80ns maximum (3V).

Conclusion

This document reports results of a low dose rate total dose test of the ISL71831SEH 32-channel analog multiplexer. Parts were tested at low dose rate under biased and unbiased conditions as outlined in MIL-STD-883 Test Method 1019.7. The samples were also taken through a high temperature biased anneal at +100°C for 168 hours.

ATE characterization testing at downpoints showed no rejects to the SMD Group A limits after biased and grounded irradiation at low dose rate or after the high temperature anneal. Attributes data is presented in Table 1 on page 3, while variables data for selected parameters is presented in Figures 2 through 22. All parameters showed excellent stability.

Appendices

Reported Parameters

TABLE 2. REPORTED PARAMETERS

FIGURE	PARAMETER	LIMIT, LOW	LIMIT, HIGH	UNIT	NOTES
2	Switch ON-resistance	-	120	Ω	
3	Switch ON-resistance match	-	5	Ω	
4	Switch ON-resistance flatness	-	40	Ω	
5	Switch input OFF leakage	-30	30	nA	
6	Switch input OFF leakage	-30	30	nA	Overvoltage
7	Switch input OFF leakage	-20	20	nA	Supplies grounded
8	Switch input OFF leakage	-20	20	nA	Supplies open
9	Switch input ON leakage	2.75	5.5	µA	
10	Switch output OFF leakage	-30	30	nA	
11	Switch output ON leakage	-30	30	nA	
12	Logic input LOW voltage	1.3	1.6	V	
13	Logic input HIGH voltage	1.3	1.6	V	
14	Logic input LOW current	-0.1	0.1	µA	
15	Logic input HIGH current	-0.1	0.1	µA	
16	Quiescent supply current	-	0.3/0.5	µA	3.6V and 5.5V
17	VREF supply current	-	0.2	µA	3.6V and 5.5V
18	Address input to output delay	-	100/70	ns	3V and 4.5V, LOW to HIGH
19	Address input to output delay	-	100/70	ns	3V and 4.5V, HIGH to LOW
20	Break before make delay	5	50/40	ns	3V and 4.5V
21	Enable ON to output delay	-	60/40	ns	3V and 4.5V
22	Enable OFF to output delay	-	80/50	ns	3V and 4.5V

NOTE: Limits are taken from Standard Microcircuit Drawing (SMD) 5962-15248.

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