ISL71841SEH

Single Event Effects (SEE) Testing

TR007
Rev 0.00
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Introduction

The intense proton and heavy ion environment encountered in space applications can cause a variety of Single Event Effects (SEE) in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Gate Rupture (SEGR), and Single Event Burnout (SEB). SEE can lead to system-level performance issues including disruption, degradation and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. This report discusses the results of SEE testing performed on the Intersil ISL71841SEH 32:1 analog multiplexer (MUX) designed for space applications.

Product Description

The ISL71841SEHVF is a 32:1 analog multiplexer (MUX) that operates with supply voltages from ±10.8V to ±16.5V and input overvoltage capability to ±35V. The part is also “cold spare” capable; i.e., inputs of an unpowered part do not leak more than 1µA to ±35V. The ISL71841SEHVF is fabricated in a proprietary Intersil bonded wafer SOI BiCMOS process. The ISL71841SEHVF is a 32-Channel version of the ISL71840SEHVF, 16:1 analog MUX.

Product Documentation

For more information about the ISL71841SEH, refer to the following documentation.

- Datasheets:
  - ISL71840SEH, “Radiation Hardened 30V 16-Channel Analog Multiplexer”
  - ISL71841SEH, “Radiation Hardened 30V 32-Channel Analog Multiplexer”
- Standard Microcircuit Drawing (SMD):
  - 5962-15219 - (ISL71840SEH)
  - 5962-15220 - (ISL72841SEH)
- Test Reports:
  - TR004, “ISL71840SEH Single Event Effects (SEE) Testing of the ISL71840SEH 16:1 30V Mux”

SEE Test Objectives

The ISL71841SEH was tested to determine its susceptibility to destructive single event effects (SEGR and SEB, collectively referred to by SEB herein) and to characterize its Single Event Transient (SET) behavior over various conditions and ion Linear Energy Transfer (LET) levels. The ISL71841SEH parts tested came from lot J67669.1, wafer #5 manufactured on Intersil's proprietary P6SOI process.

SEE Test Facility

Testing was performed at the Texas A&M University (TAMU) Cyclotron Institute heavy ion facility. This facility is coupled to a K500 super-conducting cyclotron, which is capable of generating a wide range of test particles with the various energy, flux and fluence levels needed for advanced radiation testing. Details on the test facility can be found on the TAMU Cyclotron website. Testing was carried out on March 20, 2015 and May 30, 2015.

SEE Test Setup

SEE testing is carried out with the sample in an active configuration. A schematic of the ISL71841SEH SEE test fixture is shown in Figure 1 on page 2. The test circuit is configured to accept variable supply voltages and two groupings of input voltages. The addressing of input IN22 is accomplished with VD1 low and VD2 high. With both VD1 and VD2 high the switches are all disabled. The output is set to half of VIN22-GND by a resistor divider formed from VIN22 to GND through VOUT. Of the remaining inputs, the odd numbered ones are connected to VINO and the even numbered ones are connected to VINE.

ISL71841SEH samples in standard ceramic flatpack packages without lids were assembled on boards that allowed two parts to be irradiated at one time. A 20-foot coaxial cable was used to connect the test fixture to a switch box in the control room which contained all of the monitoring equipment. The switch box allowed the two test circuits to be controlled and monitored remotely.

Digital multimeters were used to monitor pertinent voltages and currents. LeCroy waveRunner 4-Channel digital oscilloscopes were used to capture and store SET traces at VOUT that exceeded the oscilloscope’s ±20mV AC trigger setting.

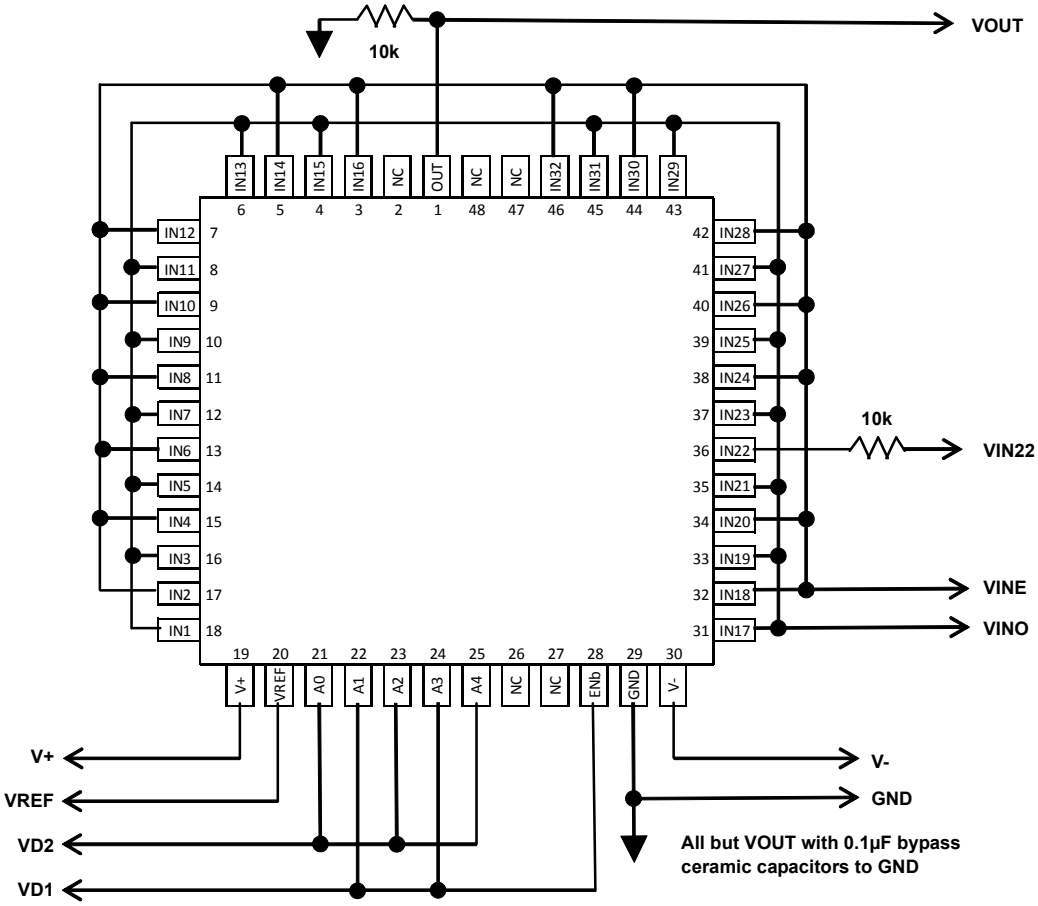

FIGURE 1. SCHEMATIC OF THE ISL71841SEHVF SEE TESTING CONFIGURATION

SEE Damage (SEB) Testing

For the destructive SEE (SEB) tests, conditions were selected to maximize the electrical and thermal stresses on the Device Under Test (DUT), thus insuring worst-case conditions. Two SEB tests were run with the conditions listed in Table 1. The supply voltages were set to the part's absolute maximum rating of ±20V. The input voltages were varied between ±17V, and ±35V to stress the switches at relevant conditions. Case temperature was maintained at +125°C ±10°C by controlling the current flowing into a resistive heater bonded to the underside of the board. Four DUTs were irradiated with 2.954GeV Au ions at normal incidence resulting in a surface LET = 86.4MeV•cm^2/mg. The normal range into silicon for these Au ions after 30mm of air is about 118µm with a Bragg peak range of 53µm. More details can be found on the TAMU Cyclotron website. These conditions guaranteed ions transited all active device volume in this SOI process (about 10µm depth). Each irradiation was to a fluence of $5x10^6$ions/cm^2. The currents into each of the voltage supplies was measured before and after each irradiation to look for changes indicative of permanent damage to the part.

As none of the supply currents reported in Table 2 changed by more than measurement repeatability it is inferred that they indicate no damage occurred due to the exposure to the ions. Based on this, it is concluded that the part is immune to destructive SEE effects under the conditions tested in Table 1.

TABLE 1. SEB CONDITIONS FOR TESTING THE ISL71841SEH. IRRADIATION WAS WITH 2.954 GeV Au AT 0° INCIDENCE FOR LET = 86.4MeV•cm^2/mg TO A FLUENCE OF $5x10^6$ions/cm^2.

	EFFECTIVE LET (MeV-cm^2/mg)	T_{CASE} (°C)	V± (V)	VINO (V)	VINE (V)	VIN22 (V)	VREF (V)	VD1 (V)	VD2 (V)
Test 1	86.4 at 0°	+125	±20	+17	-17	0	20	0	20
Test 2	86.4 at 0°	+125	±20	+35	-35	0	20	0	20

TABLE 2. SEB MONITOR PARAMETERS FOR TESTING AT LET 0° = 86.4MeV•cm^2/mg AND TCASE = +125°C. EACH IRRADIATION WAS TO A FLUENCE OF 5x106ions/cm^2.

MONITORED PARAMETER			I+ (µA)	I- (µA)	IINO (nA)	IINE (nA)	IREF (µA)	ID2 (nA)
DUT1	Test 1	Pre	336	336	17	21	170	12
		Post	320	320	18	21	171	12
	Test 2	Pre	281	281	67	72	171	12
		Post	281	281	63	74	171	12
DUT2	Test 1	Pre	310	310	10	20	168	14
		Post	310	310	11	22	168	14
	Test 2	Pre	280	280	64	59	169	14
		Post	280	280	64	64	169	14
DUT3	Test 1 (Note 1)	Pre	299	303	91	170	164	43
		Post	301	300	90	180	165	41
	Test 2	Pre	281	282	81	119	169	12
		Post	282	282	80	120	169	12
DUT4	Test 1 (Note 1)	Pre	303	302	75	51	165	61
		Post	303	303	88	48	165	65
	Test 2	Pre	290	290	18	141	171	11
		Post	291	291	18	122	172	11

NOTE:

1. Units tested in march 2015; other units tested in May 2015.

SET Testing of ISL71841SEH 32:1 Analog MUX

SET testing was done on four samples of the ISL71841SEH. Testing started with normal incidence gold (Au) at LET = 86.4MeV • cm^2/mg and with the SET detection threshold set to ±20mV deviation on V_{OUT}. Three separate conditions, as shown in Table 3, were applied to each of the four parts tested. Tests 1 and 2 looked for SET on V_{OUT} with IN22 selected, while Test 3 looked at V_{OUT} with all switches disabled. Addressing inputs were put at the respective VIL and VIH levels to test for addressing upsets.

The first test, Test 1, tests the part operating at the bottom of the recommended supply voltage range, ±10.8V. The second test exercises the part at the maximum of the supply voltage range, ±16.5V. In both cases the VREF is set to the minimum of the recommended operating range of 4.5V to minimize the noise margin in the addressing circuits. The lower noise margins makes the addressing most susceptible to a SEE leading to an address change SET.

Table 4 summarizes the SET counts for each test by DUT and then reports the nominal SET cross section for the complement of all four DUTs. The cross sections reported are the nominal found by dividing the event counts by the total fluence generating those counts.

Post processing of the captured SET oscilloscope traces generated the composite plots in Figures 2, 3, and 4 for the LET = 86.4MeV • cm^2/mg case. These plots show the composite of the 20 largest and 20 longest for each sense (positive and negative) of the extreme deviation so they reflect the worst 80 SET's observed in the run. Figures 2 and 3 show the SET with IN22 selected and connected to GND through both ends with 10kΩ resistors. Figure 4 shows the VOUT SET with all switches disabled.

In Figure 2 the vast bulk of the SET are less than 100mV, but for DUT2, 3, and 4 a handful of SET approaching 1V were recorded. In all cases the SET decayed away in about 15µs. These larger SET were not repeated under the conditions of Test 2 and Test 3 represented in Figures 3 and 4.

TABLE 3. THE ISL71841SEH SET TESTING CONDITIONS

	V± (V)	VREF (V)	VD1 (V)	VD2 (V)	VINO (V)	VINE (V)	VIN22 (V)
Test 1	±10.8	4.5	0.8	2.0	+10.8	-10.8	0
Test 2	±16.5	4.5	0.8	2.0	+16.5	-16.5	0
Test 3	±16.5	4.5	2.0	2.0	+16.5	-16.5	0

TABLE 4. ±20mV SET COUNTS ON V_{OUT} FOR TESTING OF THE ISL71841SEH. LET WAS 86.4MeV • cm^2/mg AND FLUENCE OF $4x10^6$ Ions/cm^2 PER RUN

TEST CONFIGURATIONS	DUT1 ±20mV EVENT COUNTS	DUT2 ±20mV EVENT COUNTS	DUT3 ±20mV EVENT COUNTS	DUT4 ±20mV EVENT COUNTS	TOTAL ±20mV SET CROSS SECTION (cm^2)
Test 1	1584	1564	1865	1712	4.2E-04
Test 2	1739	1606	1913	1738	4.4E-04
Test 3	1643	1801	1915	1681	4.4E-04

Composite Plots

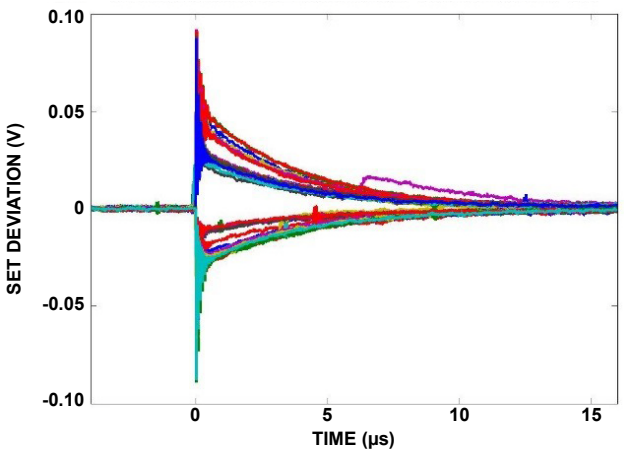

FIGURE 2A. DUT 1

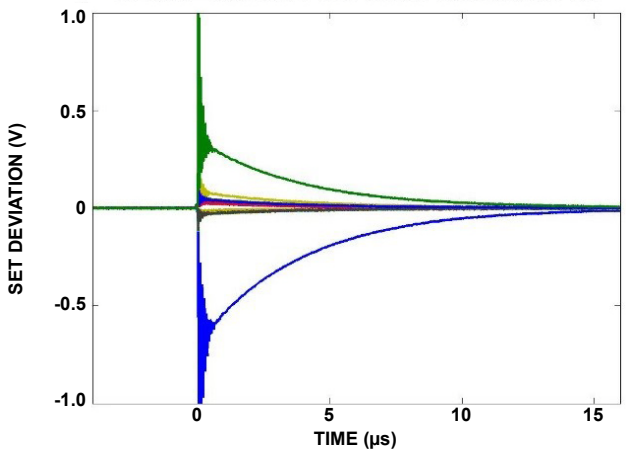

FIGURE 2B. DUT 2

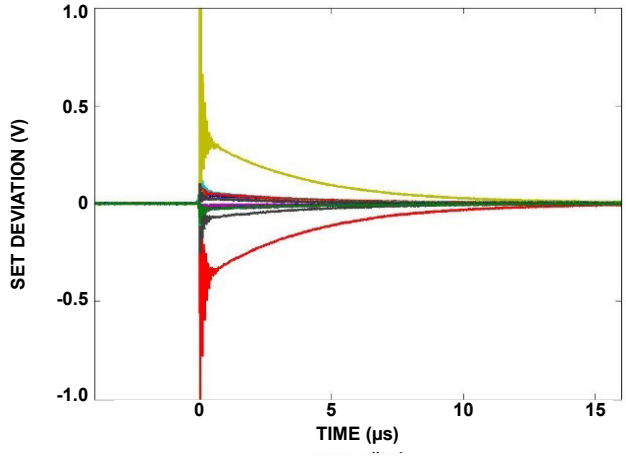

FIGURE 2C. DUT 3

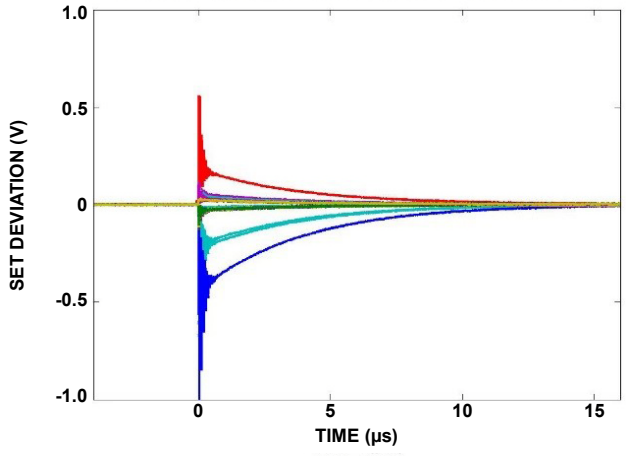

FIGURE 2D. DUT 4

FIGURE 2. Composite plots of extreme SET for LET = 86.4MeV • cm^2/mg for DUT 1 through 4 and Test 1, ±10.8V supplies and IN22 selected. Each run was to 4.0x10^6ions/cm^2. Post processing selected the 20 largest and longest SET with both positive and negative deviations; not all of 80 such plots were unique.

Composite Plots (Continued)

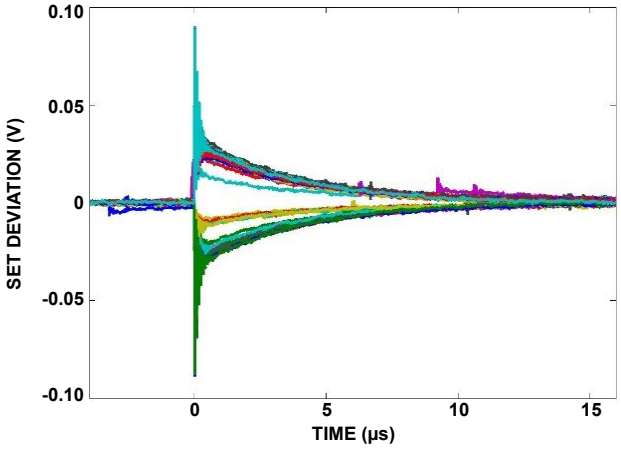

FIGURE 3A. DUT 1

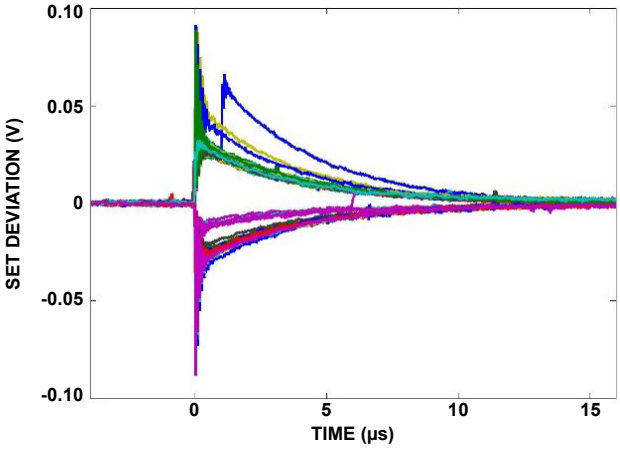

FIGURE 3B. DUT 2

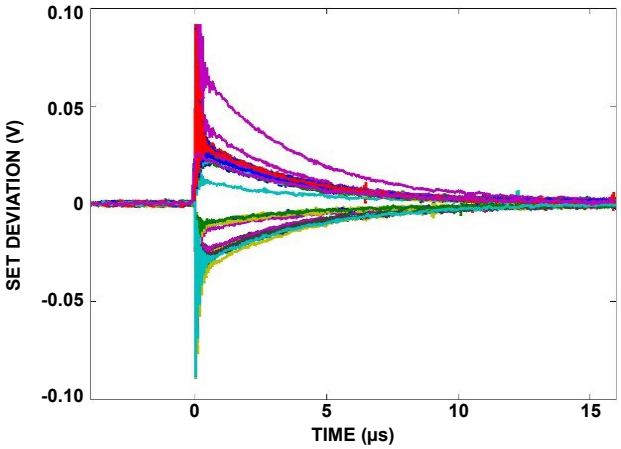

FIGURE 3C. DUT 3

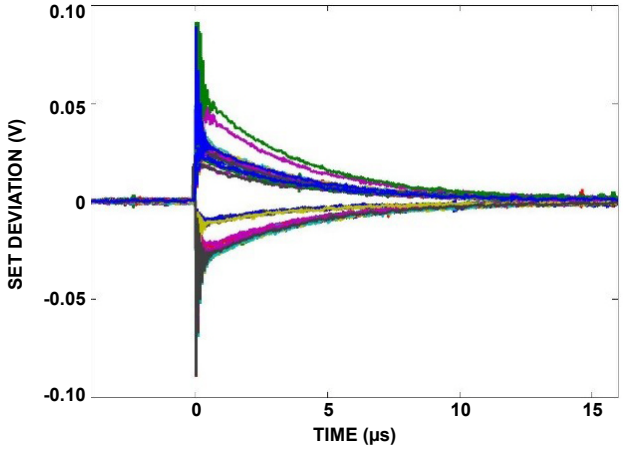

FIGURE 3D. DUT 4

FIGURE 3. Composite plot of SET for LET = 86.4MeV • cm^2/mg for DUT 1 through 4 and Test 2, ±16.5V supplies with IN22 selected. Each run was to 4.0x10^6ions/cm^2. Post processing selected the 20 largest and longest SET in both positive and negative deviations; not all of the 80 such plots were unique.

Composite Plots (Continued)

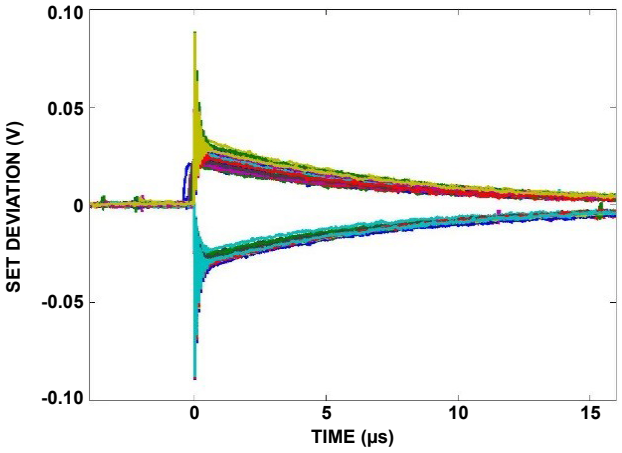

FIGURE 4A. DUT 1

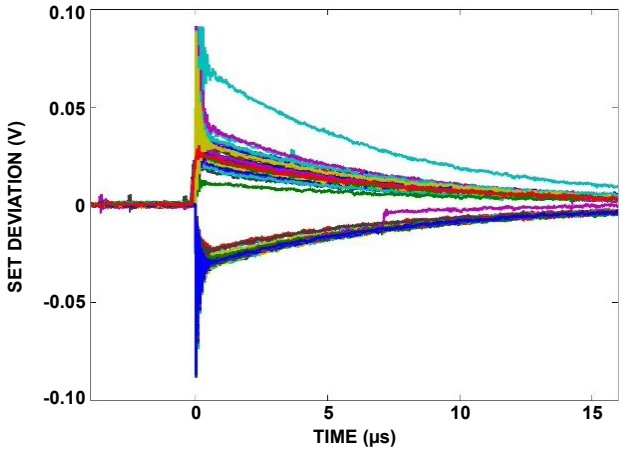

FIGURE 4B. DUT 2

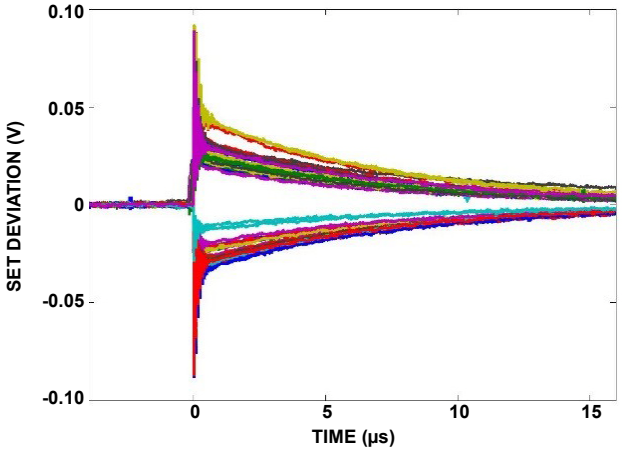

FIGURE 4C. DUT 3

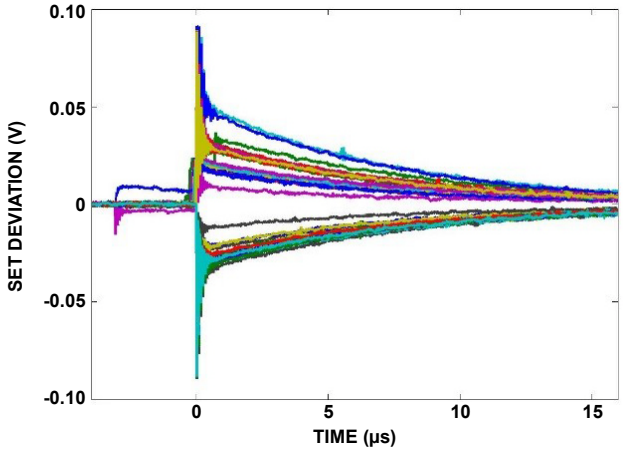

FIGURE 4D. DUT 4

FIGURE 4. Composite plot of SET for LET = 86.4MeV • cm^2/mg for DUT 1 through 4 and Test 3, ±16.5V supplies and switches disabled. Each run was to 4.0x10^6ions/cm^2. Post processing selected the 20 largest and longest SET in both positive and negative deviations; not all of the 80 such plots were unique.

Discussion and Conclusions

SEL and SEB

Testing with normal incidence Au at LET = 86.4MeV • cm^2/mg did not result in any indications of SEB or SEGR at applied voltages up to the absolute maximum rating of ±20V for supplies and ±35V for inputs. The 2.954GeV Au had a range into silicon of 117µm and a Bragg range of 53µm putting the Bragg peak well into the inactive handle wafer of the SOI part. Functionality and operational currents monitored did not change as a result of the irradiations carried out at a case temperature of +125°C ±10°C. A minimal interpretation of the possible SEB/SEGR cross section is less than $1.5x10^{-7}cm^2$ to a 95% confidence at LET = 86.4MeV • cm^2/mg at normal incidence for the input voltage conditions of ±17V and ±35V. In the total testing the SEB/SEGR possible cross section is less than $7.5x10^{-8}cm^2$ at 95% confidence. This is all tantamount to saying that under normal operating conditions the ISL71841SEH is not susceptible to SEB or SEGR failures at up to normal incidence of LET = 86.4MeV • cm^2/mg.

SET Results

In SET testing no indication of an addressing upset was noted. However, SET testing did result in events exceeding the ±20mV detection threshold. The total cross section indicated by the SET capture counts topped out at $4.4x10^{-4}cm^2$ at LET = 86.4MeV • cm^2/mg. The number of SET ±20mV captures was weakly dependent on supply voltage with ±10.8V yielding slightly fewer captured SET than with ±16.5V. It appears the SET result from instantaneous coupling of the output to the supply rails. With a few exception at ±10.8V supplies all the SET captured were within ±100mV deviation.

The observed output SET had decay times of about 15µs. This is likely set by the capacitive loading on V_{OUT} (about 700pF from the cabling) and the resistance setting the nominal voltage (5kΩ). Thus, the predicted 3.5µs time constant is consistent with that observed. This is important since the application will determine this decay constant and hence the SET duration.

The SET study described here utilized a nominal V_{OUT} of 0V so that the rails were equally far from the nominal output voltage. It should be expected that as the nominal V_{OUT} moves toward a supply rail the SET toward that rail voltage would diminish in magnitude while those toward the opposite rail would increase in magnitude. Thus, the worst case SET for a nominal output near a supply rail could be 2x the magnitudes recorded here.

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