ISL73007SEH

Single Event Effects (SEE) Testing of the ISL73007SEH Synchronous Buck Regulator

Introduction

The intense proton and heavy ion environment encountered in space applications can cause a variety of Single Event Effects (SEE) in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Latch-Up (SEL), and Destructive Single Event Effects (DSEE) which include both Single Event Gate Rupture (SEGR) and Single Event Burnout (SEB). SEE can lead to system-level performance issues including, disruption, degradation, and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. This report discusses the results of SEE testing performed on the ISL73007SEH product.

SEE Summary

- All irradiations were done with normal incidence gold for a surface linear energy transfer (LET) of 86MeV·cm^2/mg at an approximate flux of 5×10^{4}cm^{-2}s^{-1}. Each irradiation was to 1×10^{7}cm^{-2}.
- DSEE of PVIN and VCC was tested with a case temperature of 125°C ±10°C, an output of 3.3V, and a switched load of 0A and 3.3A (1Ω) at 100Hz and 50% duty cycle.
- No DSEEs were observed at PVIN = 16.5V. Four units were tested.
- No DSEEs or SELs were observed for V_{CC} = 5.8V (overdriven) and PVIN = 12V. Four units were tested.
- Two ±2% SETs were observed at V_{OUT} = 1.8V and 1.8A with a net cross-section of 1.25µm^2.
- Two ±3% SETs were observed at V_{OUT} = 3.3V and 3.3A with a net cross-section of 1.25µm^2.
- Spontaneously recovering SEFIs were observed with a net cross-section of 21µm^2.

Product Description

The ISL73007SEH is a Radiation Hardened Point-of-Load (POL) buck regulator providing up to 3A of output current capability with an input voltage ranging from 3V to 18V and from 3V to 16.5V in a heavy ion environment.

The ISL73007SEH uses constant frequency peak current mode control architecture for fast loop transient response. It can use either its internal compensation optimized for its internal default 500kHz switching frequency or an external Type II compensation at other switching frequencies to stabilize the loop as determined by specific design requirements and to optimize performance. The ISL73007SEH is specified over a switching frequency of 300kHz to 1MHz, adjusted using an external resistor.

The ISL73007SEH integrates both high-side (P-channel) and low-side (N-channel) power FETs with the options of internal compensation, switching frequency, and slope control; a minimum of external components are required for implementation, thereby reducing BOM count and complexity of the design.

The ISL73007SEH includes a comprehensive suite of operational features and protections, including preset undervoltage and overvoltage power-good, soft-start, overcurrent, and over-temperature.

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The ISL73007SEH is available in a 14-lead ceramic dual in line flat package (CDFP) and in loose die form.

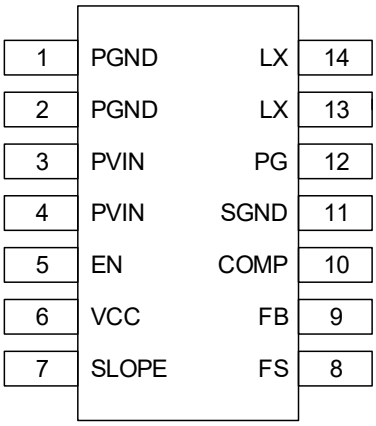

Figure 1. ISL73007SEH 14-Lead Ceramic Flatpack Pinout

Table 1. Pin Descriptions

Pin Number	Pin Name	Pin Description
1, 2	PGND	Power ground connection. Ground return for the low=side power MOSFET.
3, 4	PVIN	Power Input. Supplies the power switches of the buck converter.
5	EN	Enable input. This is a comparator-type input with a rising threshold of 1.5V. Bypass this pin to the PCB ground plane with a 10nF ceramic capacitor to mitigate SEE. The pin can be tied to PVIN and turns on at ~2.8V with a 10% hysteresis.
6	VCC	Linear regulator output from PVIN to provide an internal bias supply rail of up to 5V.
7	SLOPE	Slope Compensation. Connect a resistor from this pin to GND to externally set the slope compensation. This pin is a current source of 12µA into the external resistor. Connect the SLOPE pin to VCC to use the default internal slope compensation voltage of 1.2V If not connected to VCC, add a 1nF capacitor from this pin to ground for SEE and noise mitigation.
8	FS	Frequency select pin. Tie to VCC for 500kHz operation. Connect a resistor to ground to program the frequency from 300kHz to 1MHz.
9	FB	EA inverting input. Connect a resistor divider from VOUT to GND with the midpoint driving the FB pin.
10	COMP	EA output. The external compensation network will be connected from this pin to GND. Tie this pin to VCC to use the internal compensation setup.
11	SGND	Signal ground. The ground is associated with the internal control circuitry. Connect this pin directly to the PCB ground plane.
12	PG	Power good output. The pin is an open-drain logic output that is pulled to SGND when the output is outside of the PGOOD range. The pin can be pulled to any voltage up to the PVIN abs maximum limit. A nominal 1kΩ to 10kΩ pull-up resistor is recommended. Bypass this pin to the PCB ground plane with a 100pF capacitor for SEE mitigation.
13, 14	LX	Switch node connection. Connect this pin to the output filter inductor. Internally this pin is connected to the synchronous MOSFET power switches.

Contents

1. SEE Testing

1.1 Test Objective

The testing was intended to find the limits of the supply voltages and load currents set by the onset of DSEE at a linear energy transfer (LET) of 86MeV·cm^2/mg (normal incidence gold). Additional testing was intended to identify and quantify single-event transients (SET) and single-event functional interrupts (SEFI) occurring on the output voltage. The SET/SEFI studies were also done with normal incidence gold (86MeV·cm^2/mg).

1.2 Test Facility

Single-event effects testing was done at the Texas A&M University (TAMU) Radiation Effects Facility of the Cyclotron Institute in College Station, Texas. This facility is coupled to a K500 superconducting cyclotron which can supply a wide range of ion species and flux. The testing referred to in this report was done in August 2022.

2. Results

2.1 PVIN DSEE

DSEE testing based on the value of PVIN was done by setting the output at 3.3V, using the internally set frequency of 500kHz, and gradually walking the PVIN voltage from 15.5V to 17.0V in 0.5V steps. The output was loaded at 0A and 3.3A (1Ω) with a switching frequency of 100Hz and 50% duty cycle. The output LC filter comprised a 4.7µH inductor and a 150µF bulk capacitor (ESR < 30mΩ). The internal SLOPE and COMP were invoked by connecting those pins to VCC. Each irradiation with normal incidence gold for a surface LET of 86MeV·cm^2/mg was to 1×10^{7}ion/cm^2 at a flux of approximately 5×10^{4}ion/cm^2/s. The part was heated to a case temperature of 125°C ±10°C. Before and after each irradiation, the following four parameters were measured to look for evidence of DSEE:

- Output voltage at zero load
- PVIN current at zero load
- PVIN current at standby (EN = 1V)
- Leakage current on LX with EN = 1V and LX = 8V

Changes in these parameters were considered to indicate DSEE at changes of more than ±2%, ±25%, ±25%, and ±5%, respectively.

The results from the PVIN DSEE testing are summarized in Table 2. All four parts tested passed to 16.5V PVIN. The previous testing logged PVIN failures at 17.0V.

Table 2. Log of Results from PVIN DSEE Testing Results[1]

DUT	PVIN	VOUT (V) ±2%		I_PVIN (mA) ±25%		I_PVIN STBY (mA) ±25%		I_LX (µA) ±5% V_LX = 8V	
	(V)	Pre	Post	Pre	Post	Pre	Post	Pre	Post
DUT1	15.5	3.285	3.285	42.5	42.3	1.8	1.7	682	683
	16.0	3.287	3.284	42.4	42.7	1.7	1.8	683	683
	16.5	3.284	3.280	43.1	44.4	1.8	1.9	683	683
DUT2	15.5	3.291	3.291	37.2	37.5	1.6	1.6	684	684
	16.0	3.292	3.295	37.8	38.1	1.6	1.6	684	685
	16.5	3.294	3.293	38.3	38.1	1.7	1.7	685	683

Table 2. Log of Results from PVIN DSEE Testing Results[1] (Cont.)

DUT	PVIN	VOUT (V) ±2%		I_PVIN (mA) ±25%		I_PVIN STBY (mA) ±25%		I_LX (µA) ±5% V_LX = 8V	
	(V)	Pre	Post	Pre	Post	Pre	Post	Pre	Post
DUT3	15.5	3.291	3.295	42.2	43.4	2.8	2.9	669	670
	16.0	3.295	3.299	44.1	45.1	3.0	3.0	670	670
	16.5	3.299	3.307	45.2	46.3	3.1	3.2	670	669
DUT4	15.5	3.302	3.300	44.9	45.6	3.3	3.5	671	671
	16.0	3.301	3.306	47.1	48.2	3.9	4.0	671	671
	16.5	3.307	3.299	47.7	49.0	4.1	4.4	671	670

1. Each PVIN voltage saw the DUT receive 1×10^7ion/cm^2 of normal incidence gold for a surface LET of 86MeV·cm^2/mg at a die temperature of 125°C ±10°C.

2.2 V_{CC} DSEE

The VCC supply was overdriven for the V_{CC} DSEE testing, so the internal regulator from PVIN was inactive, and the V_{CC} current could be monitored directly. The V_{CC} voltage was varied from 5.6V to 6.2V in 0.2V steps. Other than PVIN being 12V, the situation was as for the PVIN DSEE testing. The V_{CC} current was also monitored during irradiation to detect any indications of SEL through increases in the current.

The details of the V_{CC} DSEE testing appear in Table 3. All four units tested passed at 5.8V. One unit saw abrupt I_{VCC} increases at the 6.0V irradiation, while the other three saw I_{VCC} increases at 6.2V.

Table 3. Log of V_{CC} DSEE Testing Results[1]

DUT	V_{CC}	V_{OUT} (V) ±2%		I_VCC (mA) ±25%		I_PVIN (mA) ±25%	
	(V)	Pre	Post	Pre	Post	Pre	Post
DUT5	5.6	3.301	3.304	9.96	10.01	30.0	30.3
	5.8	3.305	3.309	10.86	10.81	32.5	33.1
	6.0	3.310	3.306	11.67	11.60	35.2	35.4
	6.2	3.308	3.312	12.53	23.25	38.1	37.6
DUT6	5.6	3.301	3.296	9.85	9.85	28.0	28.0
	5.8	3.298	3.291	10.68	10.79	30.2	31.8
	6.0	3.293	3.290	11.57	11.56	33.1	33.3
	6.2	3.293	3.292	12.51	24.55	38.2	36.5
DUT7	5.6	3.270	3.261	9.89	9.79	28.3	29.6
	5.8	3.262	3.262	10.63	10.67	31.8	32.6
	6.0	3.264	3.265	11.53	11.50	34.8	35.6
	6.2	3.267	3.263	12.44	18.87	38.2	38.1
DUT8	5.6	3.302	3.301	9.63	9.61	25.9	26.9
	5.8	3.301	3.300	10.43	10.47	28.6	29.2
	6.0	3.302	3.307	11.31	31.92	31.2	31.8

1. Each V_{CC} voltage saw the DUT receive 1×10^7ion/cm^2 of normal incidence gold for a surface LET of 86MeV·cm^2/mg at a die temperature of 125°C ±10°C. Failures are indicated with shaded cells.

2.3 Single Event Functional Interrupt (SEFI)

Operation of the ISL73007SEH during both PVIN DSEE testing and SET testing was monitored for SEFI by triggering an oscilloscope on PGOOD transitions through 1V. The captures were over 19ms to accommodate normal hiccup recovery from fault events. The signals captured were PGOOD, VOUT, LX (the switching node), and VLOAD.

The summary of the SEFI captures during PVIN DSEE testing appear in Table 4. A total of 25 SEFIs were captured in a total fluence of $1.2\times10^{8}cm^{-2}$. This amounts to a net cross-section of $21\mu m^{2}$.

Table 4. SEFI counts for PVIN DSEE at $1\times10^{7}cm^{-2}$ and 125°C±10°C

PVIN	DUT 1	DUT 2	DUT 3	DUT 4
15.5	0	0	0	5
16.0	1	0	1	9
16.5	5	0	0	4

An example of SEFI captured during PVIN DSEE testing appears in Figure 2. The PGOOD trace (black) shows the duration of the SEFI at approximately 13.5ms when running at 500kHz. V_{OUT} (red) falls after the start of the SEFI as dictated by the current load on V_{OUT}. At about 8ms, V_{OUT} begins to rise with a soft-start and attains its final voltage at about 13.5ms. LX (blue), the switching node, stops switching at the start of the SEFI and only resumes switching at the start of the soft-start. V_{LOAD} (green) is an indication of the loading on V_{OUT}. When V_{LOAD} is high, the load current is 3.3A, and when V_{LOAD} is low, the load current is 0A. The 21 SEFI captured all looked as Figure 2.

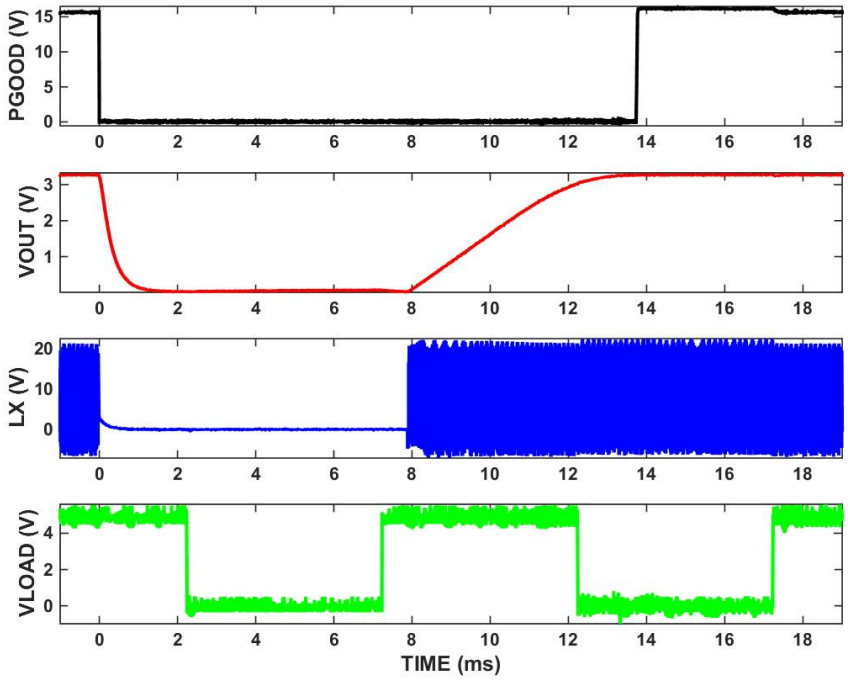

Figure 2. Example SEFI from PVIN DSEE Testing at 500kHz

The details of the SEFI captures during SET testing are covered in the section on SET testing. Table 6 provides the summary of SEFI captures in the SET testing. Only six SEFIs were captured in a $1.6\times10^{8}cm^{-2}$ fluence for a net cross-section of $3.1\mu m^{2}$. Four of these six SEFIs were captured for a part running at 1MHz switching frequency, resulting a SEFI of about 6.5ms, as shown in Figure 3.

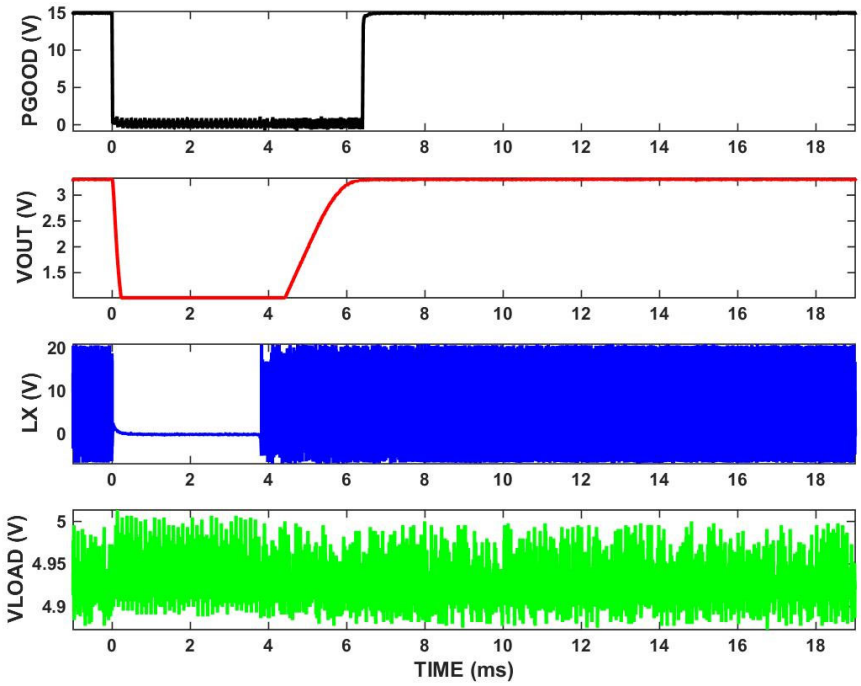

Figure 3. SEFI Captured at 1MHz in the SET Testing

2.4 Single Event Transient (SET)

Sixteen configurations were tested for single event transient (SET) and single event functional interrupt (SEFI), described in Table 5. Two parts were tested in each configuration to a fluence of $1\times10^{7}cm^{-2}$ each. In all cases, a load resistor of 1Ω was used, resulting in an output current of either 1.8A or 3.3A, depending on the output voltage. SETs were captured whenever the VOUT deviated from nominal by ±2% for the 1.8V output and ±3% for the 3.3V output. SEFIs were counted by PGOOD transitioning through 1V. All SEFI were hiccup events where the output came back up through a normal startup process (including soft-start) after a hiccup delay.

Table 5. Configurations used for SET and SEFI Testing

Configuration	COMP	SLOPE	FS	L_{OUT}	C_{OUT}	V_{OUT} (V)	PVIN (V)
1	VCC	VCC	VCC (500kHz)	1.8µH	150µF	1.8	3
2							6
3					2×150µF		3
4							6
5	14.7kΩ 1.8nF	61.9kΩ	100kΩ (500kHz)		150µF		3
6							6
7		75kΩ	30.1kΩ (1.0MHz)	0.68µH			3
8							6

Table 5. Configurations used for SET and SEFI Testing (Cont.)

Configuration	COMP	SLOPE	FS	L_{OUT}	C_{OUT}	V_{OUT} (V)	PVIN (V)
9	VCC	VCC	VCC (500kHz)	4.7µH	100µF	3.3	10
10							15
11					2×100µF		10
12							15
13	14.7kΩ 2.2nF	43.7kΩ	100kΩ (500kHz)		100µF		10
14							15
15	14.7kΩ 1.2nF	42.2kΩ	30.1kΩ (1.0MHz)	2.2µH	56µF		10
16							15

Only gold (surface LET of 86MeV·cm^2/mg) was tested for SET due to the very low number of events captured with gold. The time scale for the SET captures was set to be from -40µs from trigger to 160µs after trigger. For the SEFI captures the time scale was set from -1ms to +19ms relative to the trigger point. The SET and SEFI counts captured for each configuration appear in Table 6.

The SET captured were relatively uninteresting and are represented in Figure 4 and Figure 5. The V_{OUT} traces do not exhibit a well localized SET, and the LX (switch node) do not show any anomalies. This combined with the total of only four SET captured indicates very benign SET jeopardy.

Table 6. SET and SEFI Capture Counts for 1×10^{7}cm^{-2} Fluence at 25°C

Configuration	SET Criteria	SET Count		SEFI Count	
		DUT 1	DUT 2	DUT 1	DUT 2
1	±2%	0	0	0	0
2		2	0	0	0
3		0	0	0	0
4		0	0	2	0
5		0	0	0	0
6		0	0	0	0
7		0	0	0	0
8		0	0	0	0
9	±3%	0	0	0	0
10		0	0	0	0
11		0	0	0	0
12		0	0	0	0
13		0	0	0	0
14		2	0	0	0
15		0	0	0	0
16		0	0	0	4

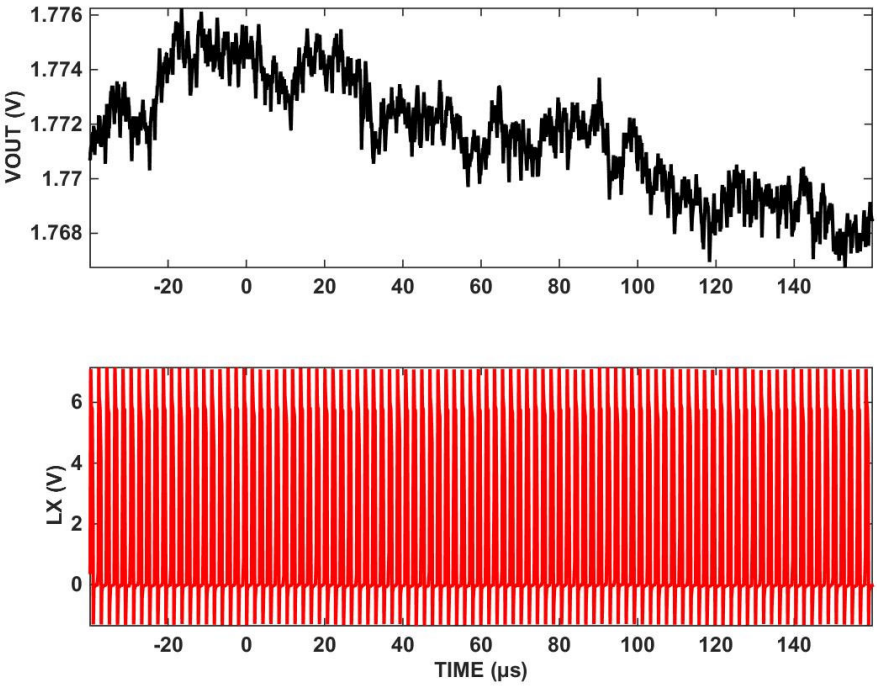

Figure 4. SET at V_{OUT} = 1.8V SET Testing

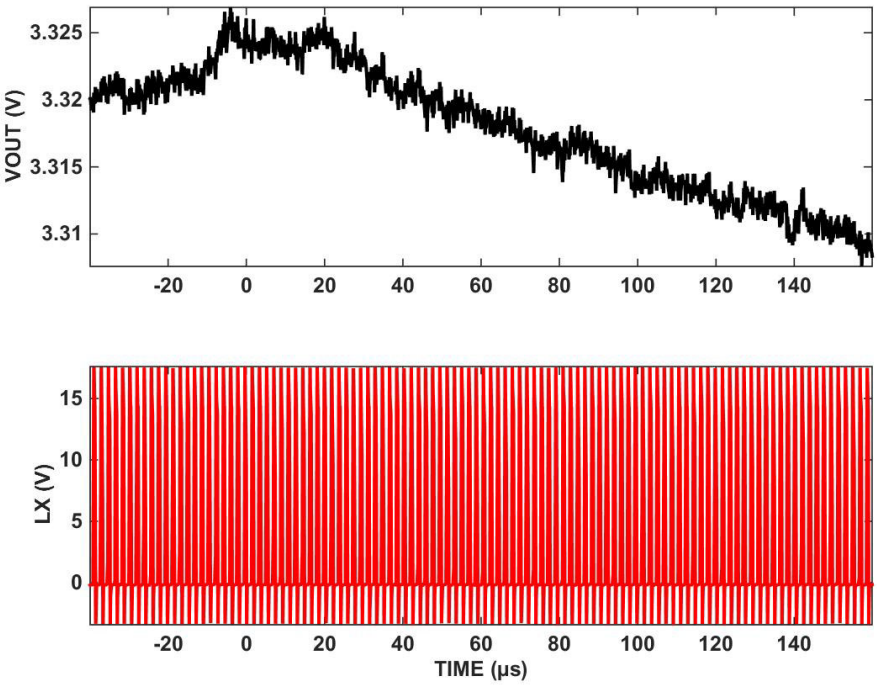

Figure 5. SET at V_{OUT} = 3.3V SET Testing

3. Discussion and Conclusions

The ISL73007SEH proved to be free of DSEE at supply voltage (PVIN) up to 16.5V and a case temperature of 125°C ±10°C when irradiated with normal incidence gold for a surface linear energy transfer (LET) of 86MeV·cm^2/mg. At 16.5V, the total fluence tested was 4×10^{7}cm^{-2} over four parts. The 3.3V output was switched between loads of 0A and 3.3A (1Ω) at 100Hz with a 50% duty cycle. The output inductor was 4.7µH, the bulk output capacitance was 150µF, and the switching frequency was the internally provided 500kHz.

A second DSEE test was run with a VCC voltage overdriving the internal regulator (4.85V to 5.10V). The external current into VCC was also monitored. Neither DSEE nor SEL was observed with VCC up to 5.8V at a case temperature of 125°C±10°C when irradiated with normal incidence gold for a surface LET of 86MeV·cm^2/mg. At 5.8V, the total fluence tested was 4×10^{7}cm^{-2} over four parts. The input PVIN was set to 12V, and the 3.3V output was loaded as for the PVIN DSEE. Again, the frequency was 500kHz, and the output LC was as for the PVIN DSEE.

SEFI comprised of a VOUT shutdown and spontaneous soft-start recovery was observed in both the PVIN DSEE testing and the SET testing. All the SEFI observed were for normal incidence gold for a surface LET of 86MeV·cm^2/mg. For the PVIN DSEE testing, 25 SEFI were recorded in a total fluence of 1.2×10^{8}cm^{-2} for a net cross-section of 21.0µm^2. These SEFI were 13.5ms long (at 500kHz). Six SEFI were captured during the SET testing with a total fluence of 3.2×10^{8}cm^{-2} for a cross-section of 1.9µm^2. Four of these SEFI were of length 6.5ms at a switching frequency of 1.0MHz. Combining all SEFI data (PVIN DSEE and SET) yields a net SEFI cross-section of 7µm^2.

The buck regulator was tested for SET defined by output voltage deviations of ±2% (±36mV) at 1.8V output or ±3% (±99mV) at 3.3V output (the latter was set to accommodate the switching noise that led to constant triggering at ±2%). All SET testing was with normal incidence gold for a surface LET of 86MeV·cm^2/mg. The 1.8V output was used for PVIN of 3V and 6V, while the 3.3V output was used for PVIN of 10V and 15V. Two 2% SETs were recorded in a total fluence of 1.6×10^{8}cm^{-2} with V_{OUT} at 1.8V for a cross-section of 1.25µm^2. Two 3% SETs were recorded in a total fluence of 1.6 ×10^{8}cm^{-2} with V_{OUT} at 3.3V for a cross-section of 1.25µm^2.

4. Revision History

Revision	Date	Description
1.01	Sep 11, 2024	Added the Appendix section.
1.00	Mar 29, 2023	Initial release.

A. Appendix: SET Testing at LET = 45.8MeV·cm^2/mg

A.1 Results

Additional SET testing was conducted at the Texas A&M University Cyclotron Institute on April 12, 2024, at an LET of 45.8MeV·cm^2/mg to estimate the threshold LET for SEFIs. The DUTs were irradiated with normal incidence silver ions at an ambient temperature of 25°C to a fluence of 1E7ions/cm^2. The ISL73007SEH was tested in the configurations displayed in Table 7.

Table 7. Configurations used for SET and SEFI Testing at LET = 45.8MeV·cm^2/mg

Configuration	COMP	SLOPE	FS	L_{OUT} (µH)	C_{OUT} (µF)	V_{OUT} (V)	PVIN (V)
1	Tied to VCC	Tied to VCC	Tied to VCC	1.8	150	1.8	3
2	Tied to VCC	Tied to VCC	Tied to VCC	1.8	150	1.8	6

Oscilloscopes were set to capture events in which V_{OUT} deviated by ±36mV, which represents a ±2% deviation of the nominal output voltage, or in which PG pulled below 1V to capture SETs and SEFIs, respectively. The results of the testing are displayed in Table 8

Table 8. SET and SEFI results at LET = 45.8MeV·cm^2/mg

Configuration #	DUT #	SET Count (#)	Total SET Count (#)	SEFI Count (#)	Total SEFI Count (#)
1	1	0	0	0	0
	2	0		0	
	3	0		0	
	4	0		0	
2	1	603	1482	0	0
	2	51		0	
	3	828		0	
	4	0		0	

No SEFIs were captured during any of the runs. There were no SET captures in configuration 1. In configuration 2, there were triggers on V_{OUT} deviations; however, V_{OUT} never deviated beyond ±2% of the operating voltage as shown in Figure 6. The red lines in the figure indicate the ±2% window.

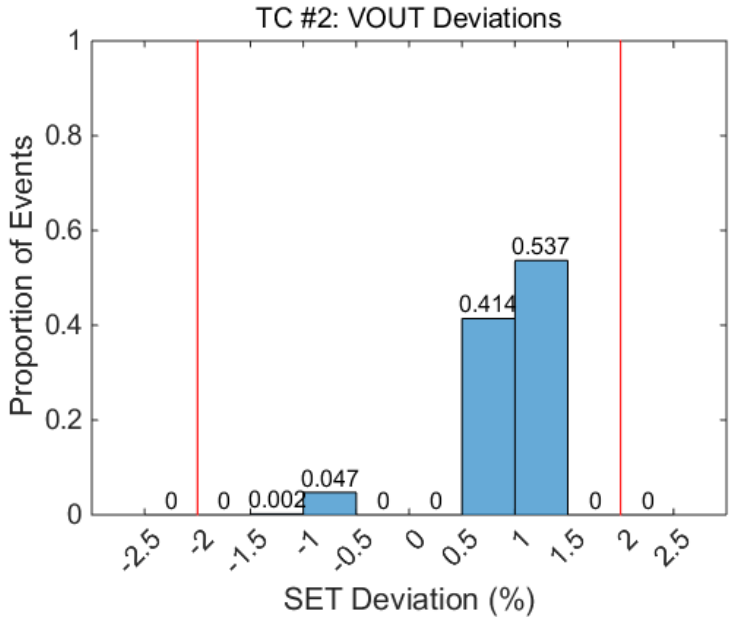

Figure 6. Test Condition #2 VOUT Deviation Size at LET = 45.8MeV·cm^2/mg

Similarly to the SET captures at LET = 86MeV·cm^2/mg, the V_{OUT} traces at LET = 45.8MeV·cm^2/mg do not exhibit a well localized SET, and the LX do not show any anomalies. An example capture is shown in Figure 7. As VOUT and LX do not exhibit well localized SETs, the susceptibility of the ISL73007SEH to disruptive SETs is minimal.

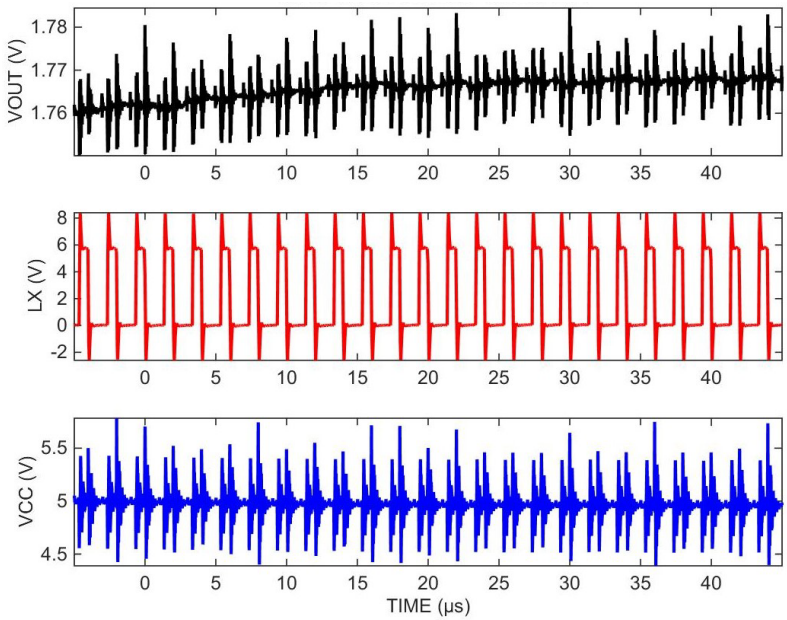

Figure 7. Example SET capture at LET = 45.8MeV·cm^2/mg

A.2 Conclusion

At an LET of 45.8MeV·cm^2/mg, ISL73007SEH did not exhibit any SEFIs. Therefore, an LET of 45.8MeV·cm^2/mg can be used as the threshold LET for SEFI events. By modeling the cross-section versus LET curve as a step function with a threshold of 45.8MeV·cm^2/mg and a saturation cross-section of 90µm^2, the worst-case SEFI cross-section measured at LET = 86MeV·cm^2/mg, the error rate for SEFIs in a geosynchronous orbit behind 100mils of aluminum shielding during solar minimum is calculated using CREME96 as 1.6E-5 SEFIs/year. This corresponds to a mean time between SEFIs of approximately 61,018 years.

The ISL73007SEH exhibited SETs at an LET of 45.8MeV·cm^2/mg; however, during the events, V_{OUT} never exceeded the ±2% window, and LX do not show any anomalies. Therefore, there is low risk of the part exhibiting any disruptive SETs.

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