ISL73007SEH

Low Dose Rate Test Results of the ISL73007SEH Radiation Hardened 18V, 3A Point-of-Load Regulator

Introduction

This report documents the results of low dose rate (LDR) total dose testing of the ISL73007SEH, a radiation hardened 18V, 3A, Point-of-Load (POL) buck regulator. The testing assesses the total dose hardness of the parts and determines any bias sensitivity. Parts were irradiated under bias and with all pins grounded - at LDR to 100krad(Si) with an anneal on the biased parts. The ISL73007SEH is rated at 75krad(Si) at LDR (0.01rad(Si)/s) and is acceptance tested on a wafer-by-wafer basis to the datasheet limits.

Product Description

The ISL73007SEH is a radiation hardened Point-of-Load (POL) buck regulator that provides up to 3A of output current capability with an input voltage ranging from 3V to 18V and from 3V to 16V in a heavy ion environment. The device uses constant frequency peak current mode control architecture for fast loop transient response. The device uses internal compensation suitable for the entire switching frequency range or an external Type II compensation to optimize performance and stabilize the loop. The ISL73007SEH is specified over a switching frequency of 300kHz to 1MHz using an external resistor.

The ISL73007SEH integrates high-side (P-channel) and low-side (N-channel) power FETs. There are options for internal compensation, switching frequency, and slope control, that you can implement with a minimum of external components reducing the BOM count and design complexity.

The ISL73007SEH includes a comprehensive suite of operational features and protections, including preset undervoltage, overvoltage, overcurrent protections, power-good, soft-start, and over-temperature. The ISL73007SEH is available in a 14-lead ceramic dual in-line flat package (CDFP) and loose die form. Figure 1 shows the package and pin assignments for the ISL73007SEH, and Table 1 shows the pin descriptions.

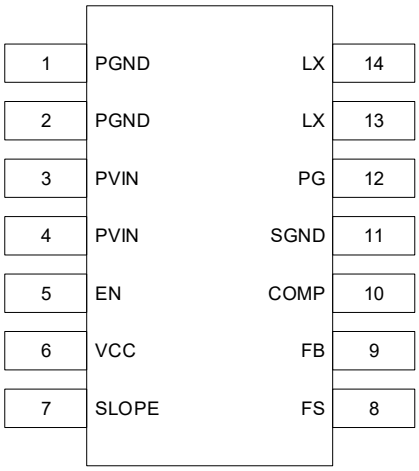


Figure 1. Pin Assignments - Top View

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
1, 2	PGND	Power ground connection. Ground return for the low-side power MOSFET.
3, 4	PVIN	Power Input. Supplies the power switches of the buck converter.

Table 1. Pin Descriptions (Cont.)

Pin Number	Pin Name	Description
5	EN	Enable input. This input is a comparator-type input with a rising threshold of 1.2V. Bypass this pin to the PCB ground plane with a 10nF ceramic capacitor to mitigate SEE. You can tie this pin to a maximum of 5V.
6	VCC	Linear regulator output from PVIN to provide an internal bias supply rail of up to 5V. Bypass this pin to the PCB ground plane with a 2.2µF ceramic capacitor for stability, SEE, and noise mitigation.
7	SLOPE	Slope Compensation. Connect a resistor from this pin to GND to externally set the slope compensation. This pin is a current source of 12µA into the external resistor. Connect the SLOPE pin to VCC to use the default internal slope compensation voltage of 1.2V. If not connected to VCC, add a 1nF capacitor from this pin to ground for SEE mitigation.
8	FS	Frequency select pin. Tie to VCC for 500kHz operation. Connect a resistor to ground to program the frequency from 300kHz to 1MHz. Reference Equation 1 of the datasheet for the frequency setting formula.
9	FB	Error Amplifier inverting input. Connect a resistor divider from VOUT to GND with the midpoint driving the FB pin.
10	COMP	Error Amplifier output. The external compensation network is connected from this pin to GND. Tie this pin to VCC to use the internal Error Amplifier compensation setup.
11	SGND	Signal ground. The ground is associated with the internal control circuitry. Connect this pin directly to the PCB ground plane at a single point. Pin 11 is connected to the thermal flash on the package bottom and lid seal ring.
12	PG	Power-good output. The pin is an open-drain logic output pulled to SGND when the output is outside of the PGOOD range. The pin can be pulled to any voltage up to the PVIN abs maximum limit. Renesas recommends using a nominal 1kΩ to 10kΩ pull-up resistor. Bypass this pin to the PCB ground plane with a 100pF capacitor for SEE mitigation.
13, 14	LX	Switch node connection. Connect this pin to the output filter inductor. Internally, this pin is connected to the common node of the synchronous MOSFET power switches.

Contents

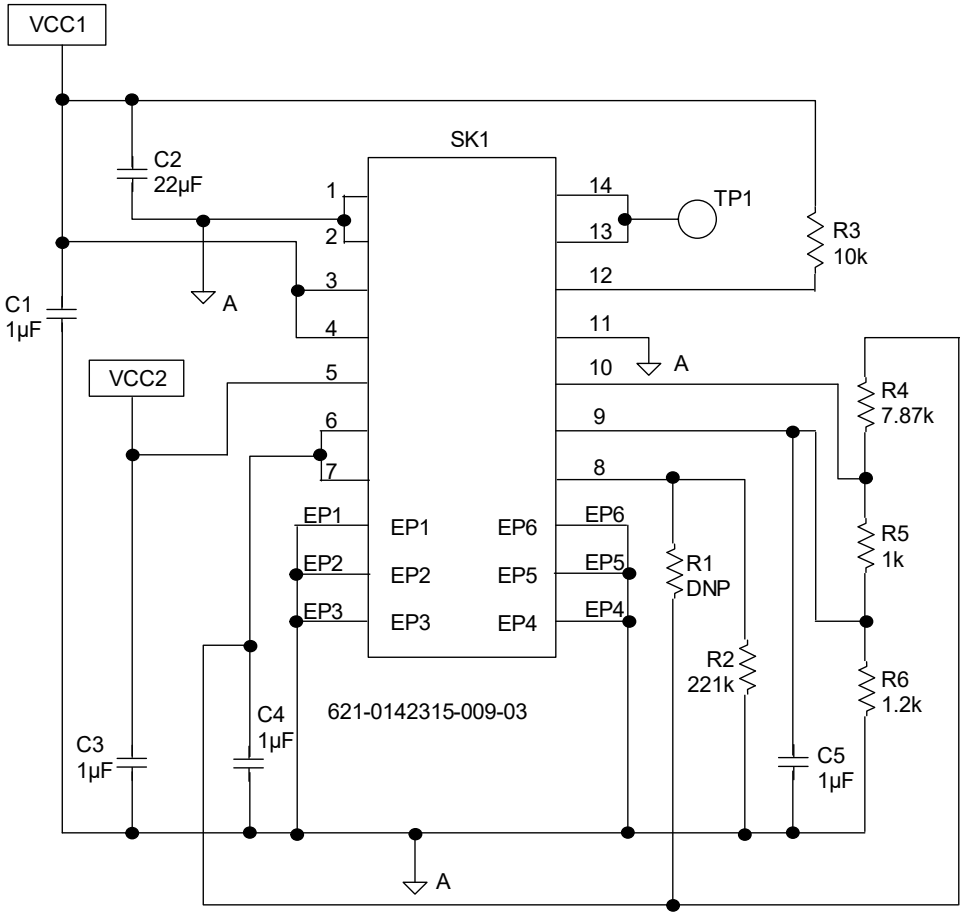
1. Test Description

1.1 Irradiation Facilities

LDR testing was performed at 0.01rad(Si)/s using the Renesas Palm Bay N40 panoramic irradiator. PbAl spectrum hardening filters were used to shield the test board and devices under test against low-energy secondary gamma radiation. Eighteen samples were biased, and six had all pins grounded during irradiation. The anneal operation was only performed on the biased units in a small temperature chamber.

1.2 Test Fixturing

The biased ISL73007SEH samples were irradiated using the configuration and voltages shown in Figure 2.



Voltages and Sequencing:

1. VCC1 = V1 = 17.0V
2. VCC2 = V2 = 5.0V

Reverse the order for power-down:

1. VCC2 = V2 = 0.0V
2. VCC1 = V1 = 0.0V

Figure 2. ISL73007SEH TID Bias Schematic and Voltages

1.3 Characterization Equipment and Procedures

All electrical testing was performed at room temperature outside the irradiator, using production automated test equipment (ATE) with data-logging at each down-point.

1.4 Experimental Matrix

Irradiation was performed following the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 18 samples irradiated at LDR under bias and six irradiated at LDR with all pins grounded. The biased parts were also subjected to a 168-hour, 125°C biased anneal. Two control units were used. The ISL73007SEH samples were from wafer lot SPX5X.

1.5 Down-points

Down-points for the LDR tests were 0, 10, 30, 50, 75, 100krad(Si), and Post-Anneal (PA).

2. Test Results

2.1 Attributes Data

LDR testing of the ISL73007SEH is complete. All tested parameters passed the datasheet limits. Table 2 summarizes the results.

Table 2. ISL73007SEH Total Dose Test Attributes Data

Dose rate (rad(Si)/s)	Bias	Sample Size	Downpoint	Pass[1]	Fail
0.01	Biased (Figure 2)	18	Pre-irradiation	18	0
			10krad(Si)	18	0
			30krad(Si)	18	0
			50krad(Si)	18	0
			75krad(Si)	18	0
			100krad(Si)	18	0
			Post-Anneal	18	0
0.01	Grounded	6	Pre-irradiation	6	0
			10krad(Si)	6	0
			30krad(Si)	6	0
			50krad(Si)	6	0
			75krad(Si)	6	0
			100krad(Si)	6	0

1. Pass indicates a sample that passes all datasheet limits.

2.2 Key Parameter Variables Data

The plots in Figure 3 through Figure 43 illustrate the LDR response of the selected parameters shown in Table 3 in the Appendix. The plots show the average tested values of the parameters as a function of the total dose for each of the irradiation conditions, biased and grounded, plus a 168-hour 125°C anneal for the biased units. That downpoint is shown as PA (Post-Anneal) on the graphs. The plots also include error bars at each downpoint, representing the sample minimum and maximum measured values. However, in some plots, the error bars might not be visible due to their values compared to the scale of the graph.

The irradiated parts passed all parameters up to the final TID characterization exposure level of 100krad(Si), and the parts that were put on a 168-hour biased anneal also passed that.

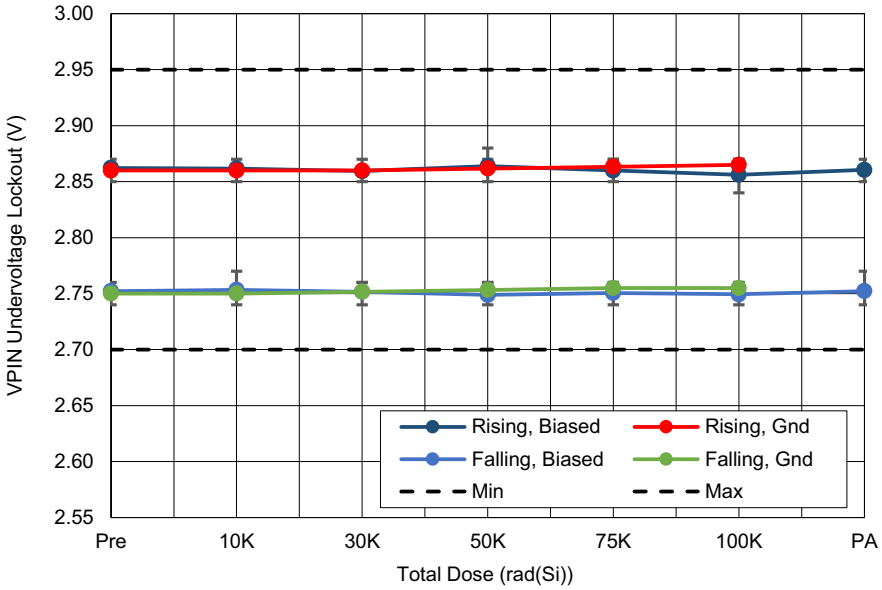


Figure 3. ISL73007SEH rising and falling undervoltage lockout (V_{PVIN_UVLO}), with EN = 2.25V, as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 2.7V minimum (falling) and 2.95V maximum (rising).

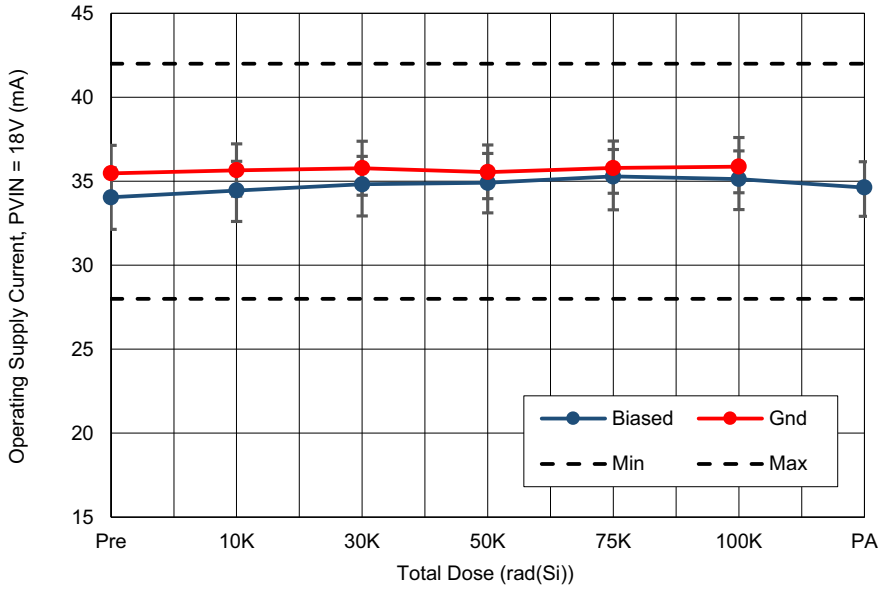


Figure 4. ISL73007SEH operating supply current (I_{PVIN_OPER}) at 500kHz, with PVIN = 18V, EN = 5V and no load, as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 28mA minimum and 42mA maximum.

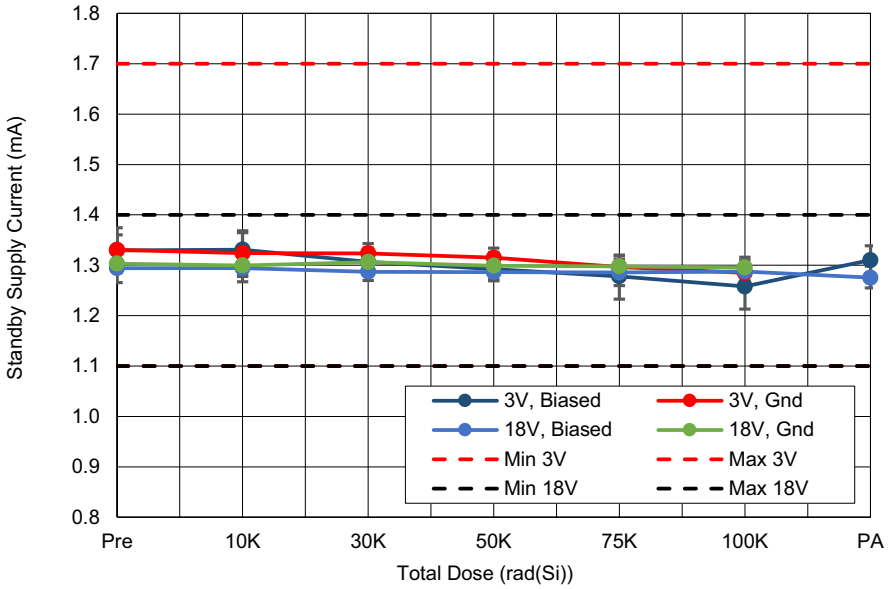


Figure 5. ISL73007SEH standby supply current (I_{PVIN_SB}) with PVIN = 3V and 18V, EN = 1V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 1.1mA minimum and 1.7mA maximum for PVIN = 3V (upper limit shown in red), and 1.1mA minimum and 1.4mA maximum for PVIN = 18V (shown in black).

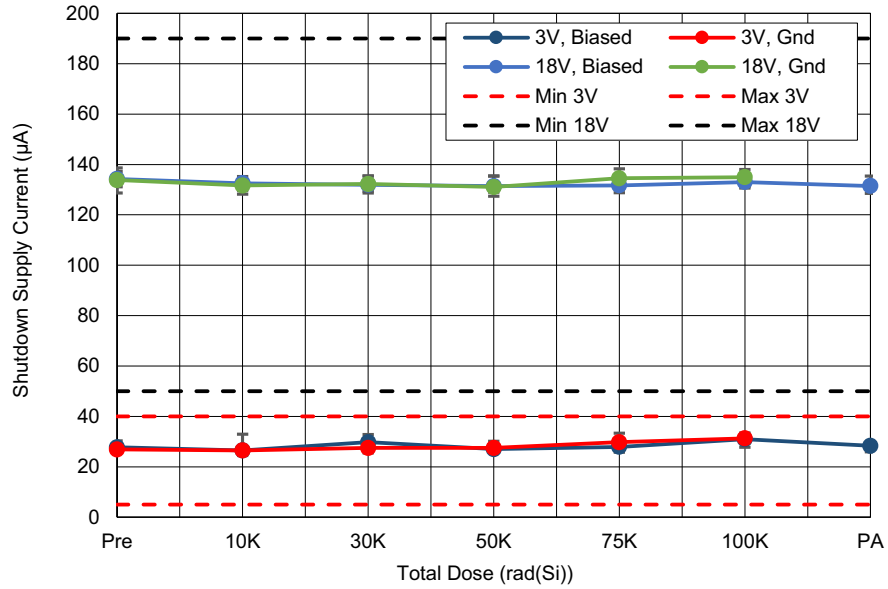


Figure 6. ISL73007SEH shutdown supply current (I_{PVIN_SD}) with PVIN = 3V and 18V, EN = 0V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 5µA minimum and 40µA maximum for PVIN = 3V (shown in red) and 50µA minimum and 190µA maximum for PVIN = 18V (shown in black).

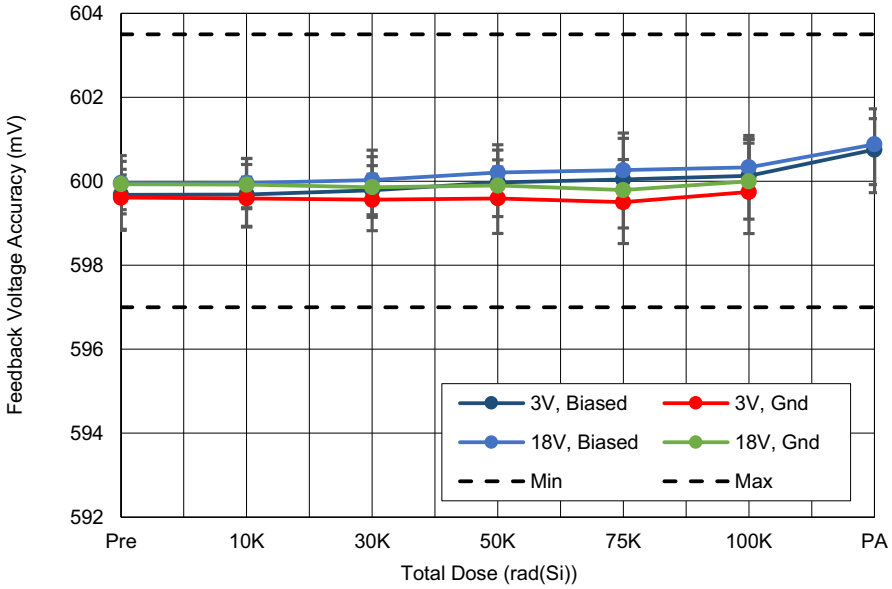


Figure 7. ISL73007SEH feedback voltage accuracy (V_{FB}) at 3V and 18V, as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 597mV minimum and 603.5mV maximum.

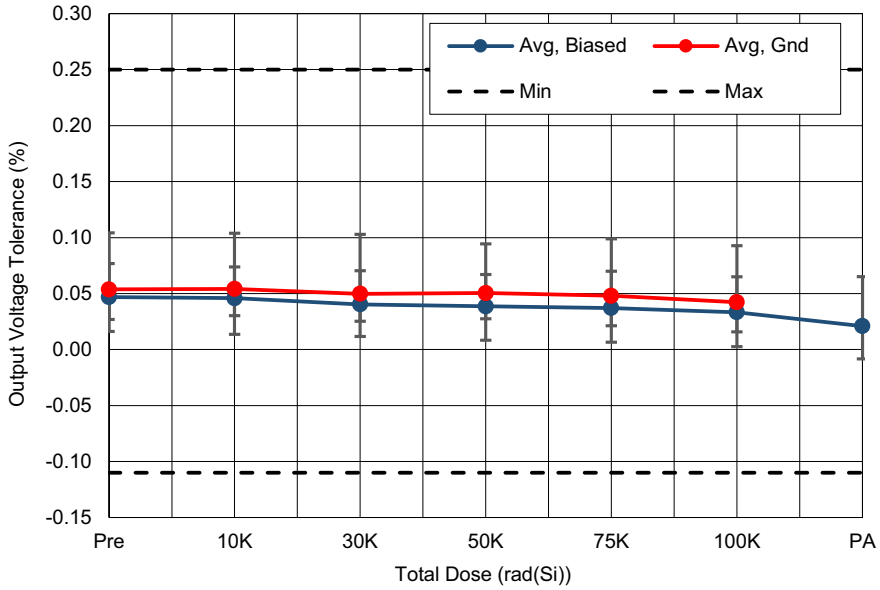


Figure 8. ISL73007SEH output voltage tolerance over input voltage range (LNREG), with PVIN = 3V and 18V using servo loop as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are -0.11% minimum and 0.25% maximum.

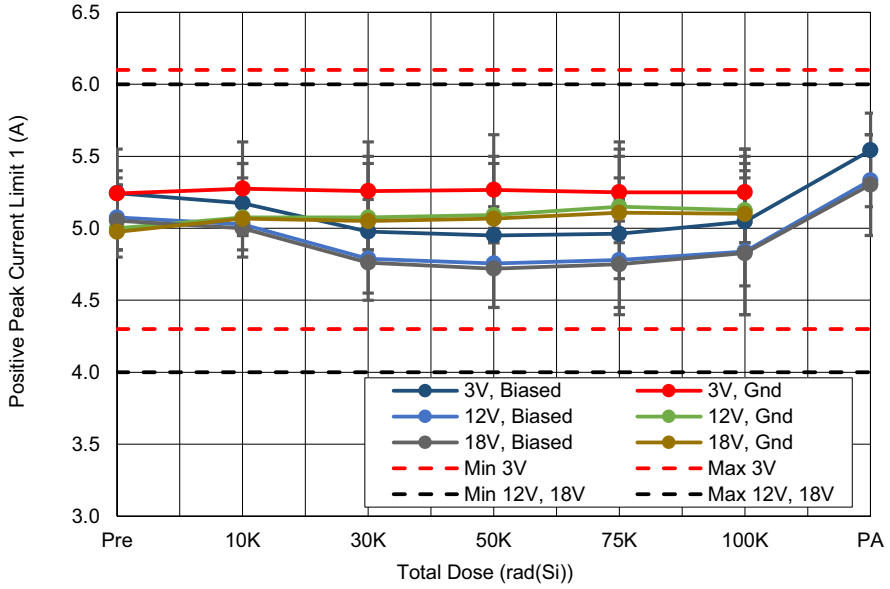


Figure 9. ISL73007SEH positive peak current limit ($I_{IPLIMIT1}$) at PVIN = 3V, 12V, and 18V, as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 4.3A minimum and 6.1A maximum for PVIN = 3V (shown in red) and 4A minimum and 6A maximum for PVIN ≥ 5V (shown in black).

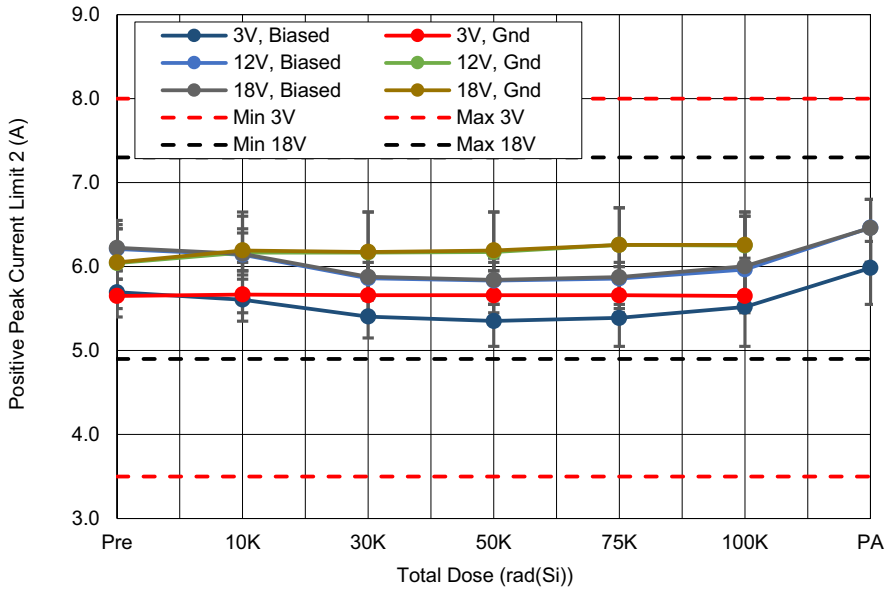


Figure 10. ISL73007SEH positive peak current limit 2 ($I_{IPLIMIT2}$) at PVIN = 3V, 12V, and 18V, as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 3.5A minimum and 8A maximum for PVIN = 3V (shown in red) and 4.9A minimum and 7.3A maximum for PVIN ≥ 5V (shown in black).

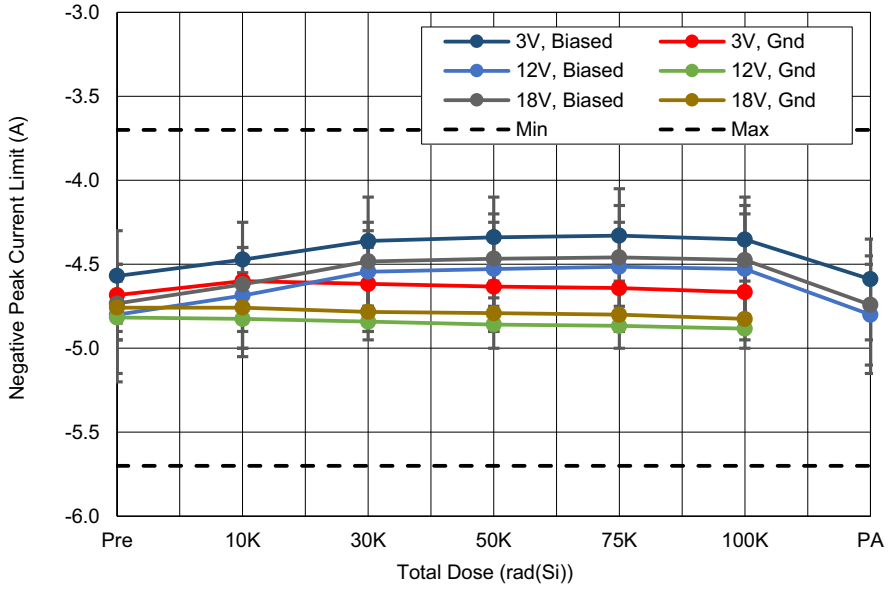


Figure 11. ISL73007SEH negative peak current limit ($-I_{IPLIMIT}$) at PVIN = 3V, 12V, and 18V, as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are -5.7A minimum and -3.7A maximum.

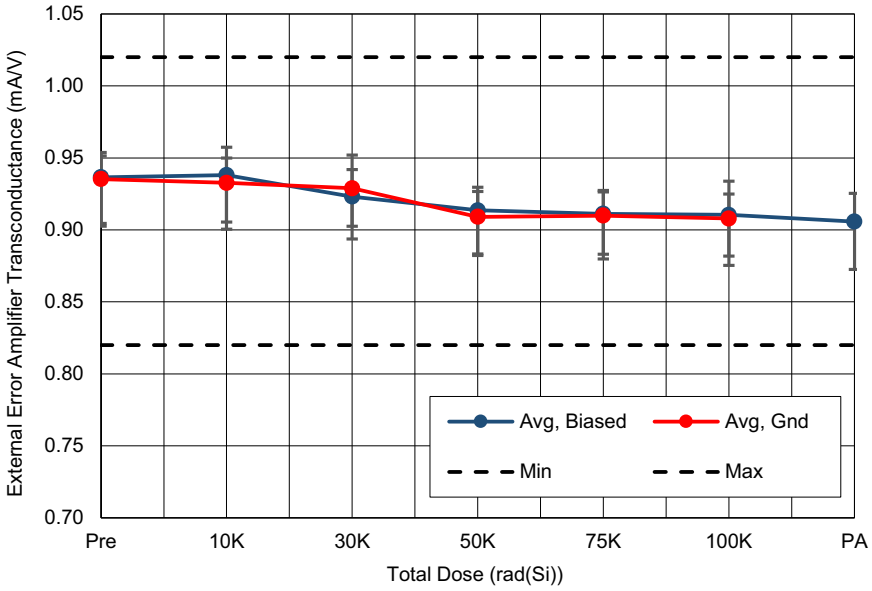


Figure 12. ISL73007SEH external error amplifier transconductance ($EA_{transcon2}$) with PVIN = 5V, delta COMP current/delta FB voltage (10mV), as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 0.82mA/V minimum and 1.02mA/V maximum.

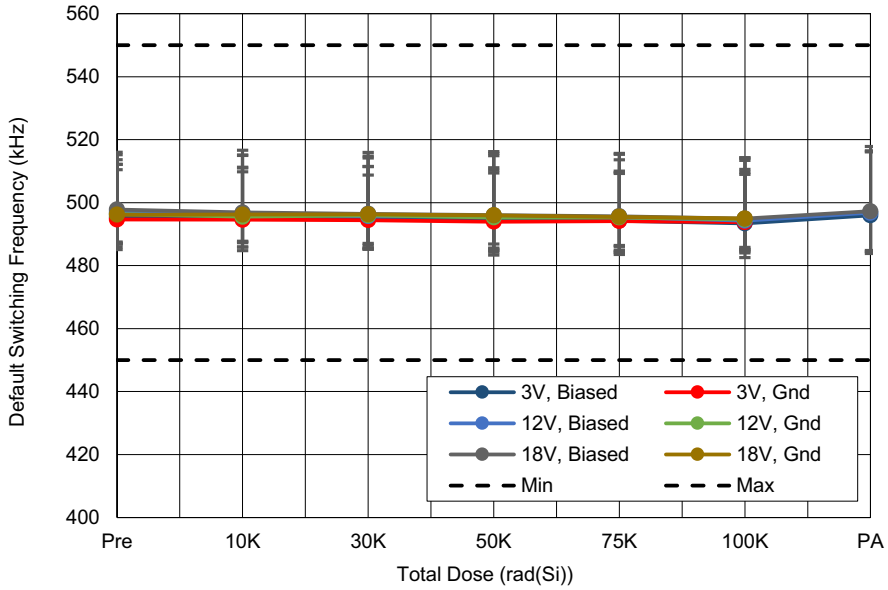


Figure 13. ISL73007SEH default switching frequency (f_{SWd}) with PVIN = 3V, 12V, and 18V; FS = VCC as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 450kHz minimum and 550kHz maximum.

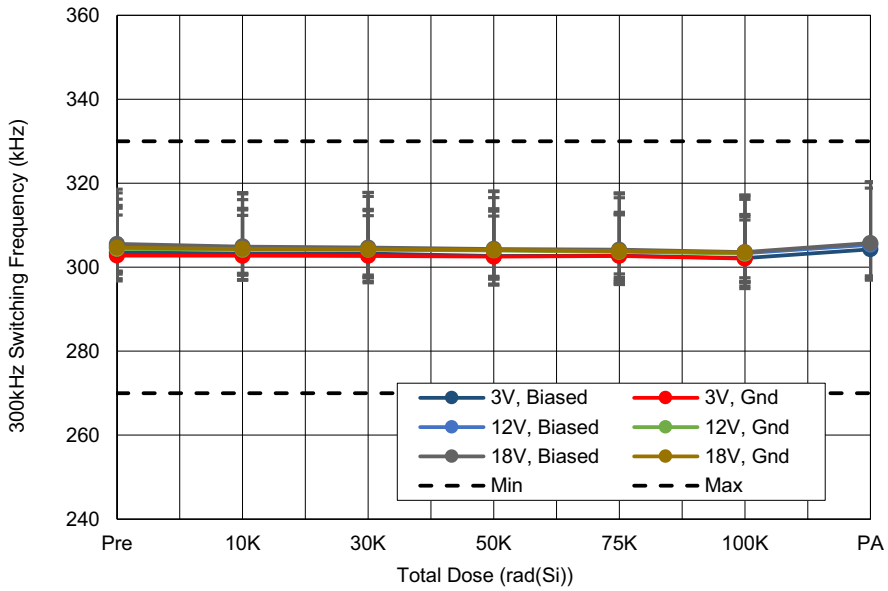


Figure 14. ISL73007SEH 300kHz switching frequency (f_{SW3}) with PVIN = 3V, 12V, and 18V; FS = 174kΩ to GND and VSLOPE = 1.2V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 270kHz minimum and 330kHz maximum.

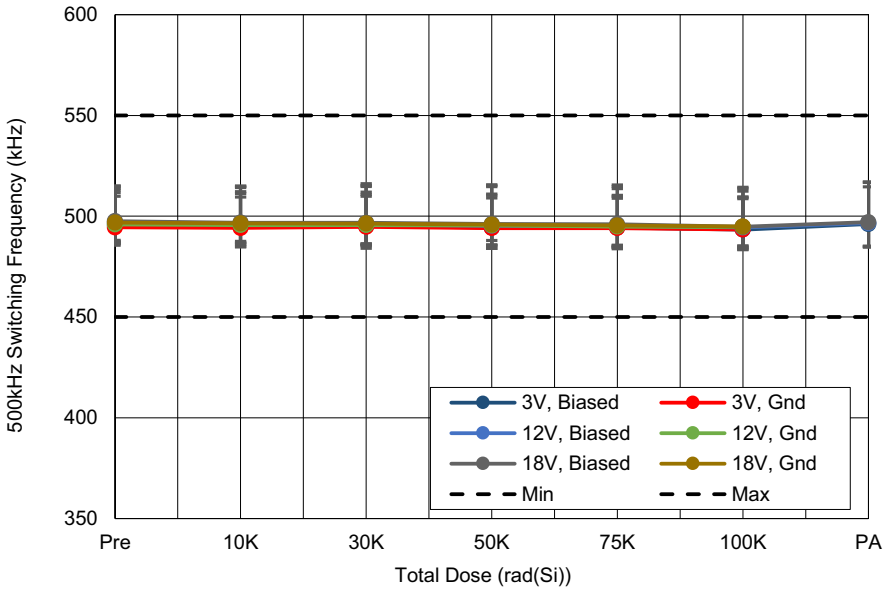


Figure 15. ISL73007SEH 500kHz switching frequency (f_{SW5}) with PVIN = 3V, 12V, and 18V; FS = 100kΩ to GND and VSLOPE = 1.2V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 450kHz minimum and 550kHz maximum.

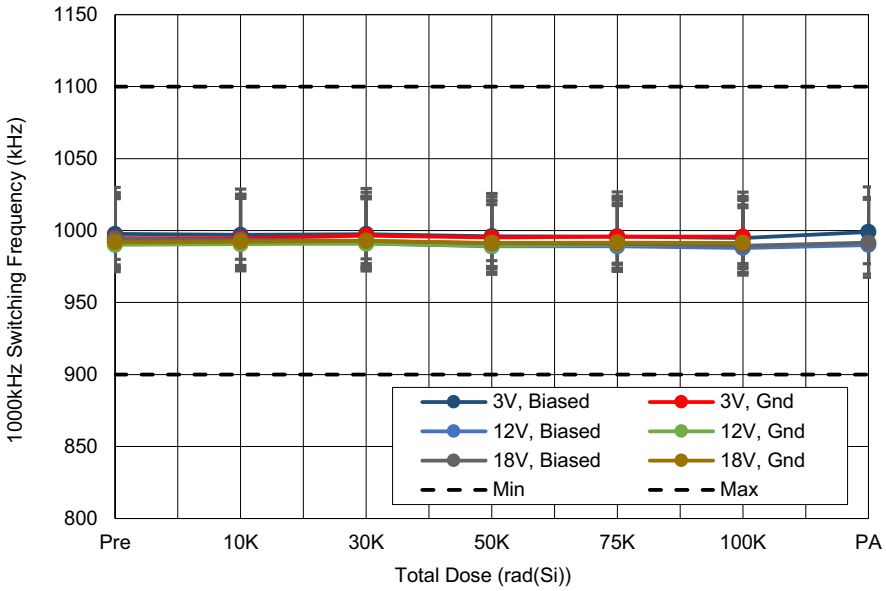


Figure 16. ISL73007SEH 1000kHz switching frequency (f_{SW10}) with PVIN = 3V, 12V, and 18V; FS = 42.7kΩ to GND and VSLOPE = 1.2V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 900kHz minimum and 1100kHz maximum.

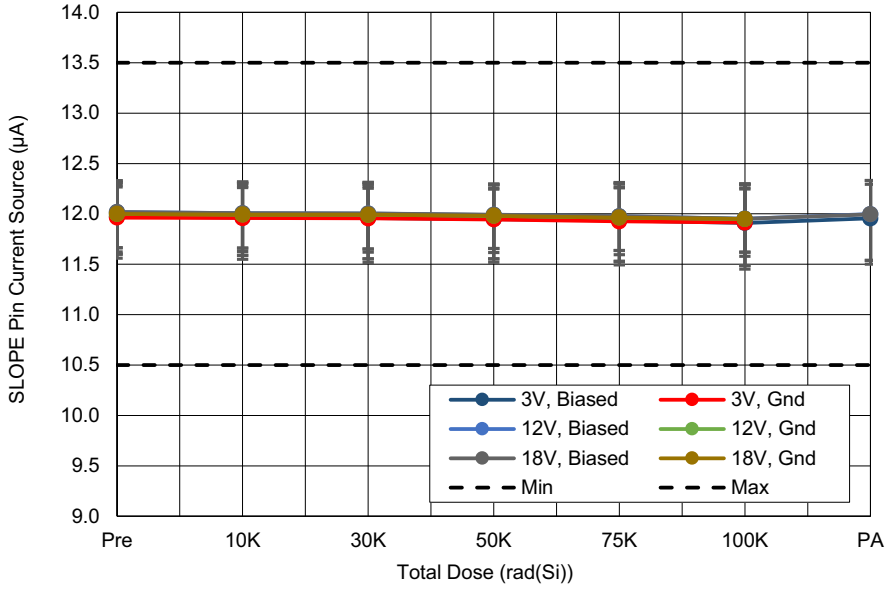


Figure 17. ISL73007SEH SLOPE pin current source (I_{SLOPE}) PVIN = 3V, 12V, and 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 10.5µA minimum and 13.5µA maximum.

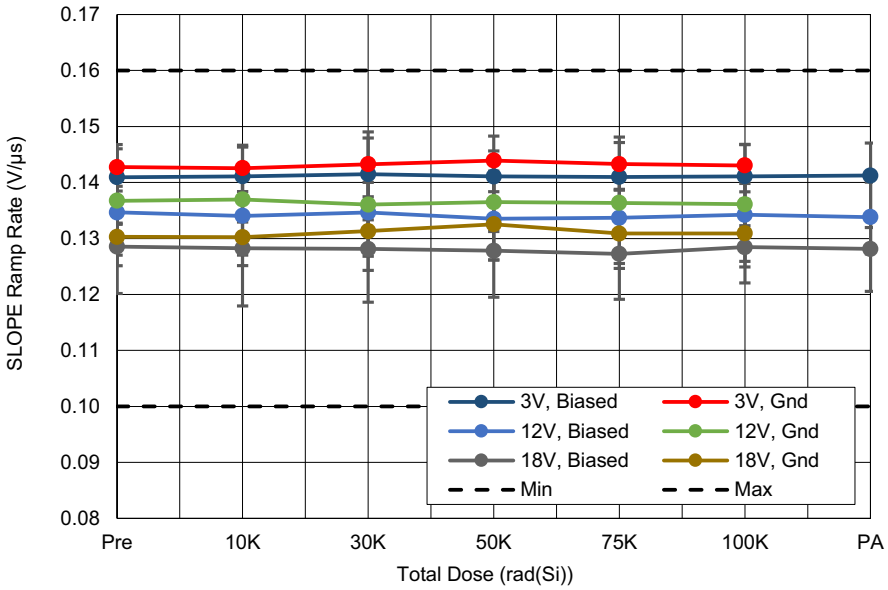


Figure 18. ISL73007SEH internal SLOPE ramp rate (t_{SLOPE}) with PVIN = 3V, 12V, and 18V; (V_{COMP} at 80% DC - V_{COMP} at 20% DC)/(t_{MIN_ON} at 80% DC - t_{MIN_ON} at 20% DC) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 0.1V/µs minimum and 0.16V/µs maximum.

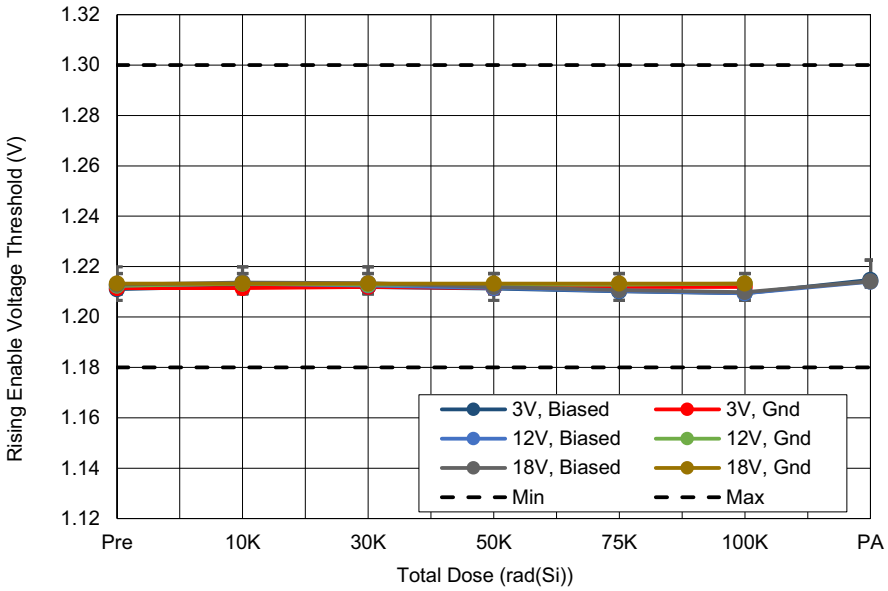


Figure 19. ISL73007SEH rising enable voltage threshold (EN_{VIH}) with PVIN = 3V, 12V, and 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 1.18V minimum and 1.3V maximum.

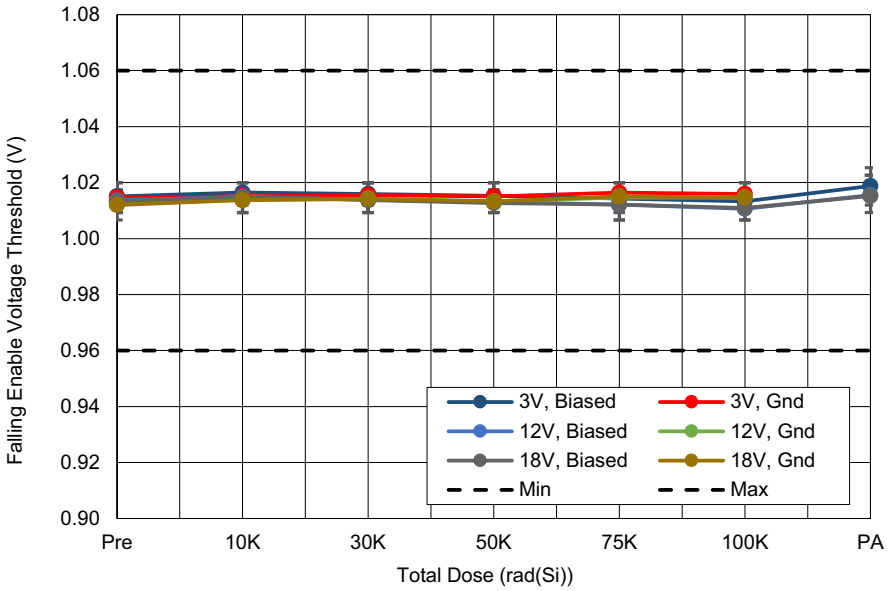


Figure 20. ISL73007SEH fall enable voltage threshold (EN_{VIL}) with PVIN = 3V, 12V, and 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 0.96V minimum and 1.06V maximum.

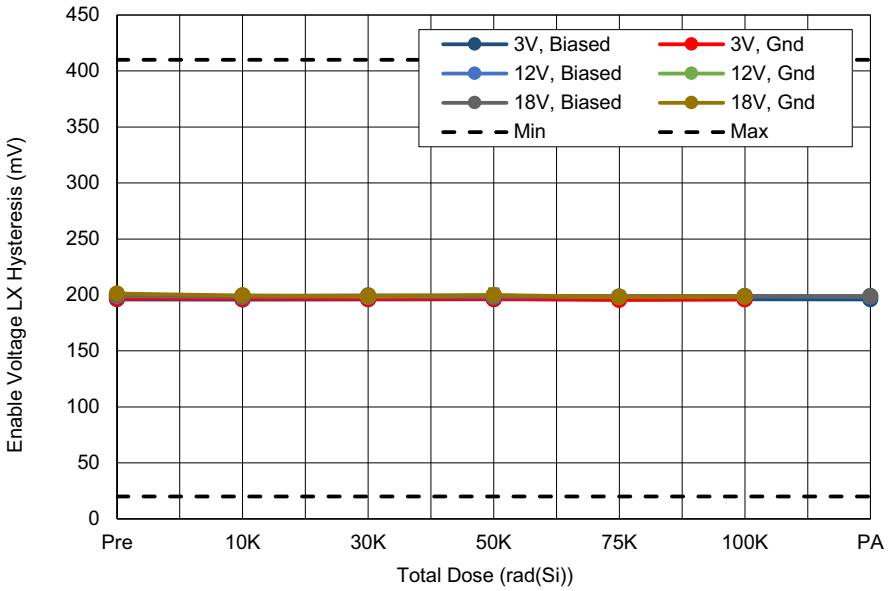


Figure 21. ISL73007SEH enable voltage LX hysteresis (EN_{VIHhys}) with PVIN = 3V, 12V, and 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 20mV minimum and 410mV maximum.

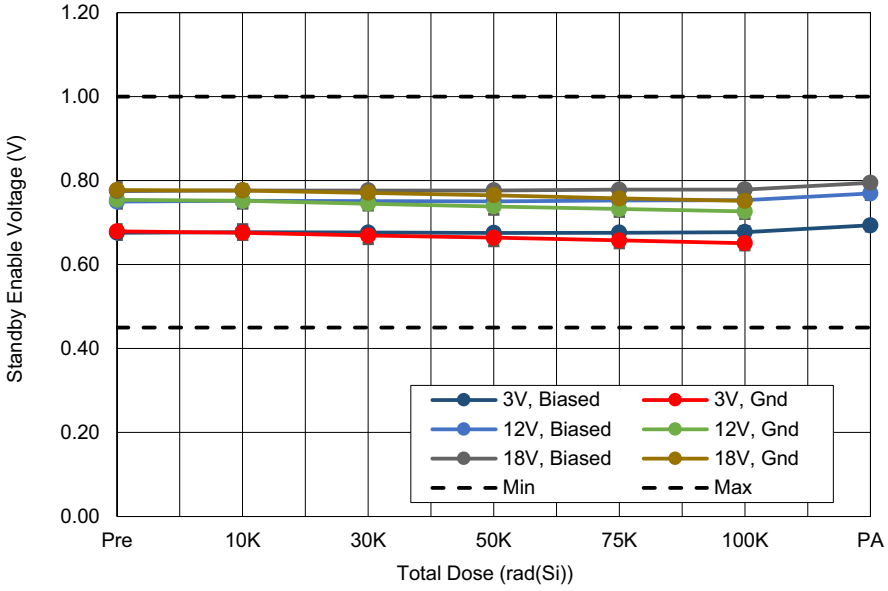


Figure 22. ISL73007SEH standby enable voltage (SB_EN_{VIH}) with PVIN = 3V, 12V, and 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 0.45V minimum and 1V maximum.

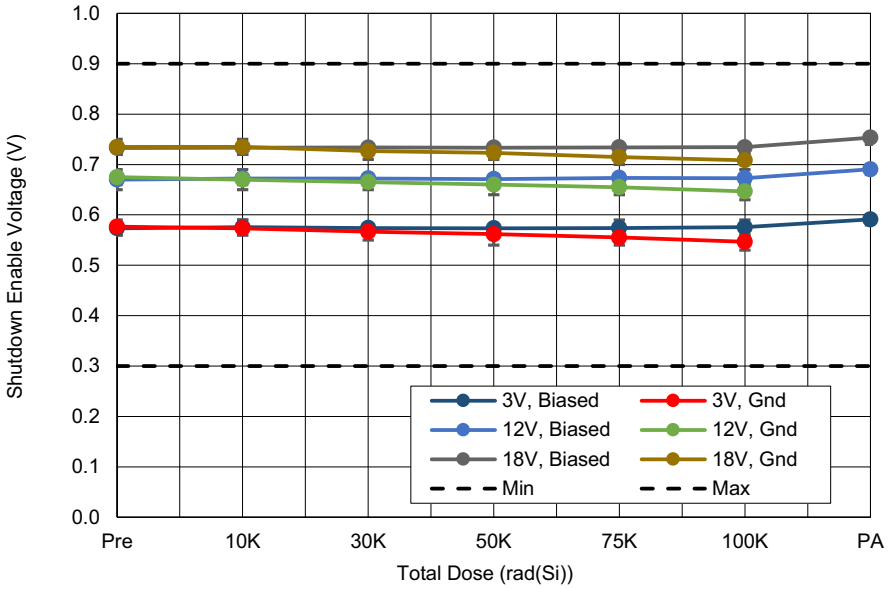


Figure 23. ISL73007SEH shutdown enable voltage (SB_EN_{VIL}) with PVIN = 3V, 12V, and 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 0.3V minimum and 0.9V maximum.

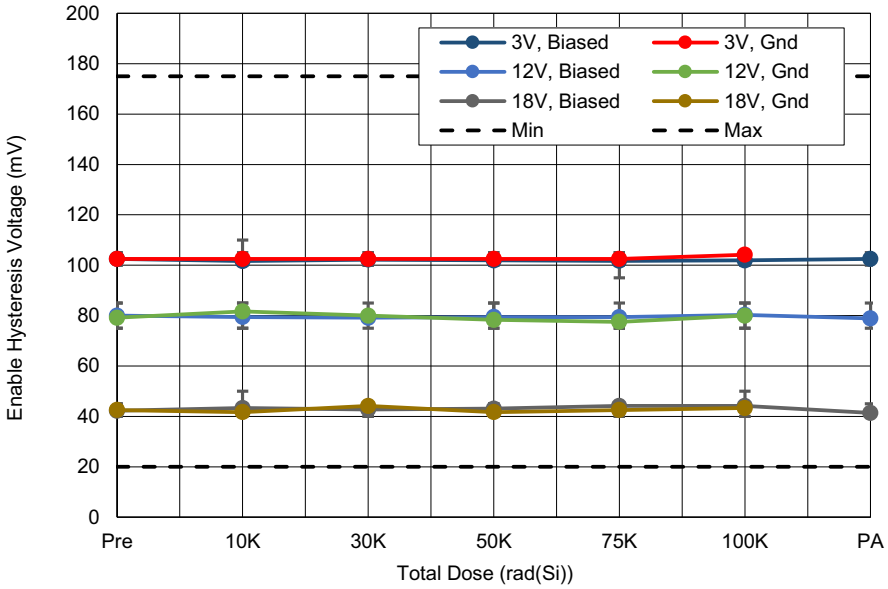


Figure 24. ISL73007SEH enable hysteresis voltage (EN_{HYS}) with PVIN = 3V, 12V, and 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 20mV minimum and 175mV maximum.

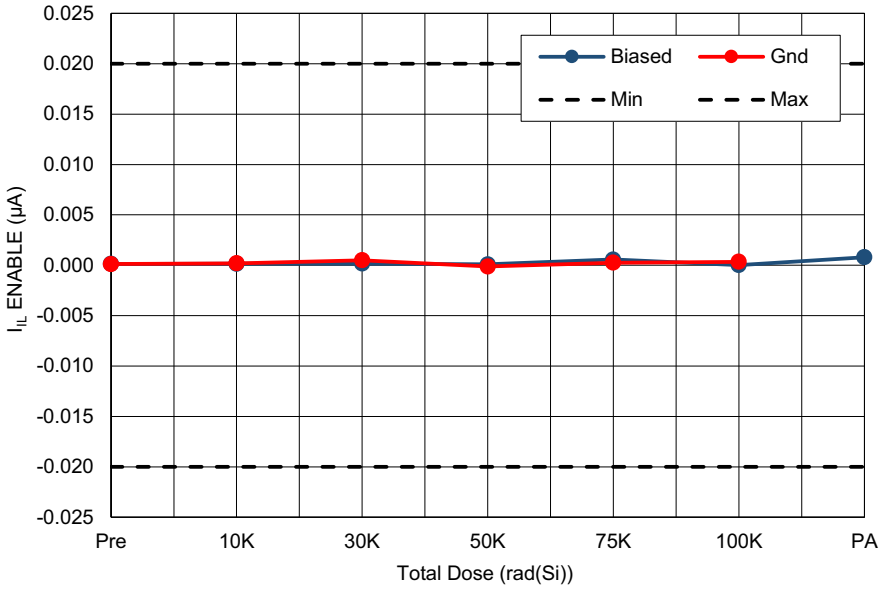


Figure 25. ISL73007SEH low enable current (EN_{IIL}) with as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are -0.02µA minimum and 0.02µA maximum.

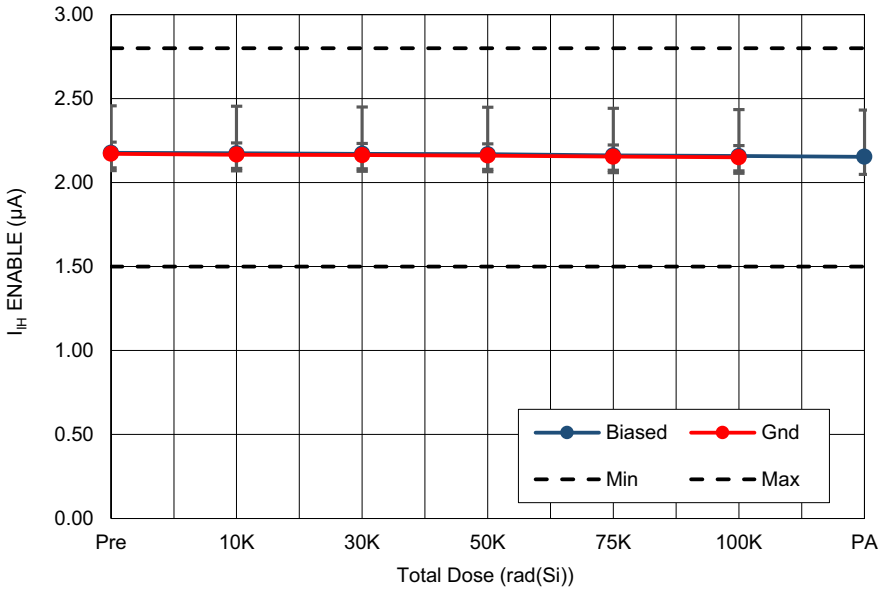


Figure 26. ISL73007SEH high enable current (EN_{IIH}) with as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 1.5µA minimum and 2.8µA maximum.

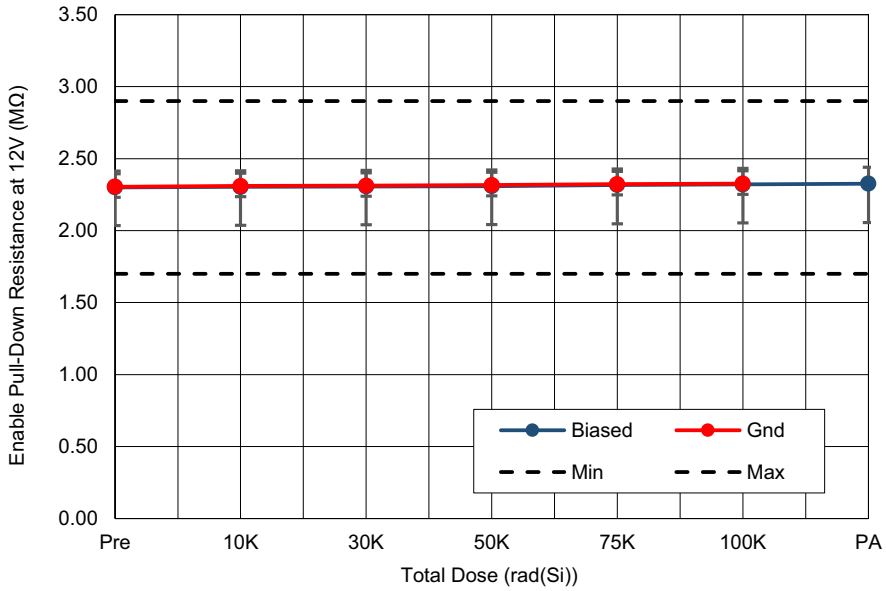


Figure 27. ISL73007SEH enable (EN) pull-down resistance (R_{EN}) with PVIN = 12V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 1.7MΩ minimum and 2.9MΩ maximum.

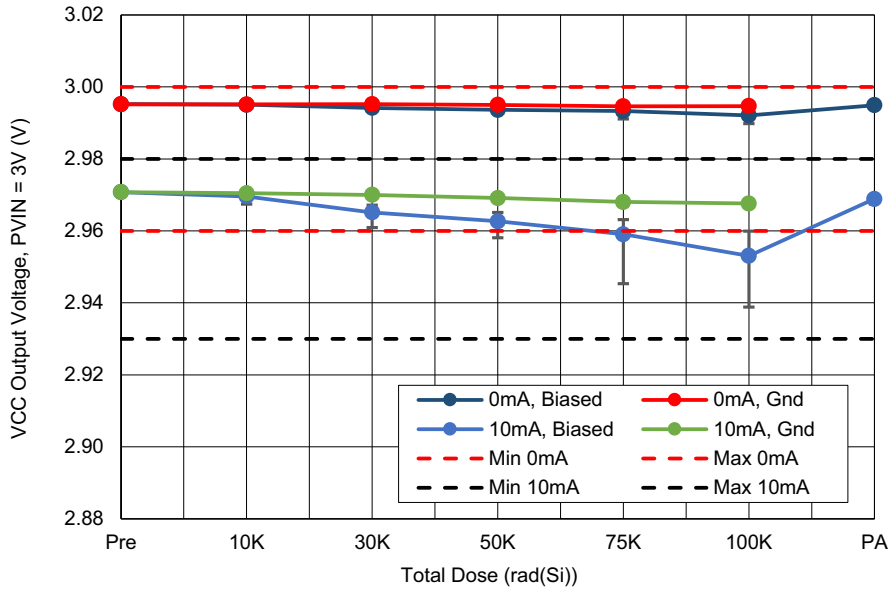


Figure 28. ISL73007SEH VCC Output Voltage ($VOUT_{3V,0mA}$) with PVIN = 3V, I_{OUT} = 0mA, and ($VOUT_{3V,10mA}$) with PVIN = 3V, I_{OUT} = 10mA as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 2.96V minimum and 3V maximum for I_{OUT} = 0mA (shown in red), and 2.93V minimum and 2.98V maximum for I_{OUT} = 10mA (shown in black).

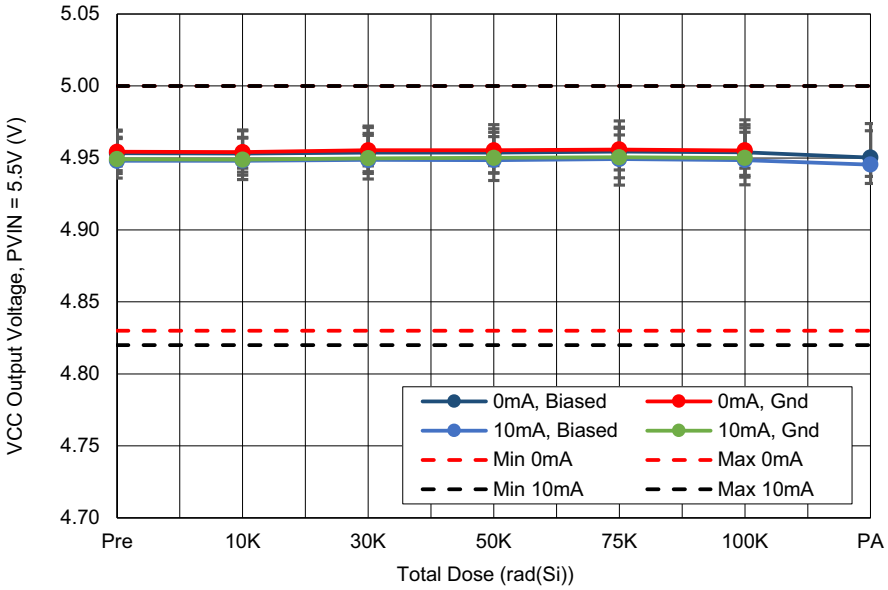


Figure 29. ISL73007SEH VCC Output Voltage ($VOUT_{5.5V,0mA}$) with PVIN = 5.5V, I_{OUT} = 0mA, and ($VOUT_{5.5V,10mA}$) with PVIN = 5.5V, I_{OUT} = 10mA as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 4.83V minimum and 5V maximum for I_{OUT} = 0mA (lower limit shown in red; upper limit shown in black) and 4.82V minimum and 5V maximum for I_{OUT} = 10mA (shown in black).

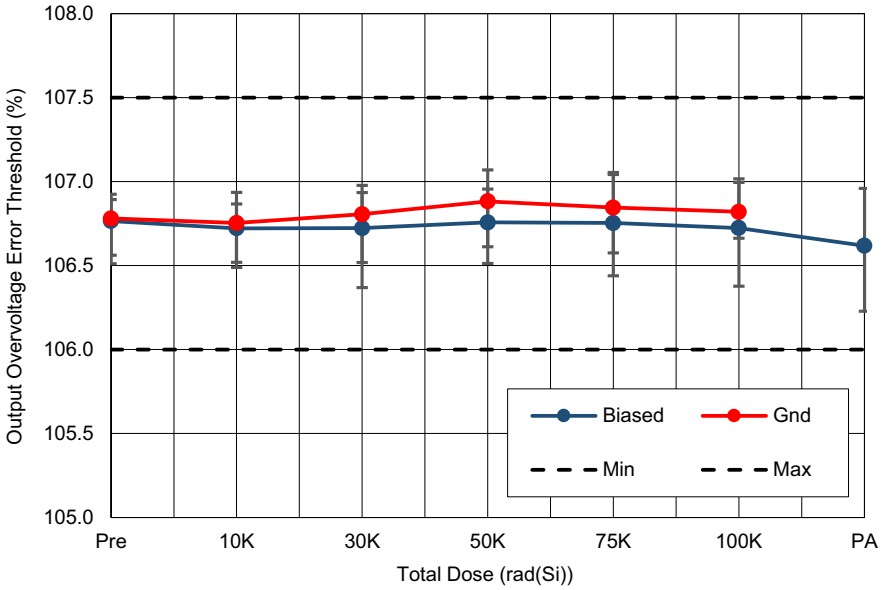


Figure 30. ISL73007SEH output overvoltage error threshold (OVPG) with PVIN = 5V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 106% minimum and 107.5% maximum.

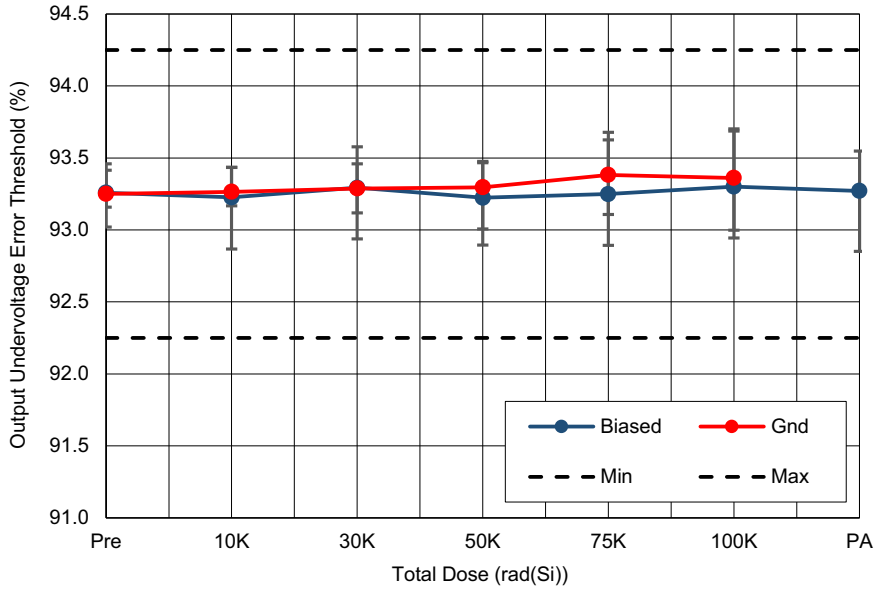


Figure 31. ISL73007SEH undervoltage fault threshold (UVPG) with PVIN = 5V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 92.25% minimum and 94.25% maximum.

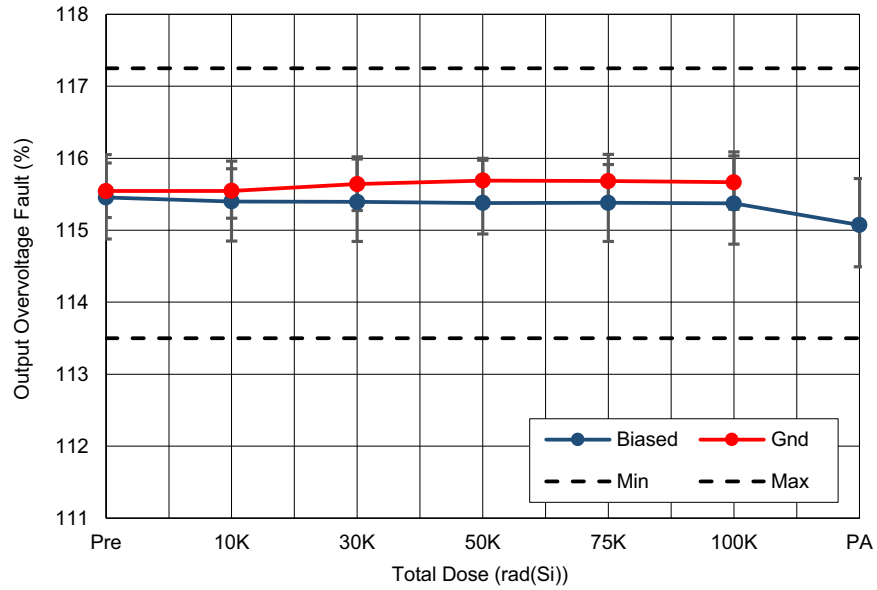


Figure 32. ISL73007SEH output overvoltage fault (OVflt) with PVIN = 5V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 113.5% minimum and 117.25% maximum.

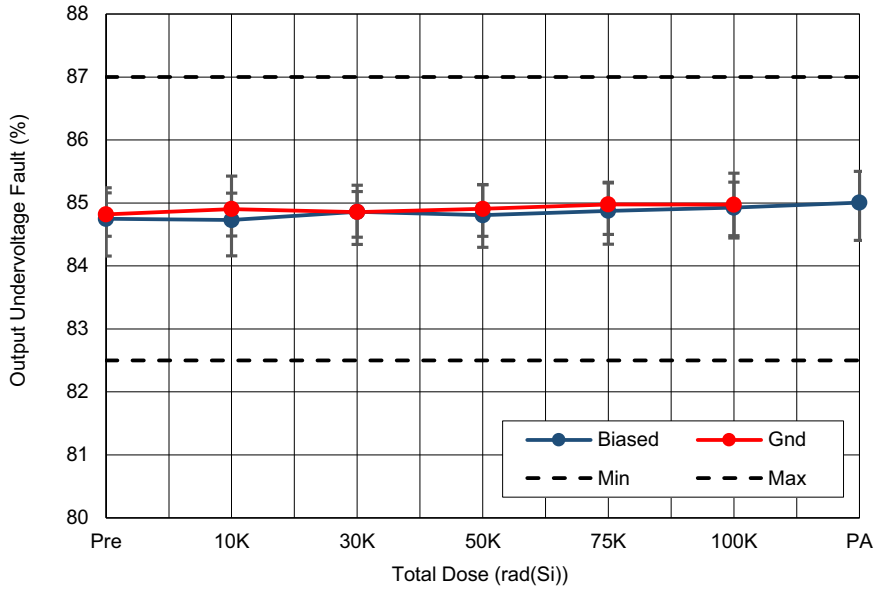


Figure 33. ISL73007SEH output undervoltage fault (UVflt) with PVIN = 5V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 82.5% minimum and 87% maximum.

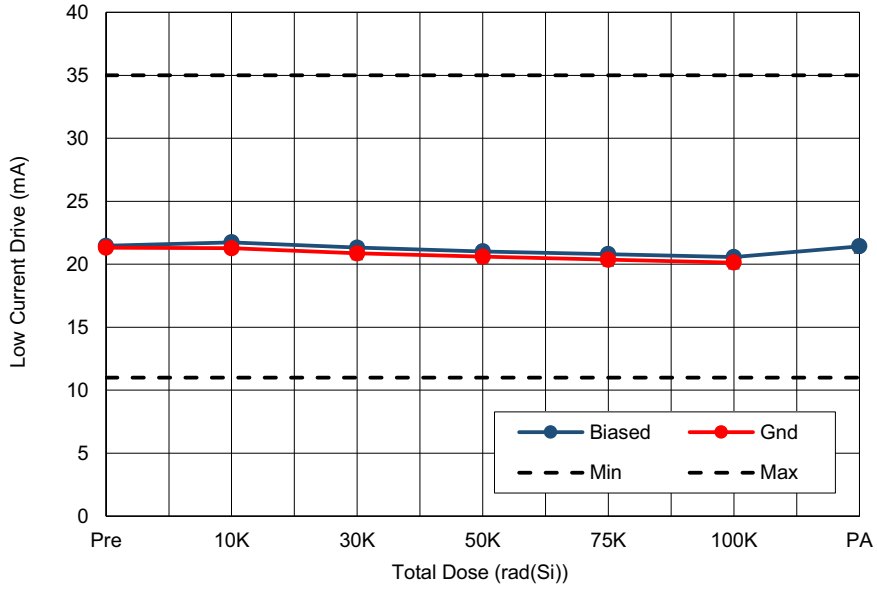


Figure 34. ISL73007SEH low current drive (PG_I_{OL}) with PVIN = 3V, PG = 0.4V, and EN = 0V, as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 11mA minimum and 35mA maximum.

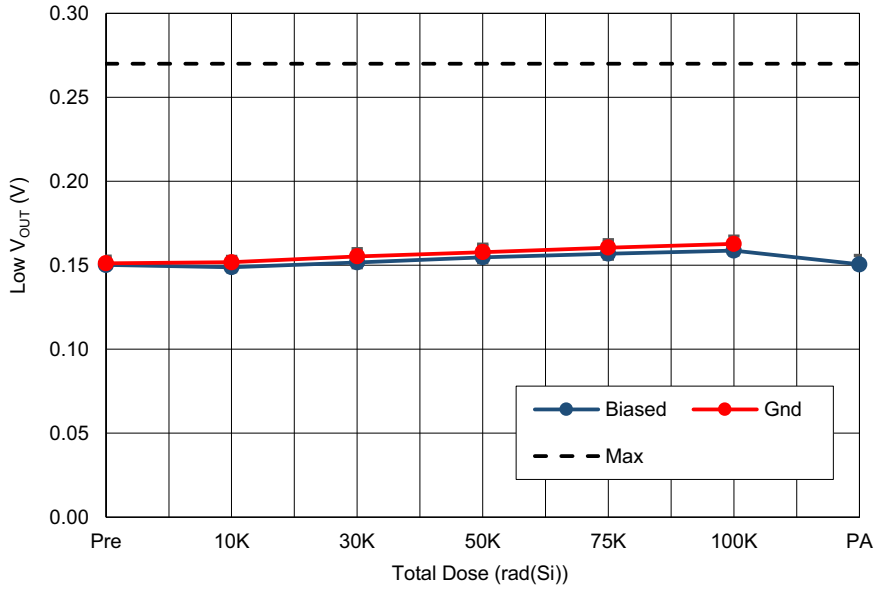


Figure 35. ISL73007SEH low VOUT (PG_V_{OL}) with PVIN = 18V, FB = 0V, EN = 0V, and IPG = 10mA, as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limit is 0.27V maximum.

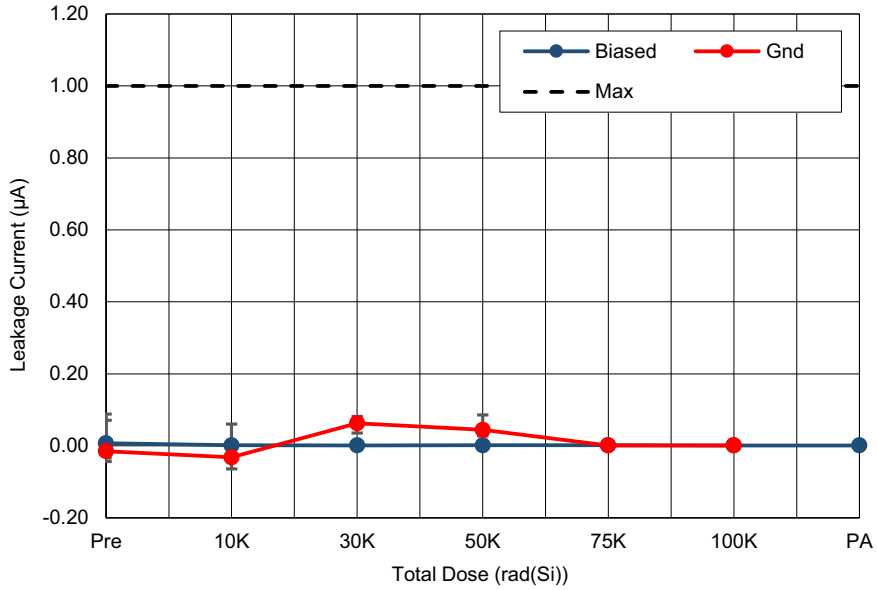


Figure 36. ISL73007SEH leakage (I_{LKGPG}) with PVIN = PG = 18V, as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limit is 1µA maximum.

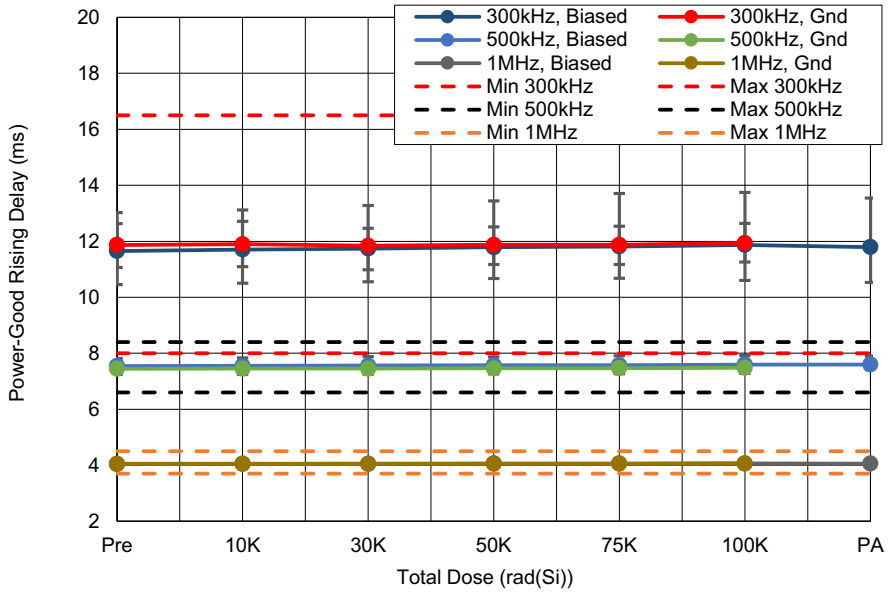


Figure 37. ISL73007SEH power-good rising delay ($t_{SSPGdlyr}$) with PVIN = 5.5V, at 300kHz, 500kHz, and 1MHz, as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 8ms minimum and 16.5ms maximum for 300kHz (shown in red), 6.6ms minimum and 8.4ms maximum for 500kHz (shown in black), and 3.7ms minimum and 4.5ms maximum for 1MHz (shown in orange).

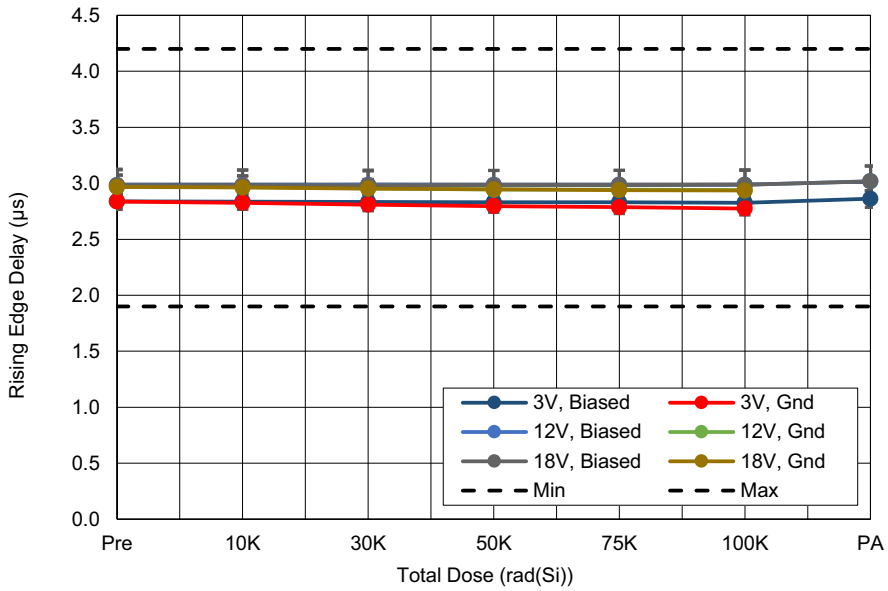


Figure 38. ISL73007SEH rising edge delay (t_{PGdlyr}) with PVIN = 3V, 12V, and 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 1.9µs minimum and 4.2µs maximum.

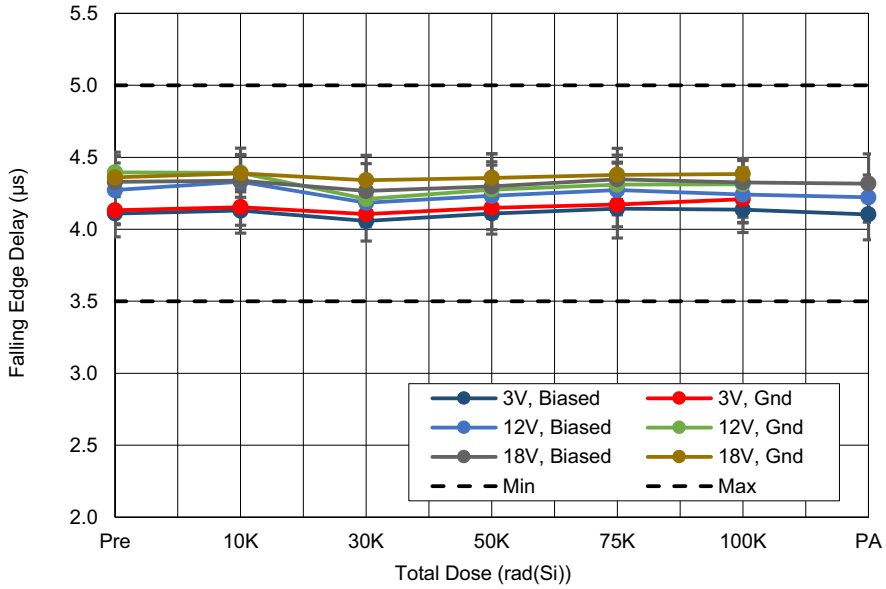


Figure 39. ISL73007SEH falling edge delay (t_{PGdlyf}) with PVIN = 3V, 12V, and 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 3.5µs minimum and 5µs maximum.

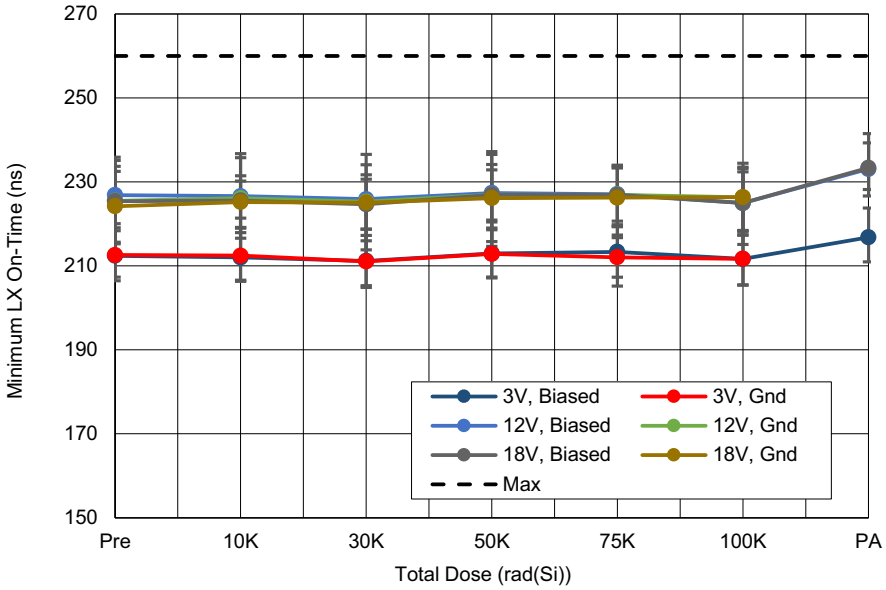


Figure 40. ISL73007SEH minimum LX on-time (t_{MIN_ON}) with PVIN = 3V, 12V, and 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limit is 260ns maximum.

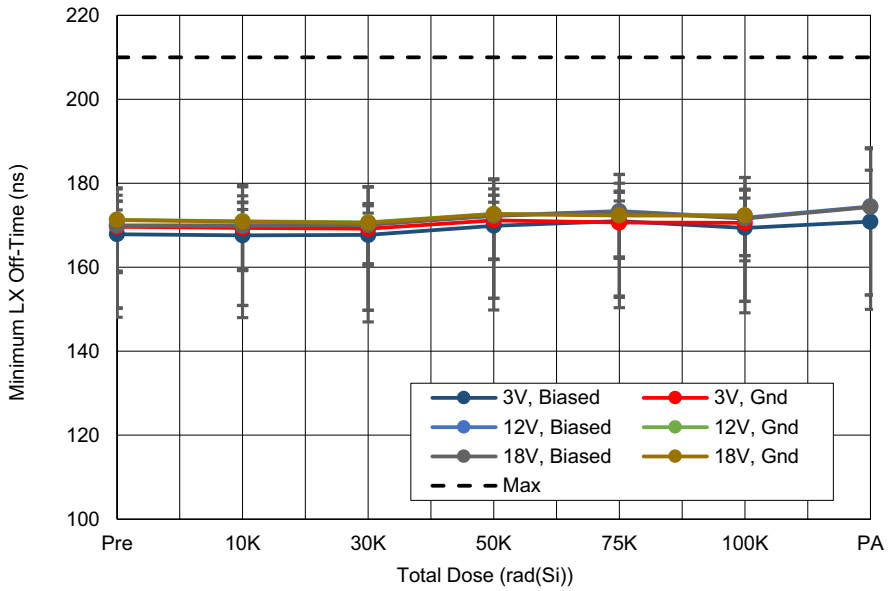


Figure 41. ISL73007SEH minimum LX off-time (t_{MIN_OFF}) with PVIN = 3V, 12V, and 18V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limit is 210ns maximum.

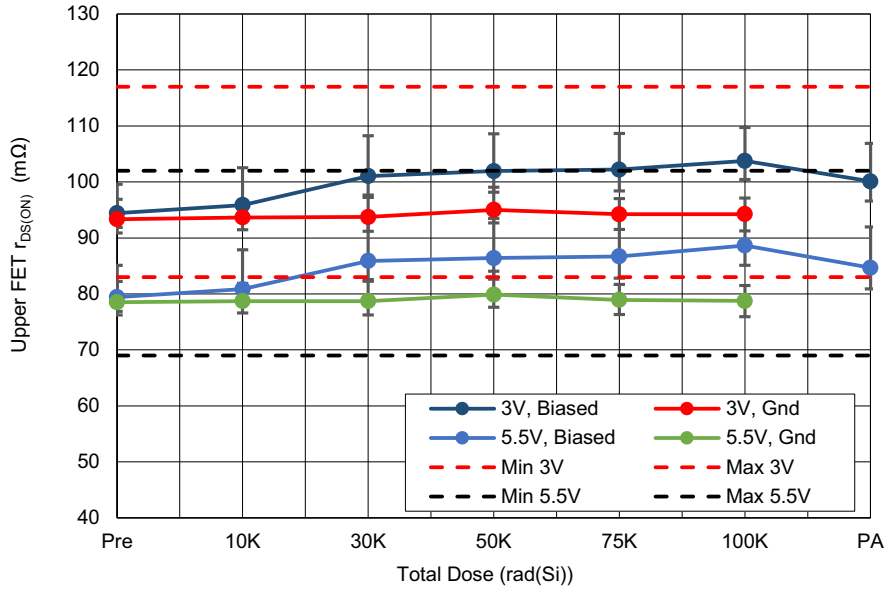


Figure 42. ISL73007SEH post-rad CDFP upper FET ON-resistance ($25UPR_{DSON\_3}$, $25UPR_{DSON\_5}$) with PVIN = 3V and 5.5V, and I_{OUT} = 200mA, as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 83mΩ minimum and 117mΩ maximum for PVIN = 3V (shown in red) and 69mΩ minimum and 102mΩ maximum for PVIN = 5.5V (shown in black).

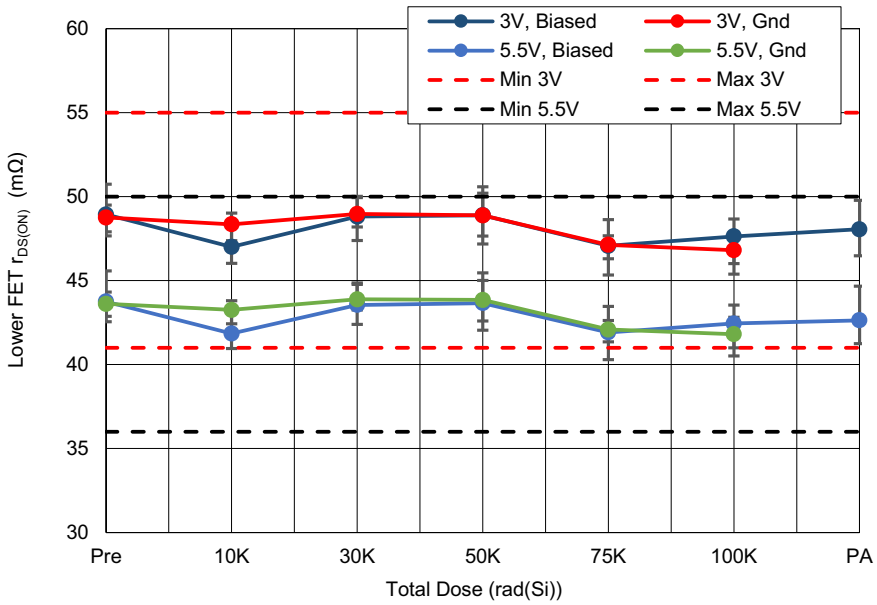


Figure 43. ISL73007SEH post-rad CDFP lower FET ON-resistance ($25LWR_{DSON\_3}$, $25LWR_{DSON\_3}$) with PVIN = 3V and 5.5V, and I_{OUT} = 200mA, as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation datasheet limits are 41mΩ minimum and 55mΩ maximum for PVIN = 3V (shown in red) and 36mΩ minimum and 50mΩ maximum for PVIN = 5.5V (shown in black).

3. Discussion and Conclusion

This document reports the LDR total dose testing results of the ISL73007SEH synchronous buck controller. Biased and grounded samples were irradiated to 100krad(Si) at a dose rate of 0.01rad(Si)/s. The biased units were then placed on a 168-hour anneal at 100°C under the same bias at which they were irradiated. The Attributes Data section summarizes the attributes data for the test, and the Key Parameter Variables Data section provides plots of the total dose response for those parameters.

All tested datasheet parameters passed at all downpoints. No evidence of bias dependence was observed.

4. Revision History

Revision	Date	Description
1.00	Apr 11, 2023	Initial release.

Appendix

Table 3 lists the datasheet parameters that are considered indicative of part performance. These parameters are plotted in Figure 3 through Figure 43. All limits are taken from the ISL73007SEH datasheet, which has more details on test conditions.

Table 3. ISL73007SEH Datasheet Total Dose Parameters (T_A = 25°C)

Fig.	Parameter	Symbol	Conditions	Low Limit	High Limit	Unit
3	Rising Undervoltage Lockout	V_{PVIN_UVLO}	EN = 2.25V	-	2.95	V
	Falling Undervoltage Lockout		EN = 2.25V	2.7	-	
4	Operating Supply Current	I_{PVIN_OPER}	PVIN = 18V, EN = 5V, ext. 500kHz, no load	28	42	mA
5	Stand-by Supply Current	I_{PVIN_SB}	PVIN = 3V, EN = 1V	1.1	1.7	mA
			PVIN = 18V, EN = 1V	1	1.4	
6	Shutdown Supply Current	I_{PVIN_SD}	PVIN = 3V, EN = 0V	5	40	µA
			PVIN = 18V, EN = 0V	50	190	
7	Feedback Voltage Accuracy	V_{FB}	V_{FB} (including Error Amplifier V_D to SGND)	597	603.5	mV
8	Output Voltage Tolerance Over Input Voltage Range	LNREG	PVIN = 3V, 18V using servo loop	-0.11	0.25	%
9	Positive Peak Current Limit[1]	$I_{IPLIMIT1}$	PVIN = 3V	4.3	6.1	A
			PVIN = ≥ 5V	4	6	
10		$I_{IPLIMIT2}$	PVIN = 18V	4.9	7.3	A
11	Negative Peak Current Limit [1]	$-I_{IPLIMIT}$	PVIN = ≥3V	-5.7	-3.7	A
12	External Error Amplifier Transconductance	$EA_{transcon2}$	PVIN = 5V, delta COMP current/delta FB Voltage (10mV)	0.82	1.02	mA/V
13	Default Switching Frequency	f_{SWd}	FS = VCC	450	500	kHz
14	300kHZ Switching Frequency	f_{SW3}	FS = 174kΩ to GND, V_{SLOPE} = 1.2V	270	330	kHz
15	500kHZ Switching Frequency	f_{SW5}	FS = 100kΩ to GND, V_{SLOPE} = 1.2V	450	550	kHz
16	1000kHZ Switching Frequency	f_{SW10}	FS = 42.7kΩ to GND, V_{SLOPE} = 1.2V	900	1100	kHz
17	SLOPE Pin Current Source	I_{SLOPE}		10.5	13.5	µA
18	Internal SLOPE Ramp Rate	t_{SLOPE}	(V_{COMP} at 80% DC - V_{COMP} at 20% DC)/ (t_{MIN_ON} at 80% DC - t_{MIN_ON} at 20% DC)	0.1	0.16	V/µs
19	Rising Enable Voltage Threshold	EN_{VIH}	Enable Rising to LX Switching	1.18	1.3	V
20	Falling Enable Voltage Threshold	EN_{VIL}	Enable Falling to LX Stops Switching	0.96	1.06	V
21	Enable Voltage LX Hysteresis	EN_{VIHhys}		20	410	mV
22	Standby Enable Voltage	SB_EN_{VIH}	Enable Rising to VCC Enabled	0.45	1	V
23	Shutdown Enable Voltage	SB_EN_{VIL}	Enable Falling to VCC Disabled	0.3	0.9	V
24	Enable Hysteresis Voltage	EN_{HYS}	Enable Rising to LX Switching - EN Falling to VCC Disable	20	175	mV
25	Low Enable Current	EN_{IIL}		-20	20	nA
26	High Enable Current	EN_{IIH}		1.5	2.8	µA

Table 3. ISL73007SEH Datasheet Total Dose Parameters (T_A = 25°C) (Cont.)

Fig.	Parameter	Symbol	Conditions	Low Limit	High Limit	Unit
27	Enable (EN) Pull-Down Resistance	R_{EN}	PVIN = 12V	1.7	2.9	MΩ
28	VCC Output Voltage	$VOUT_{3V,0mA}$	PVIN = 3V, I_{OUT} = 0mA	2.96	3	V
		$VOUT_{3V,10mA}$	PVIN = 3V, I_{OUT} = 10mA	2.93	2.98	
29		$VOUT_{5.5V,0mA}$	PVIN = 5.5V, I_{OUT} = 0mA	4.83	5	
		$VOUT_{5.5V,10mA}$	PVIN = 5.5V, I_{OUT} = 10mA	4.82	5	
30	Output Overvoltage Error Threshold	OVPG	PVIN = 5V, FB as a % of VREF	106	107.5	%
31	Output Undervoltage Error Threshold	UVPG	PVIN = 5V, FB as a % of VREF	92.25	94.25	%
32	Output Overvoltage Fault	OVflt	PVIN = 5V, FB as a % of VREF	113.5	117.25	%
33	Output Undervoltage Fault	UVflt	PVIN = 5V, FB as a % of VREF	82.5	87	%
34	Low Current Drive	PG_I_{OL}	PVIN = 3V, PG = 0.4V, EN = 0V	11	35	mA
35	Low V_{OUT}	PG_V_{OL}	PVIN = 18V, FB = 0V, EN = 0V, IPG = 10mA	-	0.27	V
36	Leakage	I_{LKGPG}	PVIN = PG = 18V	-	1	µA
37	Power-Good Rising Delay	$t_{SSPGdlyr}$	PVIN = 5.5V From EN edge to PG high, 300kHz	8	16.5	ms
			PVIN = 5.5V From EN edge to PG high, 500kHz	6.6	8.4	
			PVIN = 5.5V From EN edge to PG high, 1000kHz	3.7	4.5	
38	Rising Edge Delay	t_{PGdlyr}	Return to regulation to PG response	1.9	4.2	µs
39	Falling Edge Delay	t_{PGdlyf}	Out of regulation to PG response	3.5	5.0	µs
40	Minimum LX On-Time	t_{MIN_ON}	PVIN = 3V, 12V and 18V, Forced Min On-Time by COMP bias, No Load	-	260	ns
41	Minimum LX Off-Time	t_{MIN_OFF}	PVIN = 3V, 12V and 18V, Forced Min Off-Time by COMP bias, No Load	-	210	ns
42	Post Rad CDFP Upper FET $r_{DS(ON)}$ [1]	$25UPR_{DSON\_3}$	PVIN = 3.0V, I_{OUT} = 200mA	83	117	mΩ
		$25UPR_{DSON\_5}$	PVIN = 5.5V, I_{OUT} = 200mA	69	102	
43	Post Rad CDFP Lower FET $r_{DS(ON)}$ [1]	$25LWR_{DSON\_3}$	PVIN = 3.0V, I_{OUT} = 200mA	41	55	mΩ
		$25LWR_{DSON\_5}$	PVIN = 5.5V, I_{OUT} = 200mA	36	50	

1. Parameter tested in a Test Mode not available to user.

Related Information

For a full list of related documents, visit our website:

- ISL73007SEH device page
- MIL-STD-883 Test Method 1019

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

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