ISL73033SLHM

Total Dose Test Report

Introduction

This report documents the results of Low Dose Rate (LDR) total dose testing and subsequent high-temperature biased annealing of the ISL73033SLHM GaN FET + Driver. The tests were conducted to provide an assessment of the total dose hardness of the part and to provide an estimate of bias or anneal sensitivity. Parts were irradiated biased and unbiased at LDR (0.01rad(Si)/s) to 100krad(Si), followed by a 168-hour high temperature anneal at 100°C under bias. The ISL73033SLHM is rated to 75krad(Si) at LDR.

Product Description

The ISL73033SLHM is a radiation hardened Dri-GaN power stage with a 100V enhancement mode Gallium Nitride (GaN) FET in one package. The device simplifies the Printed Circuit Board (PCB) layout by integrating a driver plus GaN FET in one package and is designed for isolated topologies and boost type configurations. The driver operates with a supply voltage from 4.5V to 13.2V and has both inverting (INB) and non-inverting (IN) inputs to satisfy requirements for inverting and non-inverting gate drives with a single device.

The ISL73033SLHM has a 4.5V gate drive voltage (V_{DRV}) generated using an internal regulator that prevents the gate voltage from exceeding the maximum gate-source rating of enhancement-mode GaN FETs. The gate drive voltage also features Undervoltage Lockout (UVLO) protection that ignores the inputs (IN/INB) and keeps the GaN FET in an OFF state whenever V_{DRV} is below the UVLO threshold.

The ISL73033SLHM inputs can withstand voltages up to 14.7V regardless of the V_{DD} voltage, allowing the inputs to be connected directly to most PWM controllers.

The ISL73033SLHM is offered in an 81 ball 8x8mm Ball Grid Array (BGA) package. The block diagram for the ISL73033SLHM is shown in Figure 1.

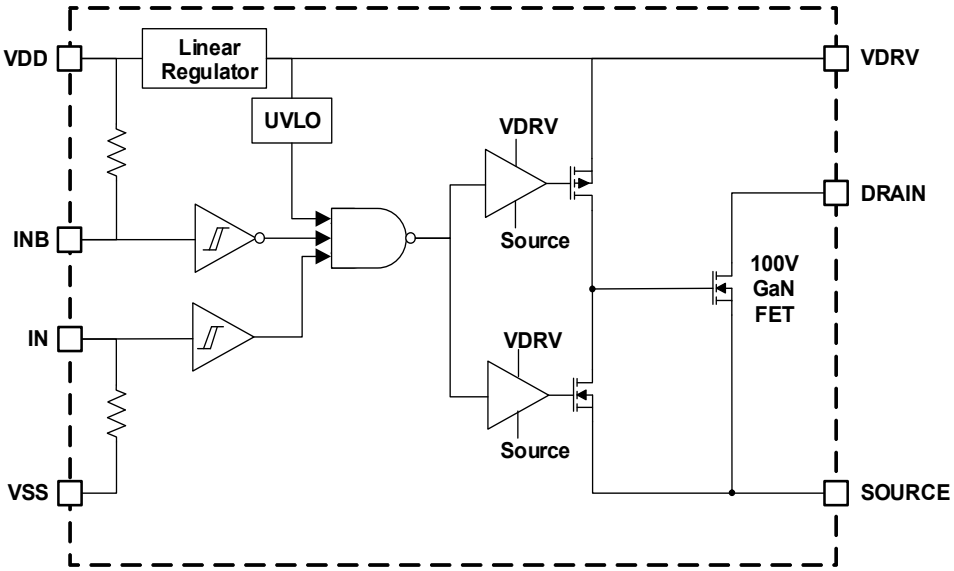

Figure 1. Functional Block Diagram

Related Information

- MIL-STD-883 Test Method 1019
- ISL73033SLHM Datasheet

The pin configurations for the ISL73033SLHM is shown in Figure 2 with the pin descriptions shown in Table 1.

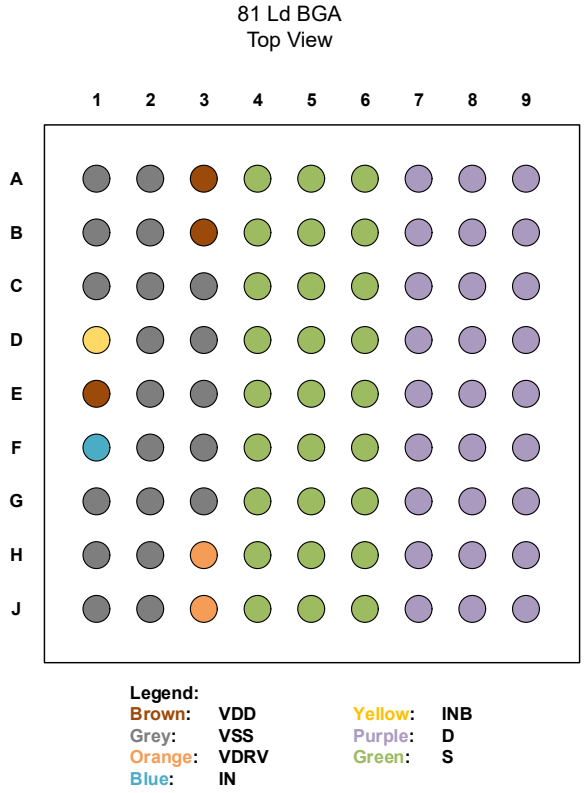

Figure 2. ISL73033SLHM Package and Pin Configurations

Table 1. ISL73033SLHM Pin Descriptions

Pin Name	ESD Circuit	Description
VDD	2	Supply for the internal linear regulator. Bypass the supply to VDD using at least a 4.7µF ceramic capacitor.
VSS	-	Ground reference for the logic circuitry. Internally shorted to Source.
VDRV	1	Gate drive voltage generated by the internal linear regulator. Bypass the supply to VDD using at least a 4.7µF ceramic capacitor. See the Applications Information section in the datasheet for more details.
IN	2	Non-inverting TTL/CMOS input pin that controls the gate of the GaN FET. When using this device in an inverting application, tie this pin to VDD.
INB	2	Inverting TTL/CMOS input pin that controls the gate of the GaN FET. When using this device in a non-inverting application, tie this pin to VSS.
D	-	Drain connection for the GaN FET
S	-	Source connection for the GaN FET

1. Test Description

1.1 Irradiation Facilities

The irradiation was performed at 0.01rad(Si)/s using the Renesas Palm Bay Hopewell Designs N40 panoramic commercial irradiator. This irradiator uses PbAl spectrum hardening filters to shield the test board and devices under test against low energy secondary gamma radiation. Biased irradiation and annealing were performed on all samples following irradiation, at 100°C for 168 hours in a small temperature chamber.

1.2 Test Fixturing

Figure 3 shows the configuration used for biased irradiation.

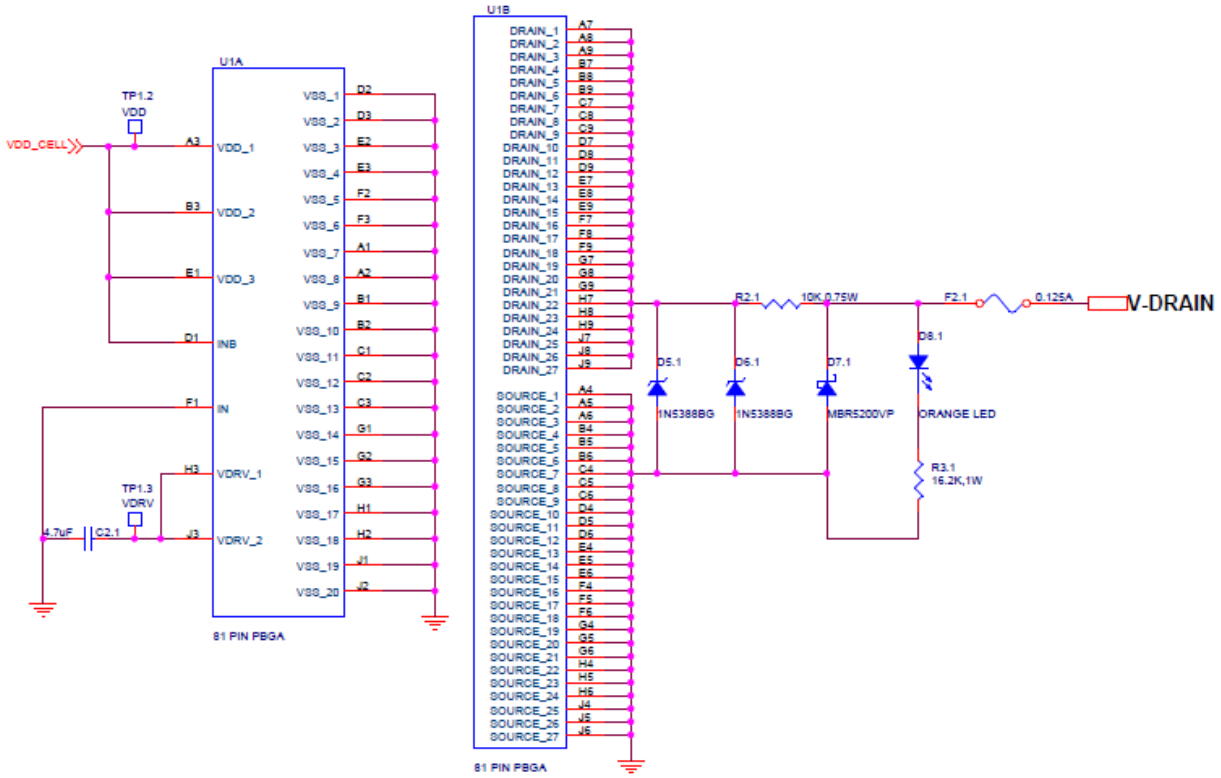

Figure 3. ISL73033SLHM TID Bias Schematic (V_{DD} = 13.2V, V-DRAIN = 84V (±4V)

1.3 Characterization Equipment and Procedures

All electrical testing was performed at room temperature outside the irradiator, using production Automated Test Equipment (ATE) with datalogging at each downpoint.

1.4 Experimental Matrix

Irradiation was performed in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 24 samples irradiated under bias and 24 samples irradiated with all pins grounded. At anneal, all samples were biased.

The ISL73033SLHM samples were drawn from wafer lot 1WZ3BA (Tracecode - 1WZ3BAU) for the ISL73040 Driver and the GaN FETs came from wafer lot EPC2016C - 917-1080-2. All samples were packaged in the standard 81 Ld BGA package (PKG Code VLB). Samples were processed through the standard burn-in cycle before irradiation.

1.5 Downpoints

Downpoints for the tests were 0, 10, 30, 50, 75, and 100krad(Si), followed by a 168-hour high temperature anneal at 100°C under bias, as described in the Experimental Matrix section.

2. Test Results

2.1 Attributes Data

Total dose testing of the ISL73033SLHM is complete. All tested parameters passed the datasheet limits. Table 2 summarizes the results.

Table 2. ISL73033SLHM Total Dose Test Attributes Data

Dose Rate (rad(Si)/s)	Condition	Sample Size	Downpoint	Pass (Note 1)	Fail
0.01	Biased (Figure 3)	24	Pre-irradiation	24	
			10krad(Si)	24	0
			30krad(Si)	24	0
			50krad(Si)	24	0
			75krad(Si)	24	0
			100krad(Si)	24	0
			Anneal	24	0
0.01	GND	24	Pre-irradiation	24	
			10krad(Si)	24	0
			30krad(Si)	24	0
			50krad(Si)	24	0
			75krad(Si)	24	0
			100krad(Si)	24	0
			Anneal	24	0

Note:
1. Pass indicates a sample that passes all post-irradiation datasheet limits.

2.2 Key Parameter Variables Data

The plots in Figure 4 through Figure 22 illustrate the TID response of selected parameters as shown in Table 3. The plots show the average tested values of the key parameters as a function of total dose for both conditions, biased and grounded, and Post Anneal (PA). The plots also include error bars at each downpoint, representing the minimum and maximum measured values of the samples, although in some plots the error bars are not visible because of their values compared to the scale of the graph.

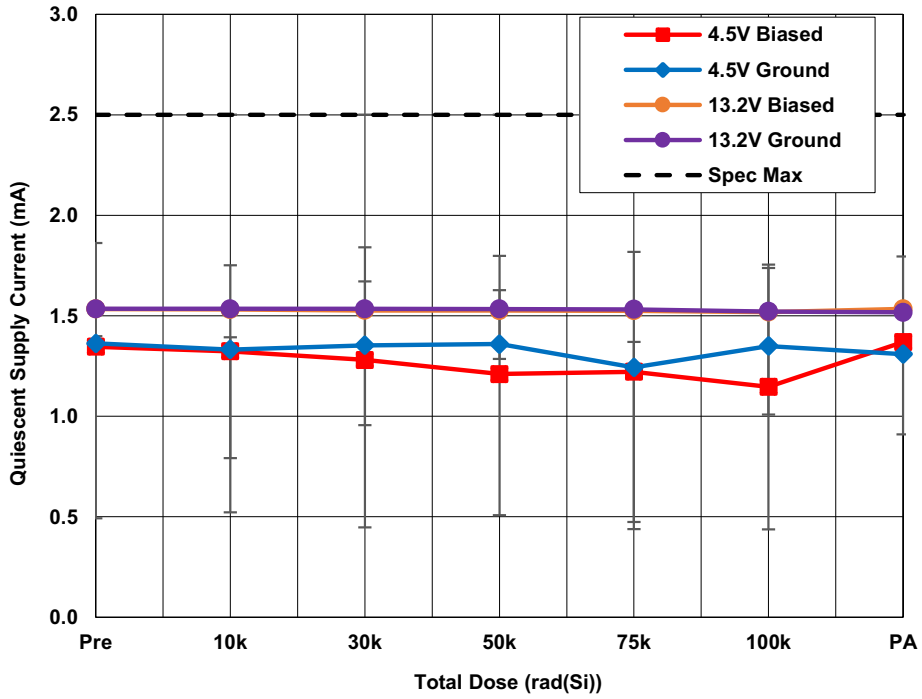

Figure 4. ISL73033SLHM average quiescent supply current (I_{DDQ}) with V_{DD} = 4.5V and 13.2V as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 2.5mA maximum.

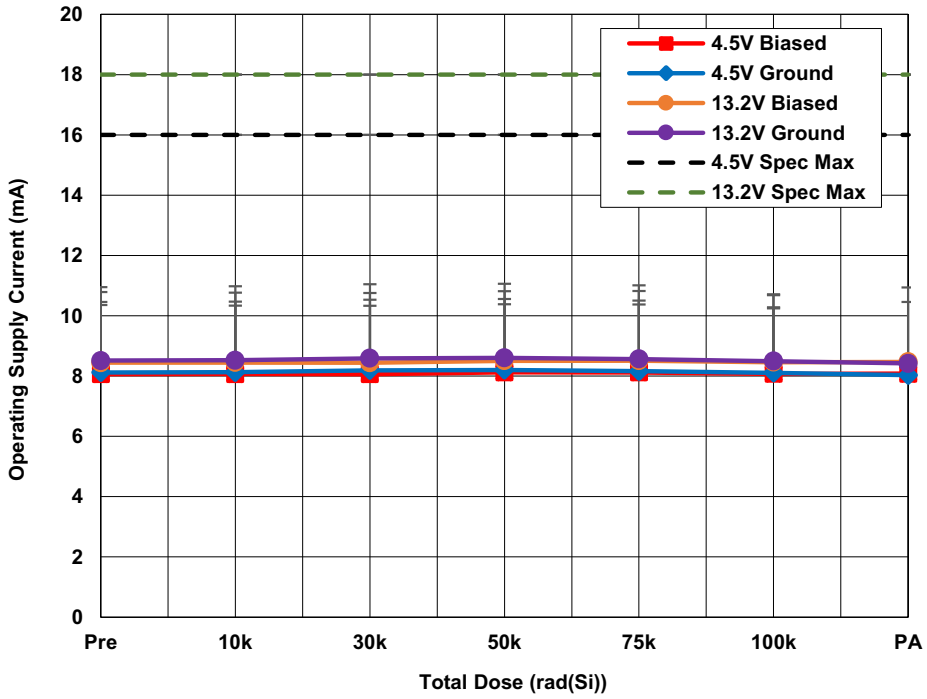

Figure 5. ISL73033SLHM average operating supply current (I_{DDO}) with V_{DD} = 4.5V and 13.2V as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limits are 16mA maximum for 4.5V and 18mA maximum for 13.2V.

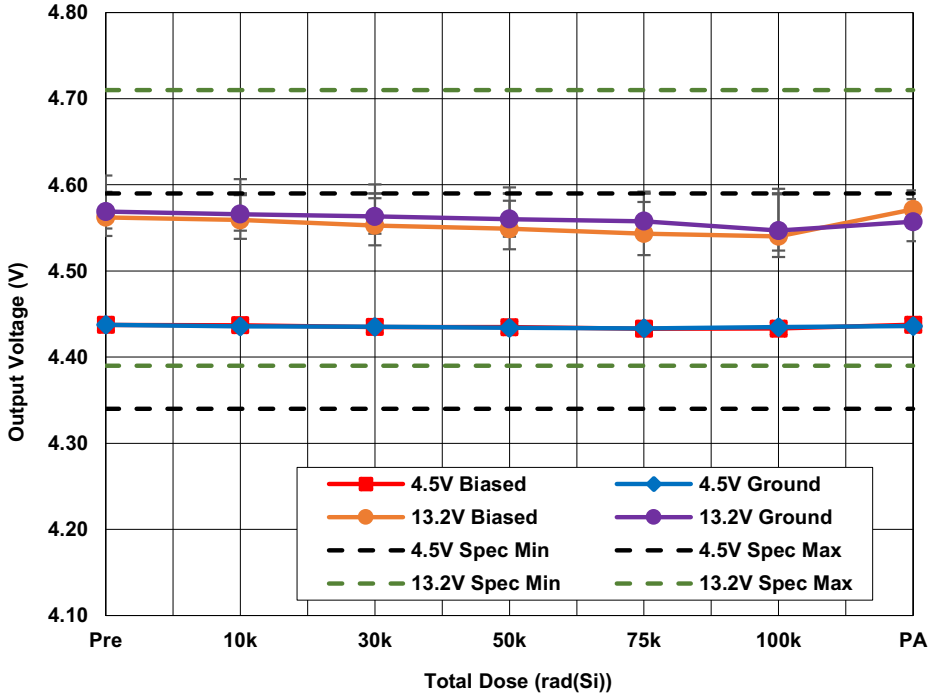

Figure 6. ISL73033SLHM average output voltage (V_{DRV}) with V_{DD} = 4.5V and 13.2V as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limits are 4.34V minimum and 4.59V maximum for 4.5V and 4.39V minimum and 4.71V maximum for 13.2V.

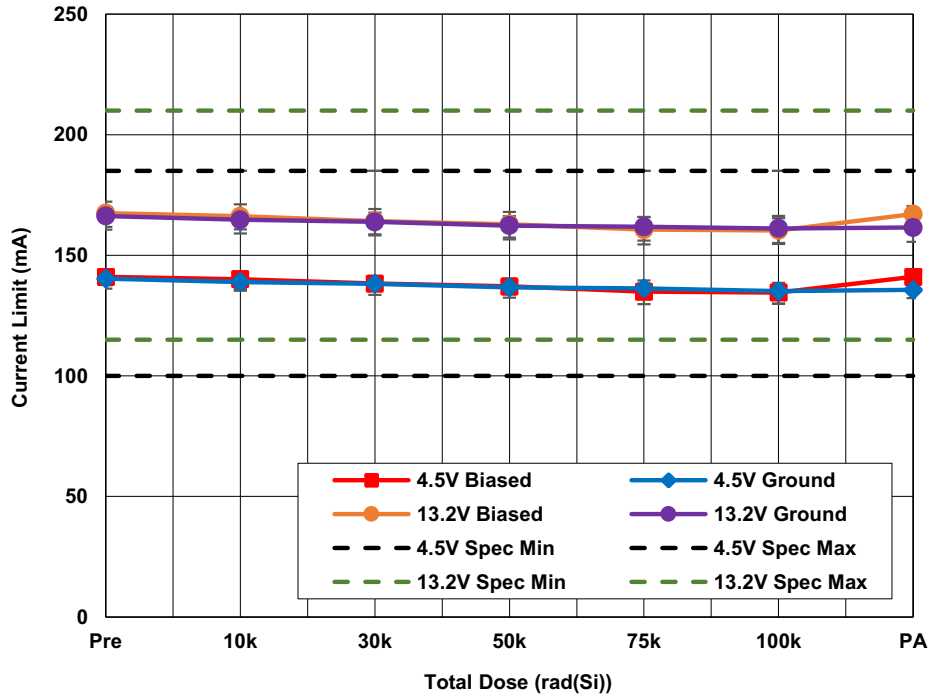

Figure 7. ISL73033SLHM average output current limit (I_{LIM}) with V_{DD} = 4.5V and 13.2V as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limits are 100mA minimum and 185mA maximum for 4.5V and 115mA minimum and 210mA maximum for 13.2V.

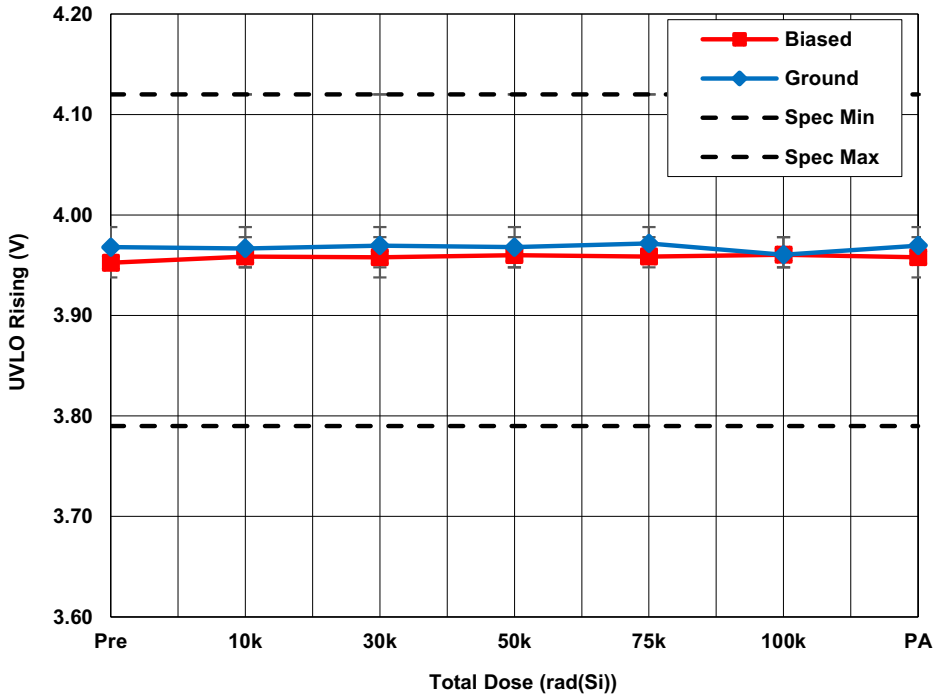

Figure 8. ISL73033SLHM average UVLO rising threshold on V_{DRV} (V_{RDRV}) with V_{DD} = 4.5V as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limits are 3.79V minimum and 4.12V maximum.

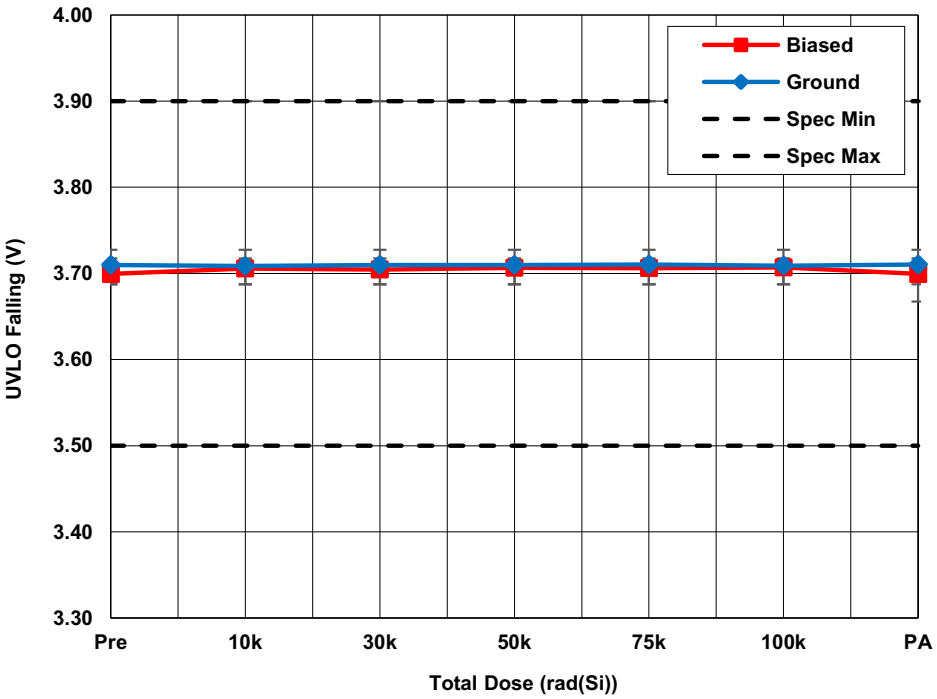

Figure 9. ISL73033SLHM average UVLO falling threshold on V_{DRV} (V_{FDRV}) with V_{DD} = 4.5V as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limits are 3.50V minimum and 3.9V maximum.

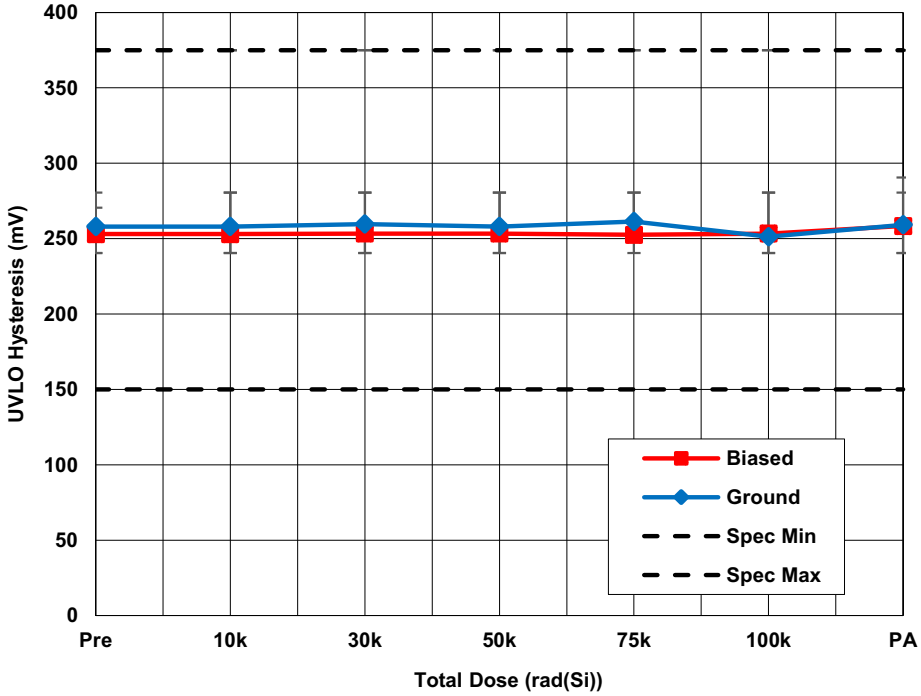

Figure 10. ISL73033SLHM average UVLO hysteresis on V_{DRV} (V_{HDRV}) with V_{DD} = 4.5V as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limits are 150mV minimum and 375mV maximum.

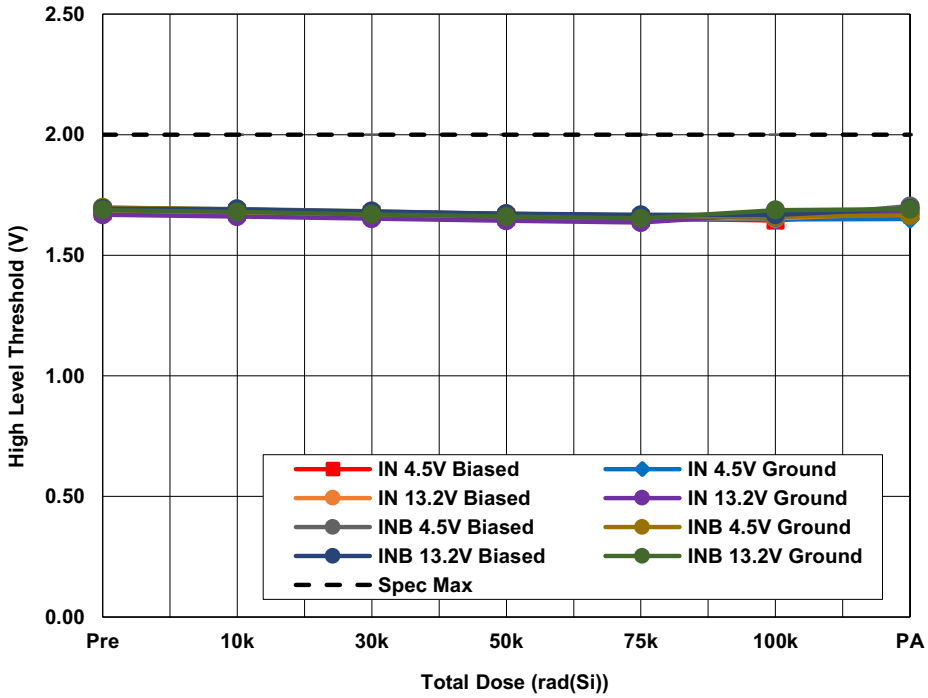

Figure 11. ISL73033SLHM average high level threshold (V_{IH}) with V_{DD} = 4.5V and 13.2V as a function of LDR irradiation and anneal. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is 2V maximum.

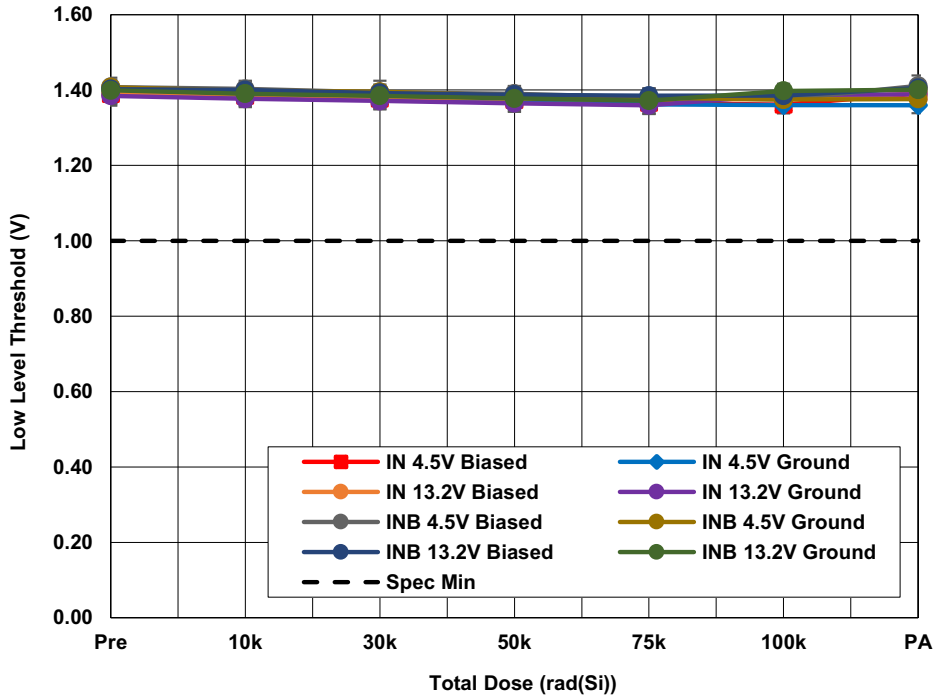

Figure 12. ISL73033SLHM average low level threshold (V_{IL}) with V_{DD} = 4.5V and 13.2V as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 1V minimum.

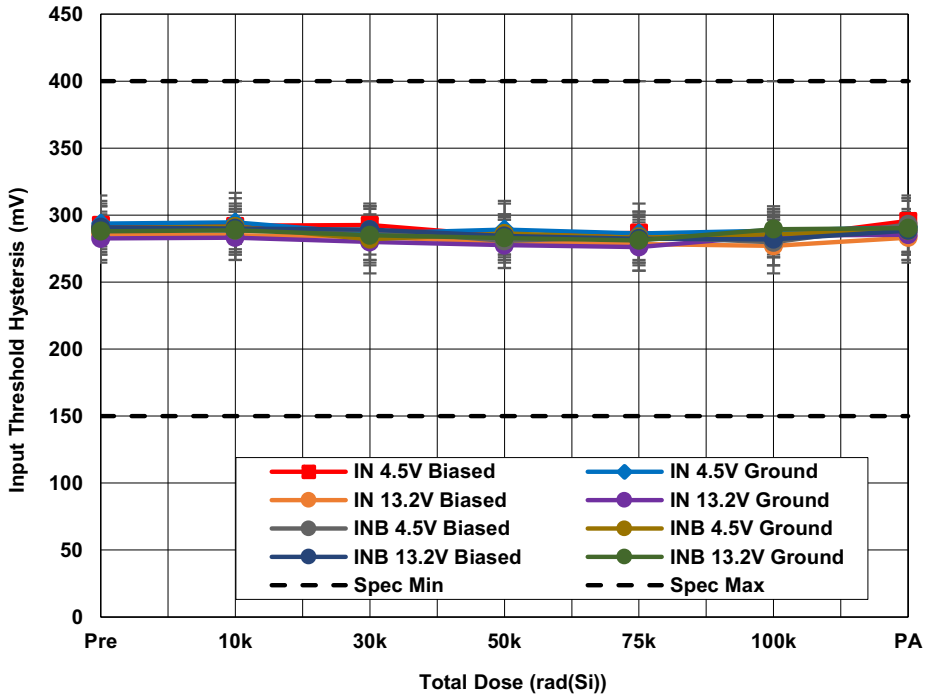

Figure 13. ISL73033SLHM average input hysteresis (V_{IHYS}) with V_{DD} = 4.5V and 13.2V as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheets limits are 150mV minimum and 400mV maximum.

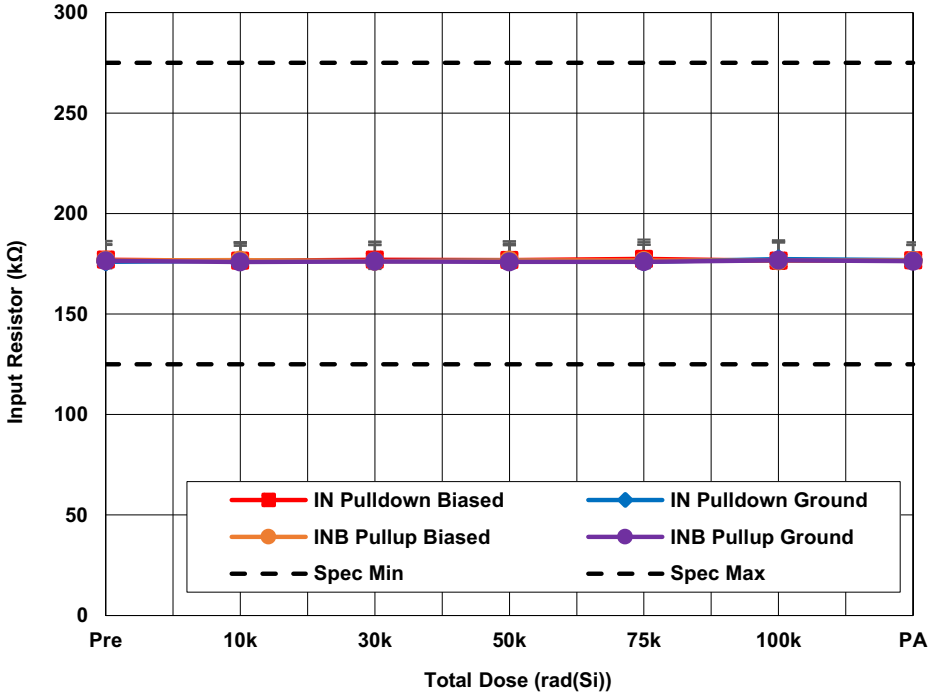

Figure 14. ISL73033SLHM average pull-up/pull-down resistance ($R_{INU/D}$) with IN to V_{SS} and INB to V_{DD} as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limits are 125kΩ minimum and 275kΩ maximum.

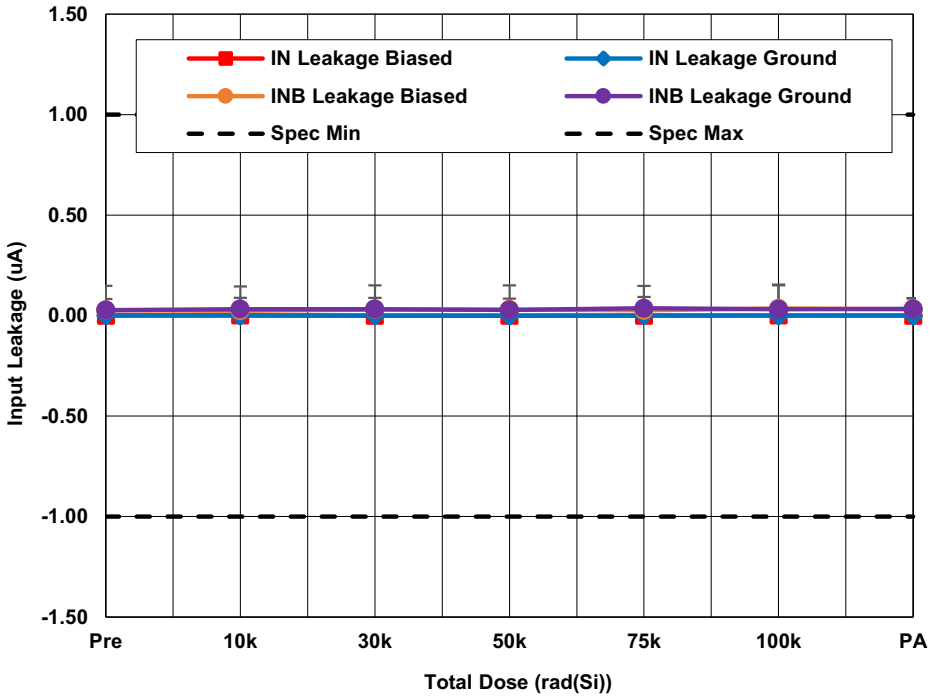

Figure 15. ISL73033SLHM average input leakage current ($I_{IN/INB}$) as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limits are -1µA minimum and 1µA maximum.

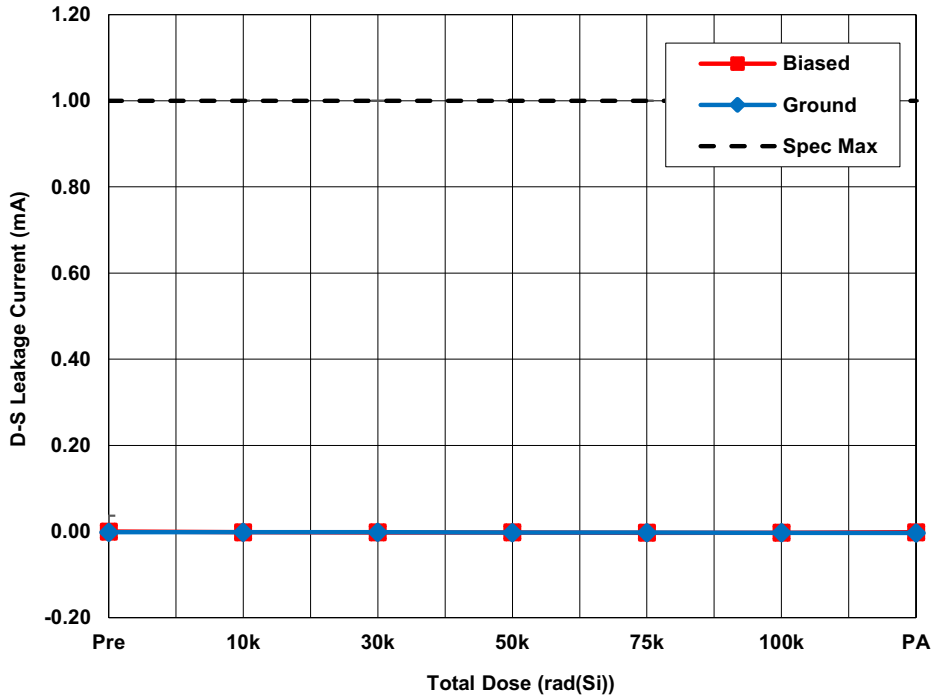

Figure 16. ISL73033SLHM average drain to source leakage current (I_{DSS}) with V_{IN} = 0V, V_{INB} = 0V, V_{DS} = 80V and V_{GS} = 0V as a function of LDR irradiation and anneal. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is 1mA maximum.

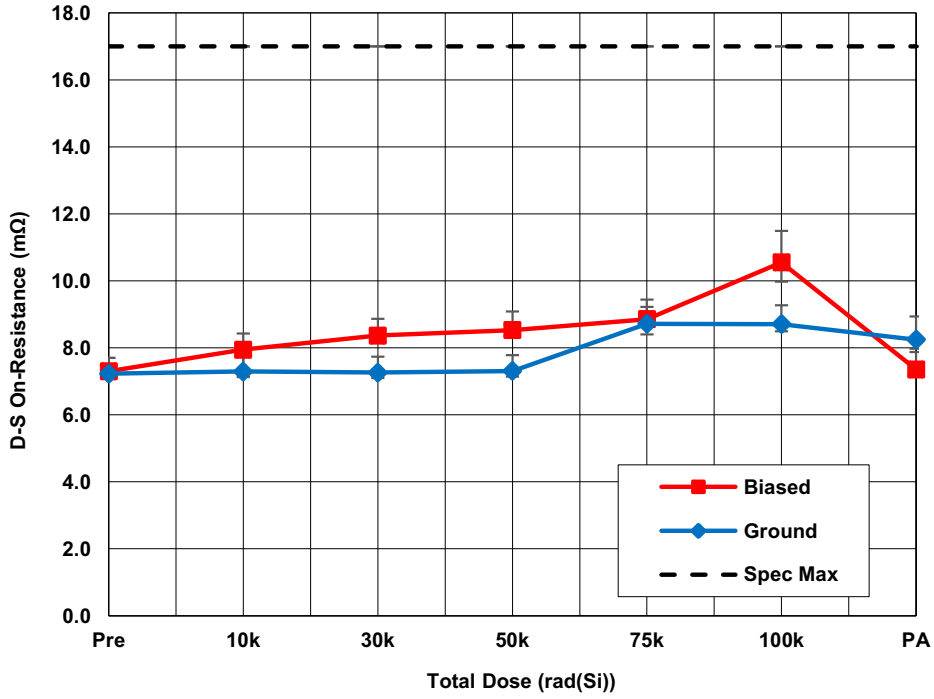

Figure 17. ISL73033SLHM average drain to source on resistance ($r_{ds(on)}$) with V_{IN} = 5V, V_{INB} = 0V and I_D = 25A as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 17mΩ maximum.

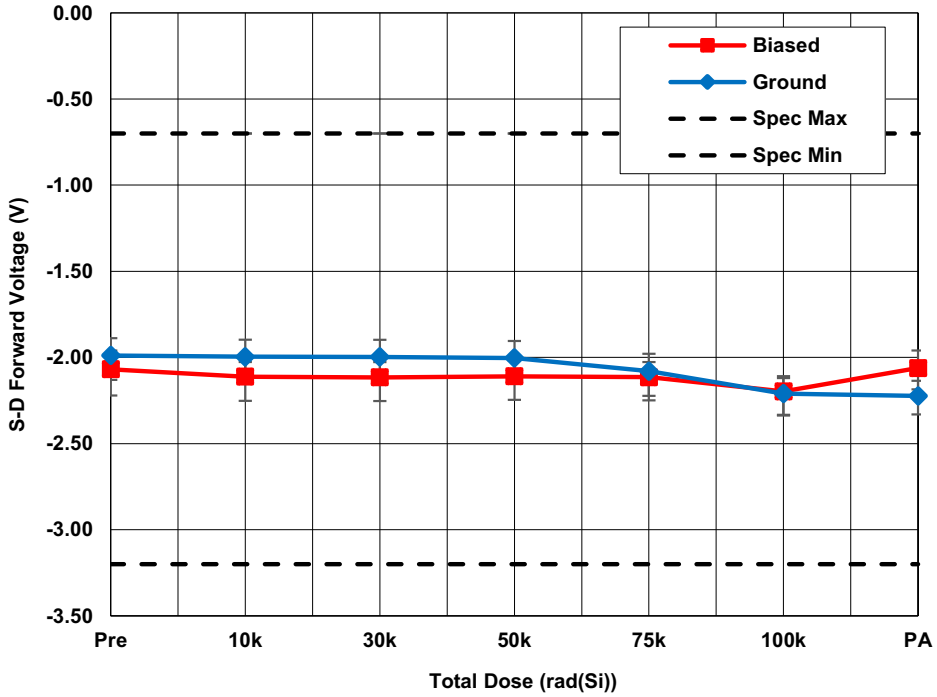

Figure 18. ISL73033SLHM average source to drain forward voltage (V_{SD}) with V_{IN} = 0V, V_{INB} = 0V and I_S = 0.5A as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limits are -3.2V minimum and -0.7V maximum.

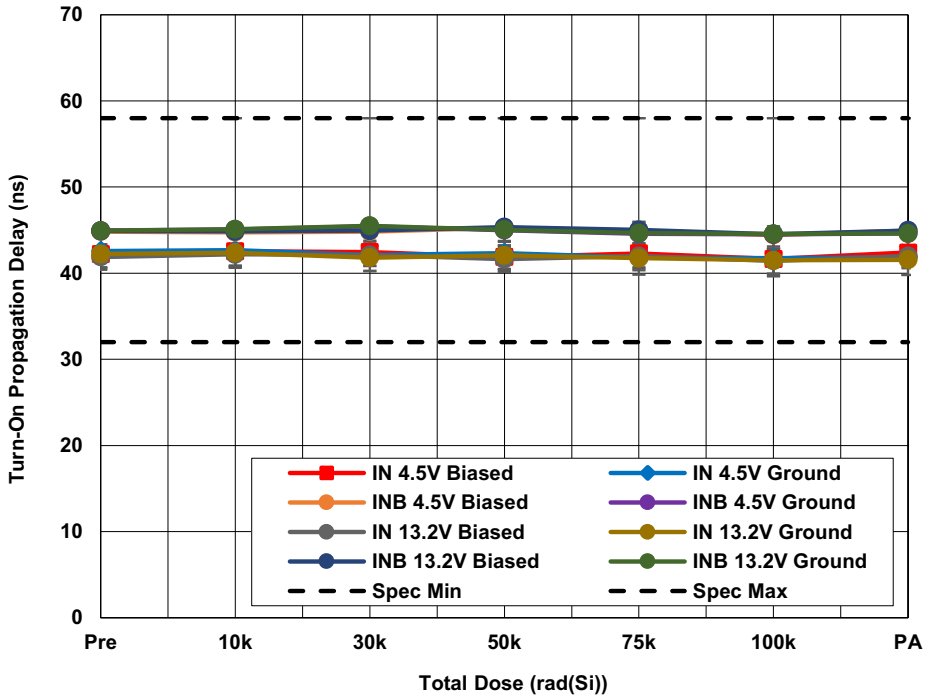

Figure 19. ISL73033SLHM average turn on propagation delay (t_{ON}) with V_{DD} = 4.5V and 13.2V as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limits are 32ns minimum and 58ns maximum.

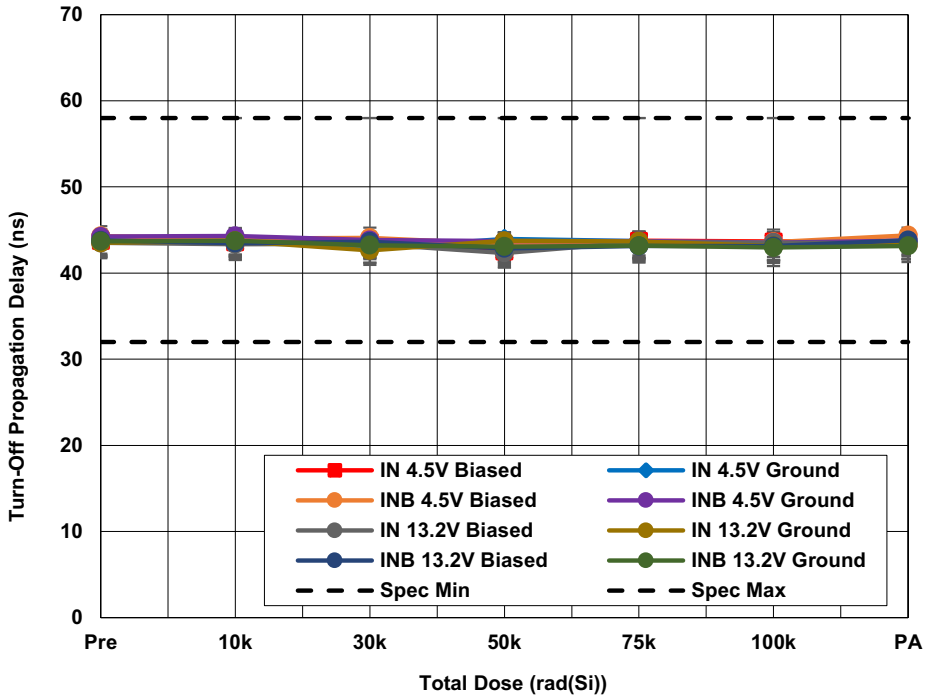

Figure 20. ISL73033SLHM average turn off propagation delay (t_{OFF}) with V_{DD} = 4.5V and 13.2V as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limits are 32ns minimum and 58ns maximum.

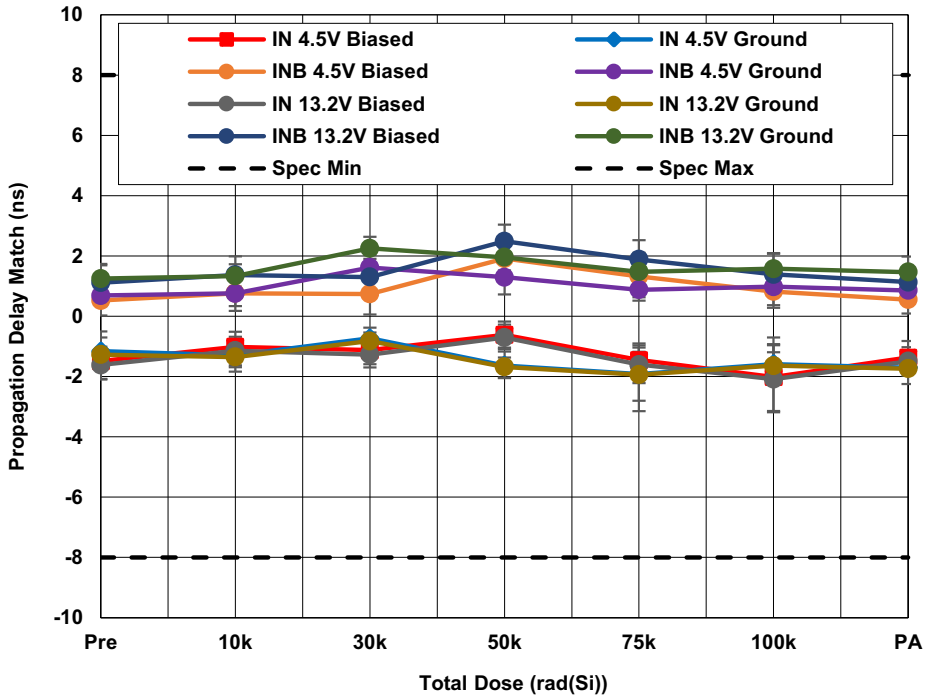

Figure 21. ISL73033SLHM average propagation delay matching (t_{DM}) with V_{DD} = 4.5V and 13.2V as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limits are -8ns minimum and 8ns maximum.

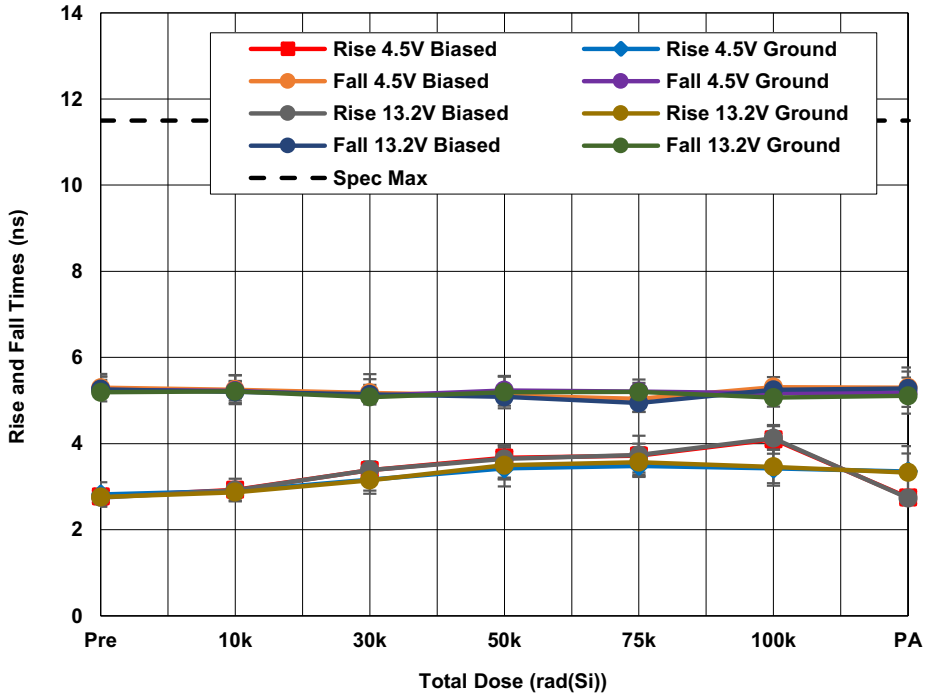

Figure 22. ISL73033SLHM average rise and fall times (t_{RISE}, t_{FALL}) with V_{DD} = 4.5V and 13.2V as a function of LDR irradiation and anneal. The error bars represent the minimum and maximum measured values. The datasheet limit is 11.5ns maximum.

3. Discussion and Conclusion

The results of a LDR total dose test of the ISL73033SLHM radiation hardened Dri-GaN power stage with a 100V enhancement mode Gallium Nitride (GaN) FET are reported. The irradiation of biased and grounded samples to 100krad(Si) was followed by a 168-hour anneal at 100°C under bias. All datasheet parameters passed at all downpoints. No evidence of bias dependence was observed.

4. Appendices

4.1 Reported parameters

Table 3 lists the key parameters that are considered indicative of part performance. These parameters are plotted in Figure 4 through Figure 22. All limits are taken from the ISL73033SLHM datasheet.

Table 3. ISL73033SLHM Key Total Dose Parameters (T_A = 25°C)

Figure	Parameter	Symbol	Conditions	Limit (Low)	Limit (High)	Unit
4	Quiescent Supply Current	I_{DDQ}	V_{IN} = 4.5V, 13.2V	-	2.5	mA
5	Operating Supply Current	I_{DDO}	V_{IN} = 4.5V, f_{PWM} = 500kHz	-	16	mA
			V_{IN} = 13.2V, f_{PWM} = 500kHz	-	18	
6	Output Voltage	V_{DRV}	V_{IN} = 4.5V	4.34	4.59	mA
			V_{IN} = 13.2V	4.39	4.71	
7	Current Limit of V_{DRV}	I_{LIM}	V_{IN} = 4.5V	100	185	mA
			V_{IN} = 13.2V	115	210	
8	UVLO Rising Threshold	V_{RDRV}	V_{IN} = 4.5V	3.79	4.12	V
9	UVLO Falling Threshold	V_{FDRV}	V_{IN} = 4.5V	3.50	3.90	V
10	UVLO Threshold Hysteresis	V_{HDRV}	V_{IN} = 4.5V	150	375	mV
11	High Level Threshold	V_{IH}		-	2	V
12	Low Level Threshold	V_{IL}		1	-	V
13	Input Threshold Hysteresis	Vihys	V_{IN} = 4.5V, 13.2V	150	400	mV
14	Input Pull-Up/Pull-Down Resistor	$R_{INU/D}$	IN to V_{SS} and INB to V_{DD}	125	275	kΩ
15	Input Leakage Current	$I_{IN/INB}$		-1	1	µA
16	Drain to Source Leakage Current	I_{DSS}	V_{IN} = 0V, V_{INB} = 0V, V_{DS} = 80V, V_{GS} = 0V	-	1.1	mA
17	Drain to Source On-Resistance	$r_{DS(ON)}$		-	17	mΩ
18	Source to Drain Forward Voltage	V_{SD}	V_{IN} = 0V, IS = 0.5A	-3.2	-0.7	V
19	Turn-ON Propagation Delay	t_{ON}	V_{IN} = 4.5V, 13.2V; I_D = 12.5A	32	58	ns
20	Turn-OFF Propagation Delay	t_{OFF}	V_{IN} = 4.5V, 13.2V; I_D = 12.5A	32	58	ns
21	Propagation Delay Matching	t_{DM}	V_{IN} = 4.5V, 13.2V	-8	8	ns
22	Rise Time (10% to 90%)	t_{RISE}	V_{IN} = 4.5V, 13.2V	-	11.5	ns
	Fall Time (90% to 10%)	t_{FALL}				

5. Revision History

Rev.	Date	Description
2.0	May 12, 2021	Updated File number to the Renesas formatting. Updated part number from ISL73033SLH to ISL73033SLHM throughout.
1.0	Dec 17, 2020	Initial release

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(Rev.1.0 Mar 2020)

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