ISL73041SEH, ISL71441SLH

Single Event Effects (SEE) Testing of the ISL73041SEH, ISL71441SLH 12V Half Bridge GaN FET Drivers

Introduction

The intense proton and heavy-ion environment encountered in space applications can cause a variety of Single Event Effects (SEE) in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Latch-Up (SEL), Single Event Gate Rupture (SEGR), and Single Event Burnout (SEB). SEE can lead to system-level performance issues including disruption, degradation, and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. This report discusses the results of the SEE testing performed on the ISL73041SEH product. Since SEE testing is performed with the devices under test decapsulated, the results of this report also apply to the ISL71441SLH as the only difference between the parts are that the ISL73041SEH has a ceramic package and the ISL71441SLH has a plastic package.

SEE Summary

Normal incidence praseodymium with a LET of 67.5MeV•cm^2/mg and a range to Bragg peak of 25µm in silicon at the surface of the device was used for SEE testing. The LET of the ions ranged from 69.5MeV•cm^2/mg to 70.5MeV•cm^2/mg in the active silicon layer.

The ISL73041SEH proved to be free of Destructive Single Event Effects (DSEE) including SEL with VDD = 20V, PVIN = 16.5V, and PVCC = AVCC = 6.3V at a die temperature of 125°C.

A SEFI was defined as an event in which FLTb pulled low. No SEFIs were observed during DSEE testing.

The ISL73041SEH was tested for two types of SETs over four test conditions (TCs) at a die temperature of 25°C. The first type of SET was an event that caused shoot-through, which is when the upper and lower gate drivers are on at the same time. The driver experienced zero shoot-through SETs when VDD = VPIN = 13.2V. The worst-case cross section for shoot-through is 2.5E-8cm^2, the reciprocal of the fluence.

The second type of SET was an event in which the PHS pulse width deviated beyond ±65ns from the average PHS pulse width before turning on the beam. Some of these deviations were extreme enough to constitute a complete missing pulse event and were analyzed separately. The largest cross section for a PHS pulse width deviation events was 8.3E-6cm^2. The largest deviation from the average PHS pulse width was 1362ns and the maximum number of subsequent PHS pulses until pulse width deviations were within ±65ns from the average pulse width was ten PHS pulses. The largest cross section for a missing pulse event was 1.8E-7cm^2. The maximum number of pulses missed in an event was two pulses, and the maximum number of subsequent PHS pulses until pulse width deviations were within ±65ns from the average pulse width was five PHS pulses.

Additional SEE testing was performed with normal incidence gold with a LET of 86.3MeV•cm^2/mg and a range to Bragg peak of 51µm in silicon at the surface of the device. The LET of the ions ranged from 88.4MeV•cm^2/mg to 90.2MeV•cm^2/mg in the active silicon layer.

The ISL73041SEH did not experience any DSEE with VDD = 20V, PVIN = 13.5V, PVCC = 6.5V, and AVCC = 6.3V at a die temperature of 125°C.

No SEFIs were observed during DSEE testing.

The ISL73041SEH did not experience any shoot-through SETs, so the worst-case cross section for shoot-through is 2.5E-8cm^2.

The largest cross section for a PHS pulse width deviation event was 5.6E-5cm^2. The largest deviation from the average PHS pulse width was 517ns. The maximum number of subsequent PHS pulses until pulse width deviations were within ±65ns from the average pulse width was eleven PHS pulses. The largest cross section for

a missing pulse event was 2.1E-6cm^2. The maximum number of pulses missed in an event was two pulses. The maximum number of subsequent PHS pulses until pulse width deviations were within ±65ns from the average pulse width was one PHS pulse. Since SEE testing is performed with the devices under test decapsulated, the results of this report also apply to the ISL71441SLH as the only difference between the parts are that the ISL73041SEH has a ceramic package and the ISL71441SLH has a plastic package.

Product Description

The ISL73041SEH is a radiation hardened PWM input 12V half bridge GaN FET driver designed to drive low $r_{DS(ON)}$, enhance mode Gallium Nitride (eGaN) FETs for DC/DC switching regulators. An integrated programmable GaN FET gate drive voltage, high-side bootstrap switch and high gate drive current provides a compact and robust GaN FET half bridge driver.

The ISL73041SEH interfaces directly to the ISL73847SEH dual phase PWM buck controller to create a high efficiency point-of-load regulator to power many of the latest low voltage high current FPGA and DSP digital core rails.

The ISL73041SEH operates across the military temperature range from -55°C to +125°C and is available in a 16 lead Ceramic Leadless Chip Carrier (CLCC) package.

The ISL73041SEH is offered with radiation assurance screening to 75krad(Si) at 10mrad(Si)/s.

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1. SEE Testing

1.1 Objective

The testing was intended to find the limits on the voltages of VDD, PVIN, AVCC, and PVCC set by the onset of DSEE at a LET of 67.5MeV•cm^2/mg (normal incidence praseodymium) and at a LET of 86.3MeV•cm^2/mg (normal incidence gold). The device was also monitored for SEFIs during DSEE studies. Additional testing was intended to identify and quantify SETs occurring during the operation of the ISL73041SEH. For SET studies, the driver was monitored for shoot-through and pulse width deviation events and was irradiated with normal incidence praseodymium (LET = 67.5MeV•cm^2/mg) and normal incidence gold (LET = 86.3MeV•cm^2/mg).

1.2 Facility

SEE testing was completed at the Texas A&M University (TAMU) Radiation Effects Facility of the Cyclotron Institute in College Station, Texas. This facility is coupled to a K500 superconducting cyclotron that can supply a wide range of ion species and flux. The SEE testing in this report was performed on November 4 and 5, 2022. At the time of testing, gold ions were unavailable at the facility. The highest LET beam available was praseodymium with a LET of 67.5MeV•cm^2/mg and a range to the Bragg peak of 25µm in silicon.

Additional testing was performed on April 13 and 14, 2023, with normal incidence gold ions for a LET of 86.3MeV•cm^2/mg and a range to the Bragg peak of 51µm in silicon.

1.3 Setup

The test boards used for ISL73041SEH SEE testing were configured so that two devices could be irradiated at the same time. The ISL73041SEH was evaluated for SEE using a general-purpose engineering evaluation board configured in half-bridge configuration. Specific configurations were imposed for different types of SEE testing. For DSEE testing on VDD and AVCC/PVCC, the half-bridge drove a 1µH/660µF LC output filter which represented a typical DC-DC converter application. For DSEE testing of PVIN and for SET testing, as it was critical to know the exact voltage or pulse width on the PHS pin, a 500kΩ load from PHS to GND was used to synchronously control the PHS voltage and pulse width through the upper and lower GaN FET.

The PWM switching frequency of 500kHz was chosen to match a typical application when used in conjunction with the ISL73847SEH PWM Controller. The 25%PWM duty cycle was chosen as it is a good low duty cycle for the PWM controller with which the driver is intended to operate, but it is not so low such that SETs on a PHS pulse width may have been indiscernible.

For SET testing, the PWM input levels switched between 1.0V and 2.8V for logic level low and high; the VDD and PVIN were tested at 4.75V and 13.2V; the output capacitors for the internal AVCC and PVCC LDO were derated down to 0.68µF from their 1.0µF minimum recommended value (-32% shift); the dead-time control setting on RDU and RDL were set at GND (minimum dead time) or 10kΩ (maximum dead-time). These settings were chosen to set the ISL73041SEH into its operational limits to determine its sensitivities to half-bridge shoot-through and PHS pulse width deviation SETs due to a heavy ion strike.

The schematics for the DSEE and the SET test boards are depicted in Figure 1 and Figure 2.

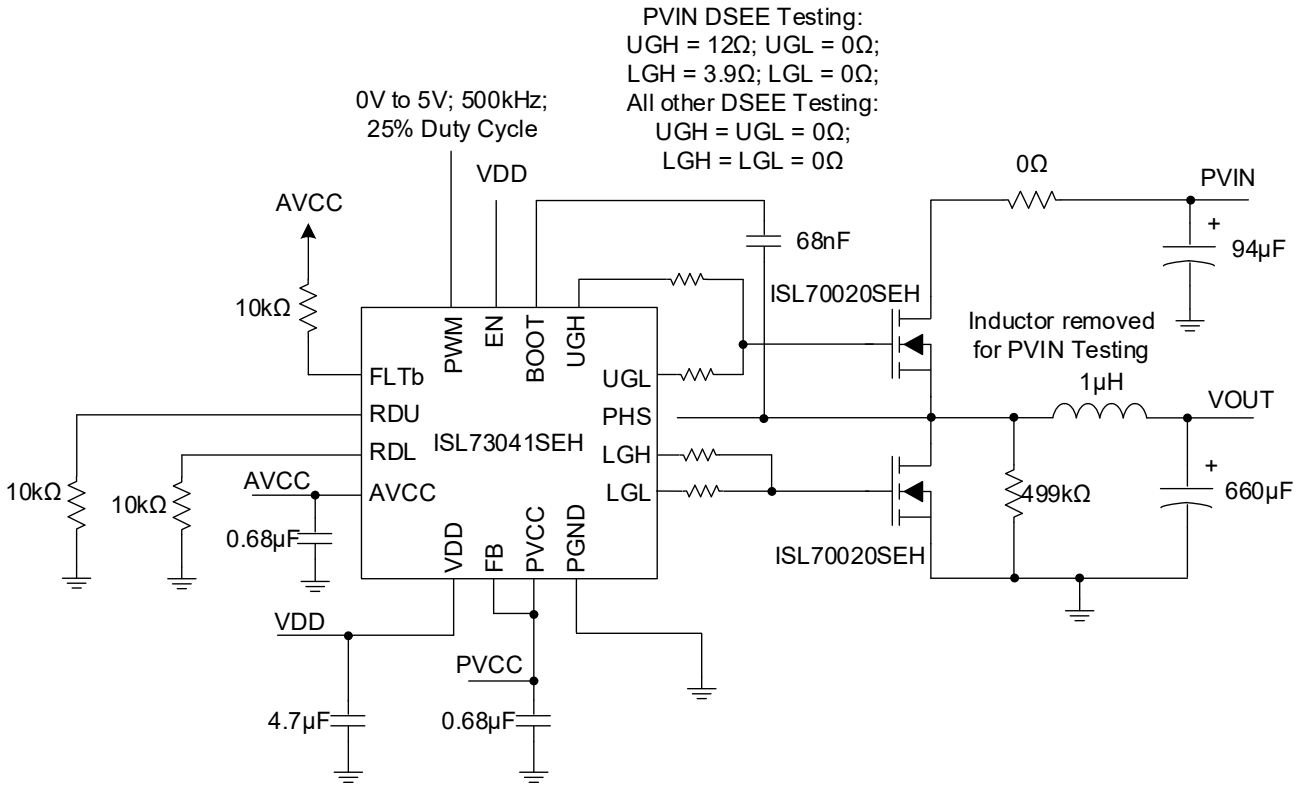

Figure 1. ISL73041SEH DSEE Test Board Schematic

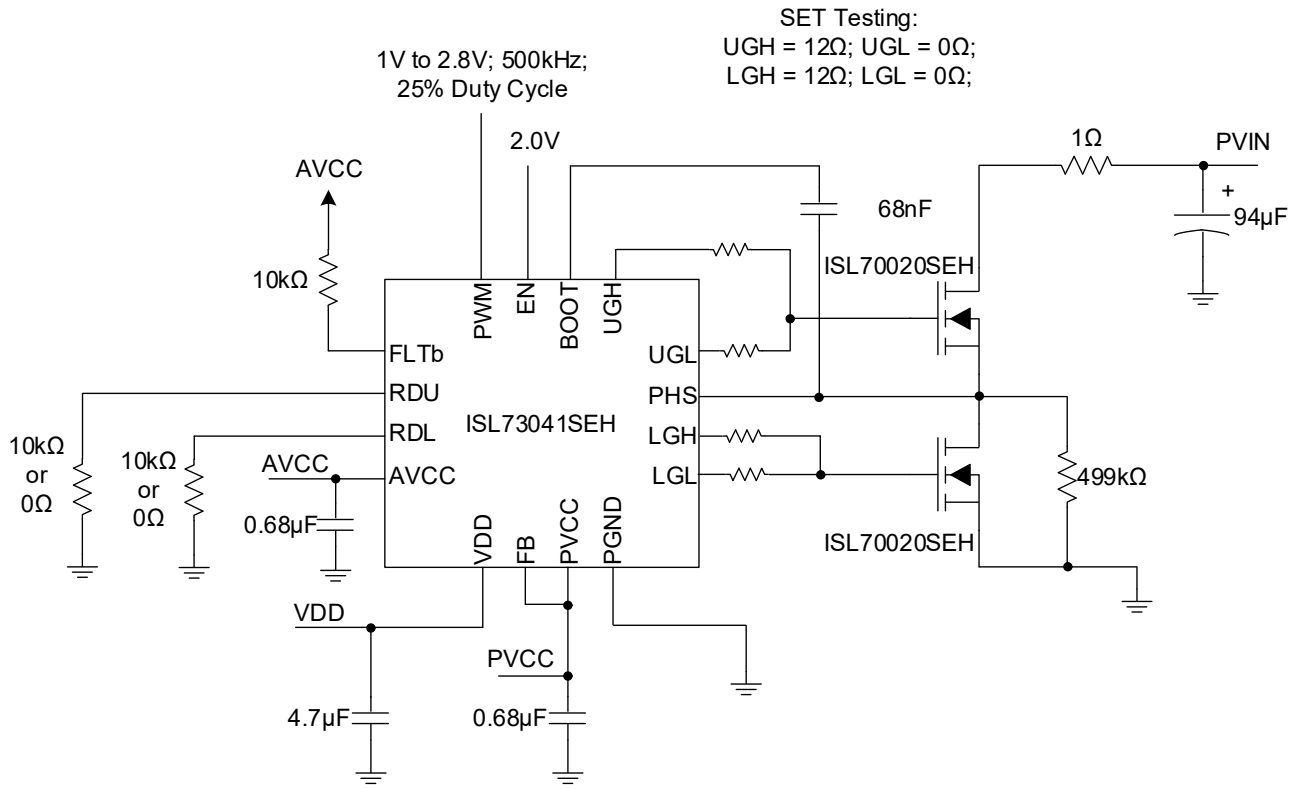

Figure 2. ISL73041SEH SET Test Board Schematic

Table 1. Monitored Parameters and Failure Criteria for the ISL73041SEH DSEE Testing

Parameter Monitored	Failure Criteria
Buck V_{OUT} Voltage with I_{OUT} = 0A (V_{OUT})	±2%
Supply Current on VDD (I_{VDD})	±20%
Supply Current on PVCC (I_{PVCC})	±20%
Supply Current on AVCC (I_{AVCC})	±20%

DSEE testing consisted of three components. For all three components, the ISL73041SEH was made to drive ISL70020SEH GaN FETs. Additionally, for all DSEE testing:

- EN was set to VDD.
- PWM modulated between 0V and 5V at a switching frequency of 500kHz and a 25% duty cycle.
- FLTb was connected to AVCC using a 10kΩ resistor.
- FB was set to PVCC.
- The die temperature was 125°C.

The purpose of the first component was to find the maximal value of the voltage on VDD set by the onset of DSEE. For this component, PVIN was set to 12V, and AVCC and PVCC were set to 5.0V and 4.5V respectively by the internal LDO. VDD was initially set to 16V and VDD was incremented by 1V for each run. Testing ended when the device underwent a DSEE or until VDD reached 20V, which is the maximum voltage on VDD allowed by the process. The supply current on the VDD pin was monitored to determine if the device underwent a DSEE.

The purpose of the second component was to find the maximal value of the voltage on PVIN set by the onset of DSEE. For this component, VDD was set to 12V, AVCC was set to 5V by the internal LDO, and PVCC was externally biased to 5V. PVIN was initially set to 13.5V and was incremented by 1V for each run. Testing ended when the device underwent a DSEE or until PVIN reached 17.5V. The supply currents on the VDD and PVCC pins were monitored to determine if the device underwent a DSEE.

The purpose of the third component was to find the maximal values of the voltages on AVCC and PVCC set by the onset of DSEE. For this component, VDD was set to 12V, and PVIN was set to 12V. AVCC and PVCC were initially set to 5.7V and AVCC and PVCC were incremented by 0.2V for each run. Testing ended when the device underwent a DSEE or until AVCC and PVCC reached 6.3V. The supply currents on VDD, AVCC, and PVCC and the buck VOUT voltage with I_{OUT} = 0A were monitored to determine if the device underwent a DSEE.

The DUT was considered to undergo a DSEE when one of its monitored parameters exceeded the failure criteria listed in Table 1.

A SEFI was defined as an event in which FLTb pulled low. The DUTs were monitored for SEFIs during DSEE testing.

During SET testing, the device was monitored for two different types of SETs over the four test conditions listed in Table 2. The first type of SET was an event that caused shoot-through, which is when the upper and lower gate drivers are on at the same time. To capture a shoot-through SET, a 1Ω resistor was inserted between the drain of the high-side GaN FET and the PVIN bus voltage. During a shoot-through event, both GaN FETs turn on, pulling the drain side of the resistor toward 0V while the PVIN side is held up by the input capacitance. The drain side of this 1Ω resistor was used to monitor for a shoot-through condition.The second type of SET was a PHS pulse width deviation event. A PHS pulse width deviation SET was defined as an event that caused a pulse width deviation of PHS from the average pre-beam PHS operating pulse width beyond ±65ns for a switching frequency of 500kHz and a 25% duty cycle operation. The pulse width deviation of ±65ns was chosen because it represents a 50% delta of 135ns, which is the minimum on-time for the ISL73847SEH controller with which the ISL73041SEH is designed to operate. Some PHS pulse width deviations were extreme enough that a LG or UG-PHS pulse was completely missed. These events were considered to be missing pulse events and were analyzed separately. For SET testing, the die temperature was 25°C. Testing for PHS pulse width deviation events was performed simultaneously to the testing for shoot-through events as the test conditions and setup were the same.

For pulse width deviation events, the trigger was set to capture events in which the PHS pulse deviated by ±65ns from the operating pulse width of the driver before the beam was turned on. For shoot-through events, the trigger was set to capture events in which VSENSE decreased by 5V. PVIN was set to the same voltage VDD, so when VDD was 4.75V, VSENSE could not decrease by 5V. Therefore, there is only shoot-through data for TC #3 and TC #4 when VDD = VPIN = 13.2V for testing with normal incidence praseodymium. This issue was corrected for testing with normal incidence gold such that the trigger was set to capture events in which VSENSE decreased by 2.4V when VDD = VPIN = 4.75V.

Table 2. ISL73041SEH Shoot-Through and Pulse Width Deviation SET Test Conditions

Test Condition	Number of Devices Tested	RDU Resistor (kΩ)	RDL Resistor (kΩ)	VDD (V)	PVIN (V)
#1	4	10	10	4.75	4.75
#2	4	GND	GND	4.75	4.75
#3	4	10	10	13.2	13.2
#4	4	GND	GND	13.2	13.2

2. Results

2.1 LET = 67.5MeV•cm^2/mg

2.1.1 DSEE Results

The results of VDD DSEE testing are displayed in Table 3. No devices experienced DSEE while under beam, therefore testing indicates that the device should be operated with a maximal value of VDD = 20V to be robust against DSEE.

Table 3. ISL73041SEH VDD DSEE Test Results For LET = 67.5MeV•cm^2/mg

VDD (V)	DUT #	Result	I_{VDD} (±20%)		
			Pre (mA)	Post (mA)	Δ (%)
16.0	17	Pass	33.18	33.12	-0.18
	18	Pass	32.96	32.85	-0.33
	19	Pass	33.30	33.30	0.00
	20	Pass	33.23	33.28	0.14
17.0	17	Pass	33.12	33.14	0.06
	18	Pass	32.85	32.91	0.18
	19	Pass	33.30	33.21	-0.26
	20	Pass	33.27	33.29	0.05
18.0	17	Pass	33.14	33.11	-0.09
	18	Pass	32.91	32.91	0.00
	19	Pass	33.21	33.22	0.03
	20	Pass	33.29	33.33	0.14
19.0	17	Pass	33.07	33.09	-0.12
	18	Pass	32.91	32.97	0.18
	19	Pass	33.22	33.24	0.06
	20	Pass	33.33	33.28	-0.15

Table 3. ISL73041SEH VDD DSEE Test Results For LET = 67.5MeV•cm²/mg

VDD (V)	DUT #	Result	I_{VDD} (±20%)		
			Pre (mA)	Post (mA)	Δ (%)
20.0	17	Pass	33.07	33.09	0.06
	18	Pass	32.97	32.94	-0.09
	19	Pass	33.24	33.27	0.09
	20	Pass	33.29	33.25	-0.12

The results of PVIN DSEE testing are displayed in Table 4. DUT 3 experienced a DSEE when PVIN = 17.5V, therefore testing indicates that the device should be operated with a maximal value of PVIN = 16.5V to be robust against DSEE.

Table 4. ISL73041SEH PVIN DSEE Test Results for LET = 67.5MeV•cm²/mg

PVIN (V)	DUT #	Result	I_{VDD} (±20%)			I_{PVCC} (±20%)		
			Pre (mA)	Post (mA)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)
13.5	1	Pass	3.888	3.880	-0.21	30.65	30.62	-0.10
	2	Pass	3.883	3.864	-0.49	30.91	30.88	-0.10
	3	Pass	3.890	3.904	0.36	31.11	31.04	-0.21
	4	Pass	3.900	4.003	2.64	29.78	29.78	0
14.5	1	Pass	3.879	3.873	-0.16	30.88	30.86	-0.06
	2	Pass	3.863	3.855	-0.21	31.12	31.11	-0.03
	3	Pass	3.904	3.896	-0.21	31.29	31.27	-0.06
	4	Pass	4.003	4.010	0.18	30.60	30.56	-0.13
15.5	1	Pass	3.872	3.872	0.00	31.12	31.13	0.03
	2	Pass	3.854	3.847	-0.18	31.36	31.35	-0.03
	3	Pass	3.896	3.903	0.18	31.51	31.50	-0.03
	4	Pass	4.008	4.010	0.050	30.88	30.78	-0.32
16.5	1	Pass	3.872	3.859	-0.34	31.37	31.35	-0.06
	2	Pass	3.856	3.870	0.36	31.59	31.58	-0.03
	3	Pass	3.903	3.892	-0.28	31.71	31.68	-0.09
	4	Pass	4.009	3.994	-0.374	31.00	30.98	-0.06
17.5	1	Pass	3.859	3.835	-0.62	31.97	31.90	-0.22
	2	Pass	3.870	3.866	-0.10	32.17	32.11	-0.19
	3	Fail	3.890	253.00	6403	32.54	533.00	1538
	4	Pass	3.994	3.984	-0.25	31.54	31.14	-1.27

The results of AVCC/PVCC DSEE testing are displayed in Table 5. No devices experienced DSEE while under beam, therefore testing indicates that the device should be operated with a maximal value of PVCC = AVCC = 6.3V to be robust against DSEE.

Table 5. ISL73041SEH AVCC/PVCC DSEE Test Results For LET = 67.5MeV·cm²/mg

AVCC/ PVCC (V)	DUT #	Result	V_{OUT} (±2%)			I_{VDD} (±20%)			I_{AVCC} (±20%)			I_{PVCC} (±20%)		
			Pre (V)	Post (V)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)
5.7	21	Pass	3.003	3.003	0.00	297.0	298.0	0.34	3.293	3.282	-0.33	36.77	36.76	-0.03
	22	Pass	3.006	3.005	-0.03	306.0	305.0	-0.327	3.273	3.276	0.09	36.72	36.74	0.05
	23	Pass	3.004	3.004	0.00	304.0	304.0	0.00	3.486	3.484	-0.06	37.21	37.22	0.03
	24	Pass	3.011	3.010	-0.03	294.0	294.0	0.00	8.593	8.586	-0.08	42.75	42.76	0.02
5.9	21	Pass	3.004	3.004	0.00	296.0	298.0	0.68	3.410	3.410	0.00	38.14	38.13	-0.03
	22	Pass	3.006	3.007	0.03	305.0	306.0	0.328	3.402	3.399	-0.09	38.09	38.08	-0.03
	23	Pass	3.006	3.005	-0.03	304.0	305.0	0.329	3.637	3.626	-0.30	38.64	38.63	-0.03
	24	Pass	3.012	3.013	0.03	294.0	294.0	0.00	8.725	8.714	-0.13	44.18	44.16	-0.05
6.1	21	Pass	3.006	3.005	-0.03	301.0	302.0	0.33	3.562	3.556	-0.17	39.53	39.53	0.00
	22	Pass	3.008	3.007	-0.03	307.0	309.0	0.65	3.549	3.559	0.28	39.46	39.47	0.03
	23	Pass	3.006	3.006	0.00	306.0	307.0	0.327	3.783	3.786	0.08	40.02	40.02	0.00
	24	Pass	3.015	3.020	0.17	296.0	296.0	0.00	8.873	8.848	-0.28	45.60	45.60	0.00
6.3	21	Pass	3.007	3.007	0.00	337.0	340.0	0.89	3.77	3.76	-0.27	40.93	40.92	-0.02
	22	Pass	3.008	3.008	0.00	326.0	328.0	0.613	3.771	3.764	-0.186	40.85	40.86	0.02
	23	Pass	3.007	3.006	-0.03	319.0	319.0	0.00	3.998	3.997	-0.03	41.43	41.43	0.00
	24	Pass	3.021	3.023	0.07	311.0	313.0	0.64	9.055	9.041	-0.04	47.00	47.01	0.02

DSEE testing indicates that the device should be operated with the following maximal parameter set to be robust against DSEE: VDD = 20V, PVIN =16.5V, and PVCC/AVCC = 6.3V.

No SEFIs were observed during DSEE testing.

2.1.2 SET Results

The results of the SET testing of the ISL73041SEH are displayed in Table 6. The results are summarized in Table 7.

Table 6. ISL73041SEH SET Test Results For LET = 67.5MeV•cm²/mg

Test Condition	RDU and RDL Resistors (kΩ)	VDD = PVIN (V)	Run #	DUT #	Fluence (ions/cm²)	Number of Shoot-Through Events	Number of Pulse Width Deviation Events	Number of Missing Pulse Events
#1	10	4.75	433	32	1.0E7	-	89	0
				33	1.0E7	-	0	0
			437	34	1.0E7	-	180	7
				35	1.0E7	-	63	0
#2	GND	4.75	434	32	1.0E7	-	84	0
				33	1.0E7	-	0	0
			438	34	1.0E7	-	42	0
				35	1.0E7	-	0	0

Table 6. ISL73041SEH SET Test Results For LET = 67.5MeV•cm^2/mg (Cont.)

Test Condition	RDU and RDL Resistors (kΩ)	VDD = PVIN (V)	Run #	DUT #	Fluence (ions/cm^2)	Number of Shoot-Through Events	Number of Pulse Width Deviation Events	Number of Missing Pulse Events
#3	10	13.2	435	32	1.0E7	0	0	0
				33	1.0E7	0	127	0
			439	34	1.0E7	0	100	2
				35	1.0E7	0	10	0
#4	GND	13.2	436	32	1.0E7	0	1	0
				33	1.0E7	0	76	0
			440	34	1.0E7	0	144	0
				35	1.0E7	0	2	0

Table 7. ISL73041SEH SET Results For LET = 67.5MeV•cm^2/mg

Test Condition	# of DUTs	RDU and RDL Resistors (kΩ)	VDD = PVIN (V)	Total Fluence (ions/cm^2)	Shoot-Through		Pulse Width Deviation		Missing Pulse	
					# of Events	σ (cm^2)	# of Events	σ (cm^2)	# of Events	σ (cm^2)
#1	4	10	4.75	4.0E7	-	-	332	8.3E-6	7	1.8E-7
#2	4	GND	4.75	4.0E7	-	-	126	3.2E-6	0	2.5E-8
#3	4	10	13.2	4.0E7	0	2.5E-8	237	5.9E-6	2	5.0E-8
#4	4	GND	13.2	4.0E7	0	2.5E-8	223	5.6E-6	0	2.5E-8
Worst Case						2.5E-8		8.3E-6		1.8E-7

There were no shoot-through events when VDD = VPIN = 13.2V; therefore, the cross-section for shoot-through events for TC #3 and TC #4 is 2.5E-8, which is the reciprocal of the total fluence. TC #1 and TC #2 were not tested for shoot-through events because the trigger was erroneously set such that the trigger criterion could never be met.

PHS pulse width deviation events were observed in all four test conditions. The sensitivity of the driver under each test condition to PHS pulse width deviation events can be described by the cross-section, the magnitude of the PHS pulse width deviation, and the amount of time until subsequent PHS pulse width deviations were within the ±65ns window. Figure 3, Figure 5, Figure 7, and Figure 8 show for each test condition, the proportional distributions of the maximum PHS pulse width deviation observed in each event. In these figures, the ±65ns window is indicated by vertical red lines. Some of the calculated PHS pulse width deviations may be within the ±65ns window. This is because the criterion for the trigger was the difference between the average width of the PHS pulses before the beam was turned on and the width of the PHS pulse under beam, while the criterion for this analysis is the difference between the average PHS pulse width of eight cycles that proceeded the trigger and the pulse width of the PHS pulses during or after the SET trigger. The pulse width deviation measurements should be treated as approximations. Figure 4 and Figure 6 show, for TC #1 and TC #2, the proportional distribution of the number of PHS pulses before the PHS pulse width deviation returned to the acceptable range of within ±65ns. If an event had 0 PHS pulses before recovery, the next PHS pulse following the SET had a pulse width deviation within the ±65ns window as compared to the average pulse width of eight PHS pulses preceding the SET. The conversion factor between the number of PHS pulses before recovery and the amount of time before recovery is 2µs/PHS pulse. Figure 9 shows the waveforms of a typical PHS pulse width deviation event. Figure 10 shows the

waveforms of the worst-case, greatest PHS pulse width deviation event. Table 8 summarizes the PHS pulse width deviation results for each test condition.

For TC #1, the greatest observed PHS pulse width deviation was 1362ns and the longest recovery time was ten PHS pulses before recovery, which corresponds to a duration of 20µs. 22.5% of the pulse width deviations were within the ±65ns window. The driver recovered by the next pulse 50.2% of the time.

For TC #2, the greatest observed pulse width deviation was 280ns and the longest recovery time was six pulses before recovery, which corresponds to a duration of 12µs. 53.2% of the pulse width deviations were within the ±65ns window. The driver recovered by the next pulse 68.2% of the time.

For TC #3, the greatest observed pulse width deviation was 169ns. 99.6% of the pulse width deviations were within the ±65ns window. The driver always recovered by the next pulse.

For TC #4, the greatest observed pulse width deviation was 78ns. 99.6% of the pulse width deviations were within the ±65ns window. The driver always recovered by the next pulse.

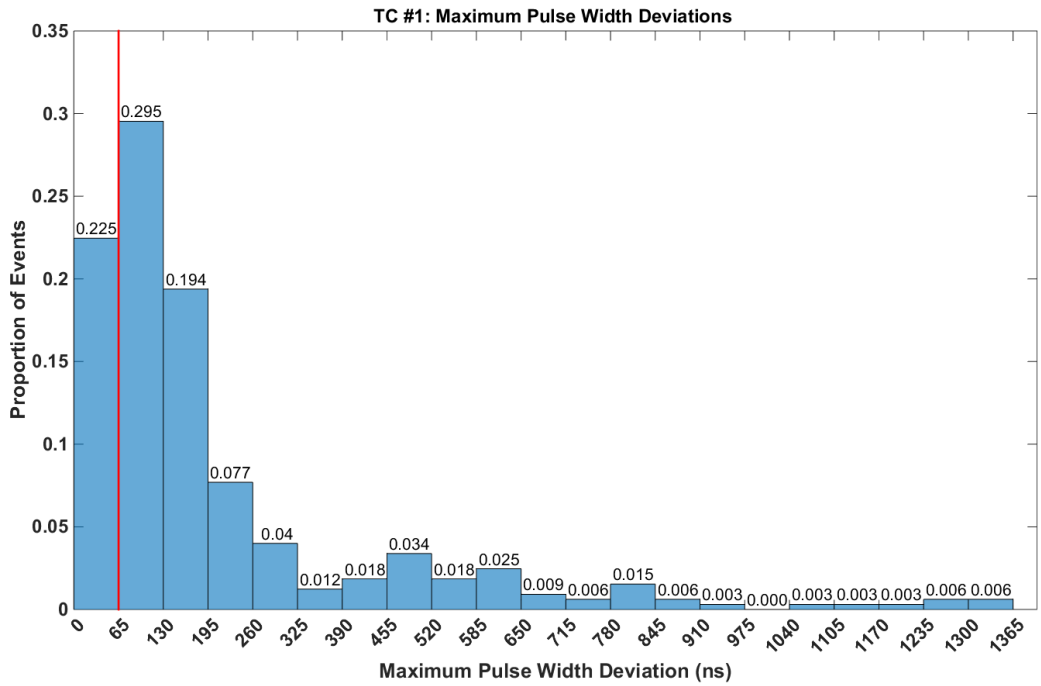

Figure 3. ISL73041SEH TC #1: Maximum Pulse Width Deviations

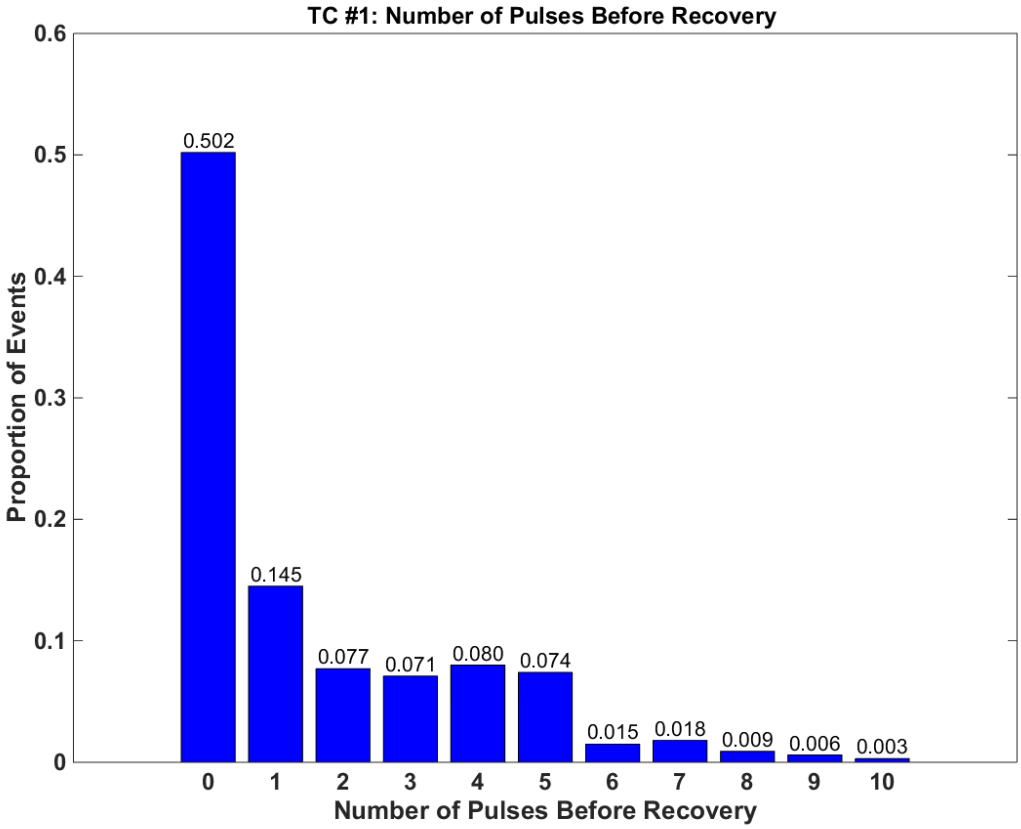

Figure 4. ISL73041SEH TC #1: Pulses Until Recovery

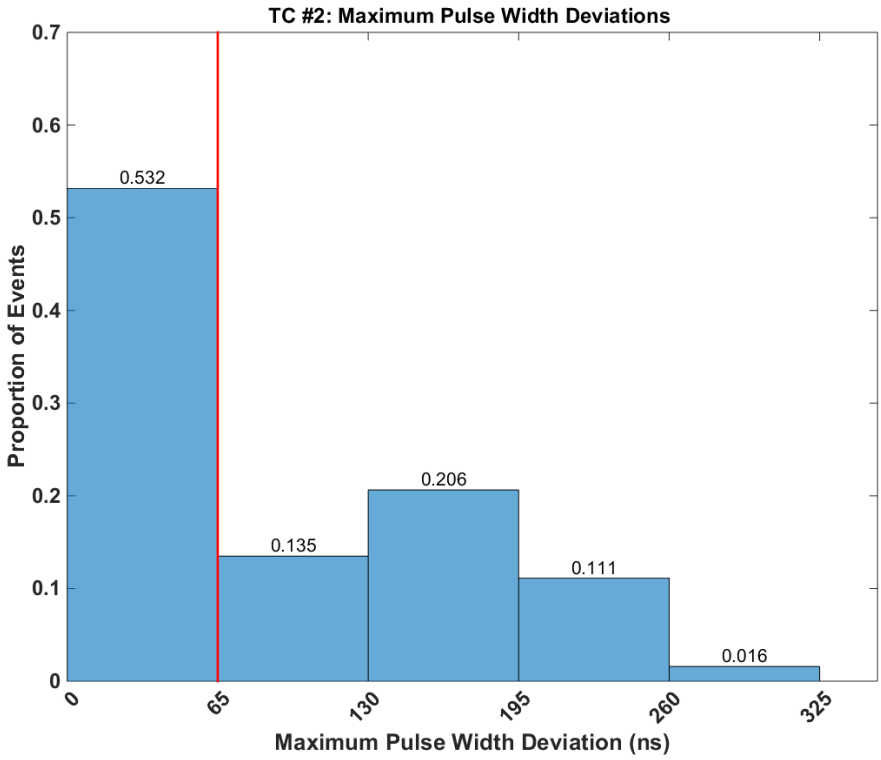

Figure 5. ISL73041SEH TC #2: Maximum Pulse Width Deviations

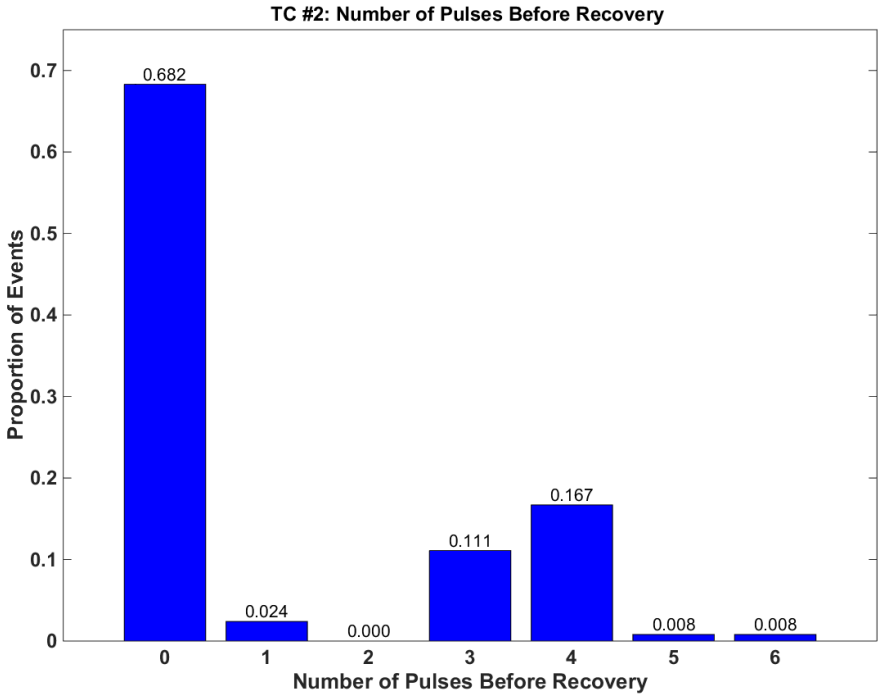

Figure 6. ISL73041SEH TC #2: Pulses Until Recovery

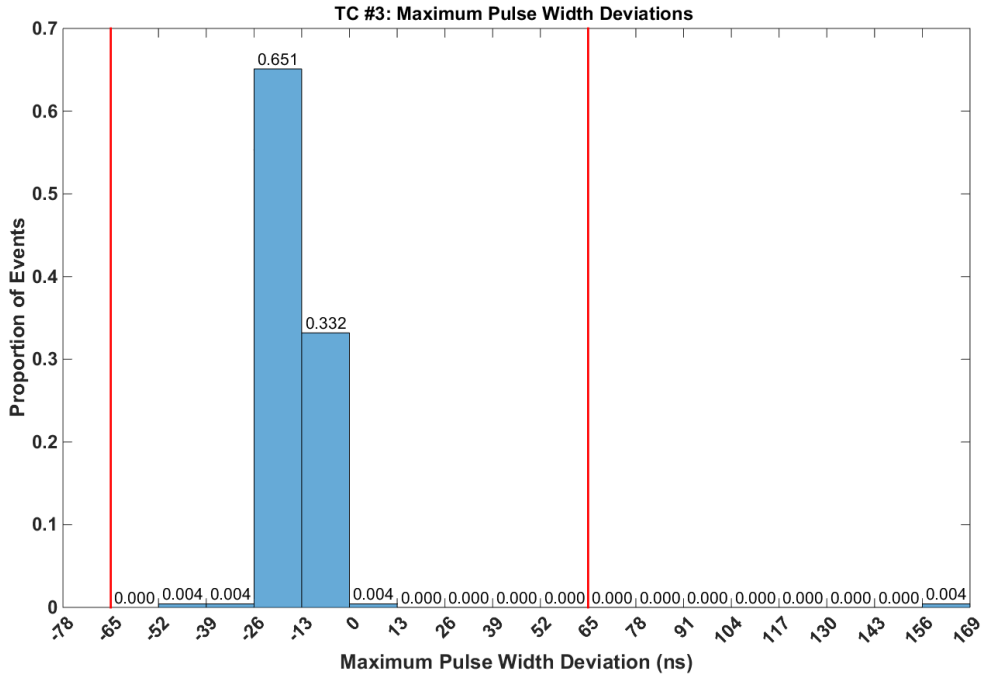

Figure 7. ISL73041SEH TC #3: Maximum Pulse Width Deviations

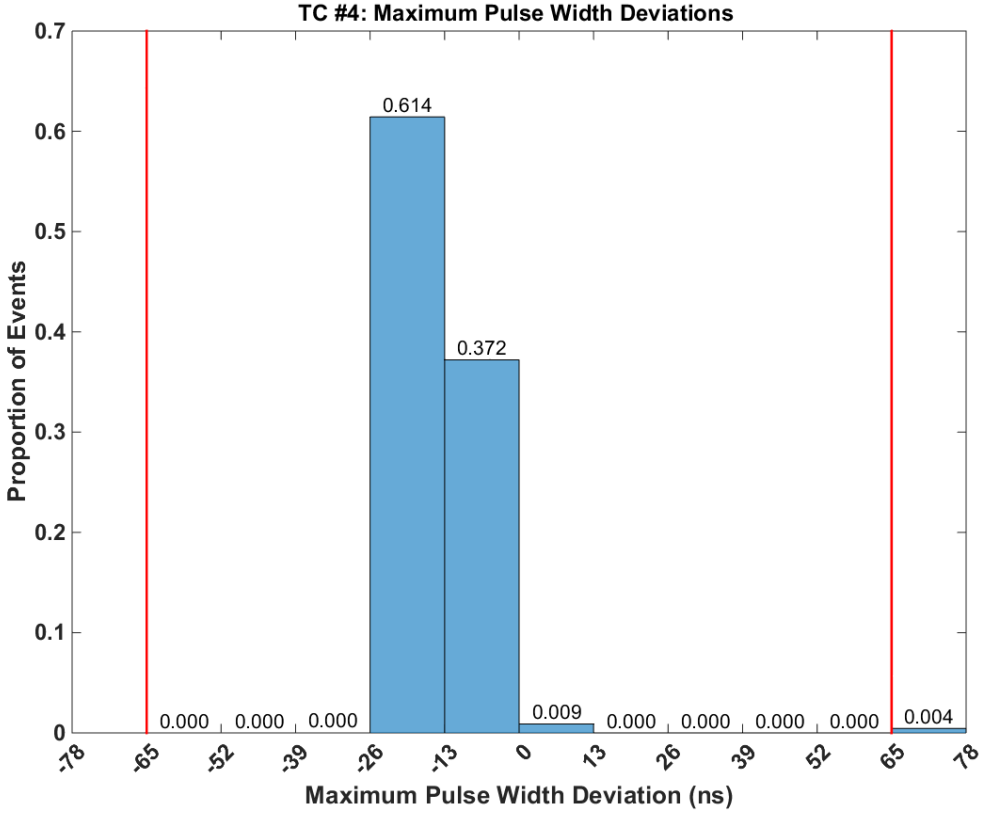

Figure 8. ISL73041SEH TC #4: Maximum Pulse Width Deviations

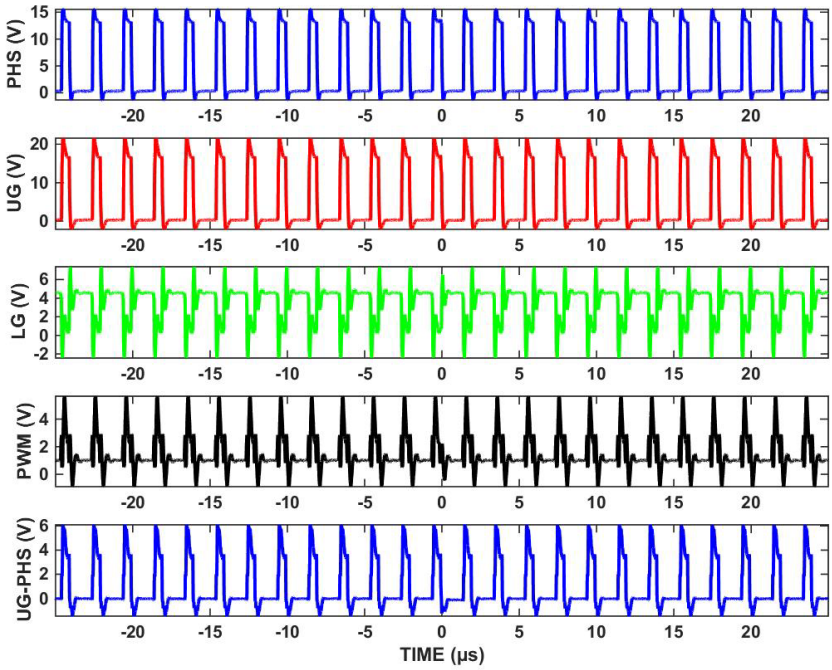

Figure 9. ISL73041SEH Typical Event, TC #4, Run 436, DUT #32, Pulse Width Deviation of 78ns

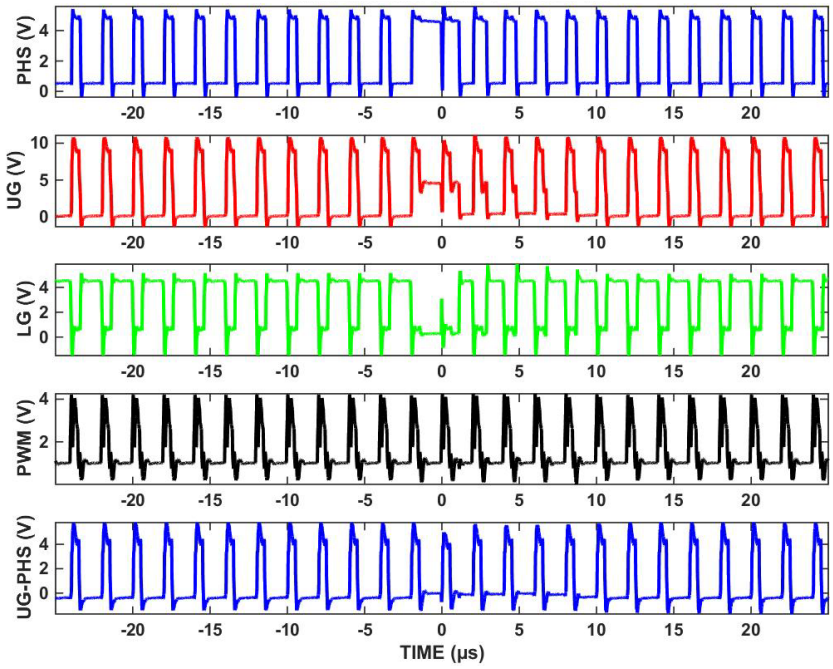

Figure 10. ISL73041SEH Worst-case Event, TC #1, Run 437, DUT #34, Pulse Width Deviation of 1362ns

Table 8. ISL73041SEH Pulse Width Deviation SET Results For LET = 67.5MeV•cm^2/mg

Test Condition	# of DUTs Tested	Total Fluence (ions/cm^2)	Pulse Width Deviation		Max SET Pulse Width Deviation (ns)	Max Recovery Time	
			# of Events	σ (cm^2)		# of Pulses	Time (µs)
#1	4	4.0E7	332	8.3E-6	1362	10	20
#2	4	4.0E7	126	3.2E-6	280	6	12
#3	4	4.0E7	237	5.9E-6	169	0	0
#4	4	4.0E7	223	5.6E-6	78	0	0
Worst Case				8.3E-6	1362	10	20

A total of nine PHS pulse width deviation events were extreme enough to constitute a missing pulse event. All nine of the missing pulse events were experienced by DUT #34 when RDL and RDU were connected to ground through a 10kΩ resistor maximizing the dead time at 50ns. The sensitivity of each test condition to missing pulse events can be described by the cross-section, the type of pulse missed, the number of pulses missed per event, and the amount of time until subsequent PHS pulse widths deviations were within the ±65ns window. Table 9 summarizes the missing pulse event results for each test condition.

The seven missing pulse events for TC #1 occurred in Run 437 and were events with missing LG pulses. In these events, PHS stayed high for the duration of an extra pulse, and there is a corresponding missing pulse in the LG signal. All of these events had similar waveforms to Figure 11. The LG signal is restored after one missed pulse; however, in the subsequent pulses there is a delay time after PWM goes low to command LG on. The UG signal momentarily sits at the PHS voltage after a UG turn off, which exceeds the 50ns dead time of the ISL73041SEH driver, before UG goes to 0V due to LG turning on and pulling PHS to 0V. The transient moment occurs on every switching cycle for approximately 10µs, with the transient moment decreasing in width during this 10µs. LG recovers after these five pulses with transient moments.

The two missing pulse events for TC #3 occurred in Run 439 and were events with missing UG-PHS pulses. In these events, LG operated normally, but two UG pulses were missed. The UG signal recovers after the 5µs of missing pulses with no distortion or delay on UG-PHS. Both SETs had similar waveforms to Figure 12.

The ISL73041SEH only experienced missing pulse events when in TC #1 and TC #3, which is when the device operated with the maximum amount of dead time. When the driver was in TC #2 and TC #4, which is when the device operated with the minimum amount of dead time, it did not experience any missing pulse events.

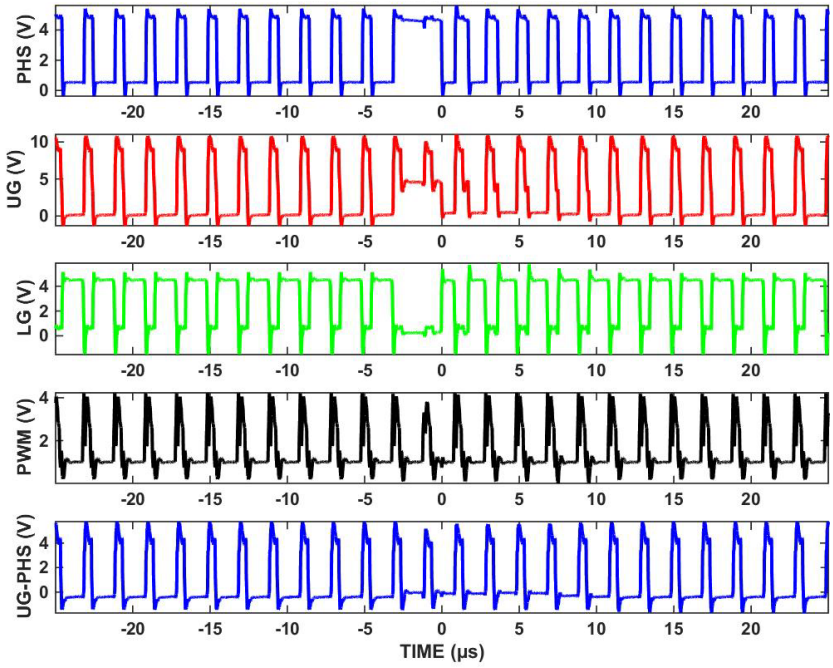

Figure 11. Typical Missing LG Pulse Event, TC #1, Run 437, DUT #34

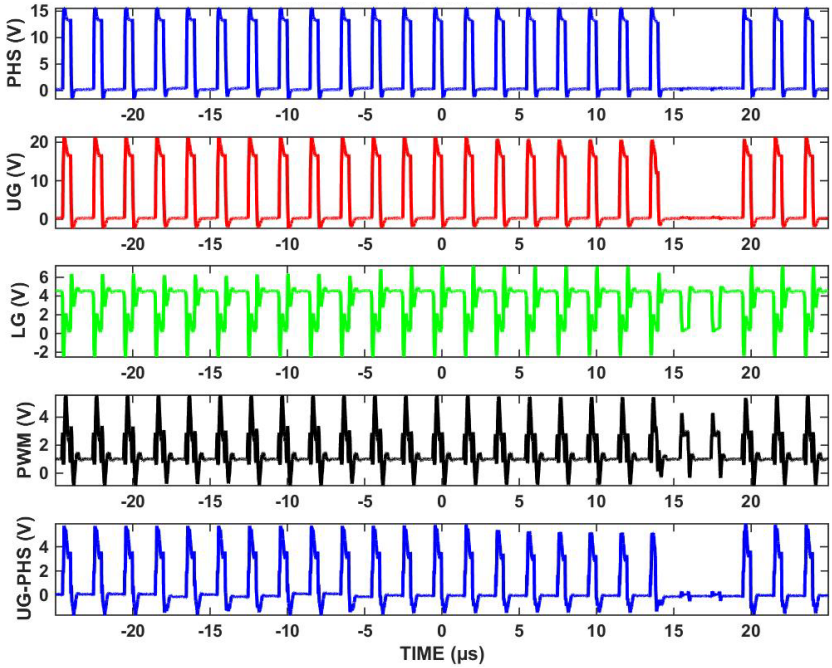

Figure 12. Typical Missing UG-PHS Pulse Event, TC #3, Run 439, DUT #34

Table 9. ISL73041SEH Missing Pulse SET Results For LET = 67.5MeV•cm^2/mg

Test Condition	# of DUTs Tested	Total Fluence (ions/cm^2)	Missing Pulse		Type of Pulse Missing	# of Pulses Missed per Event	Max Recovery Time	
			# of Events	σ (cm^2)			# of Pulses	Time (µs)
#1	4	4.0E7	7	1.8E-7	LG	1	5	10
#2	4	4.0E7	0	2.5E-8	-	-	-	-
#3	4	4.0E7	2	5E-8	UG-PHS	2	0	0
#4	4	4.0E7	0	2.5E-8	-	-	-	-
Worst Case				1.8E-7			5	10

2.2 LET = 86.3 MeV•cm^2/mg

2.2.1 DSEE Results

The results of VDD DSEE testing are displayed in Table 10. No devices experienced DSEE while under the beam; therefore, testing indicates that you should operate the device with a maximal value of VDD = 20V to be robust against DSEE.

Table 10. ISL73041SEH VDD DSEE Test Results For LET = 86.3MeV•cm^2/mg

VDD (V)	DUT #	Result	I_{VDD} (±20%)		
			Pre (mA)	Post (mA)	Δ (%)
16.0	5	Pass	33.11	33.10	-0.03
	6	Pass	33.10	33.00	-0.30
	7	Pass	33.16	33.13	-0.09
	8	Pass	32.68	32.72	0.12
17.0	5	Pass	33.10	33.09	-0.03
	6	Pass	33.00	32.99	-0.03
	7	Pass	33.13	33.12	-0.03
	8	Pass	32.73	32.66	-0.21
18.0	5	Pass	33.09	33.090	0.00
	6	Pass	33.00	32.99	-0.03
	7	Pass	33.12	33.11	-0.03
	8	Pass	32.66	32.55	-0.34
19.0	5	Pass	33.09	33.09	0.00
	6	Pass	32.99	32.98	-0.03
	7	Pass	33.11	33.03	-0.24
	8	Pass	32.55	32.59	0.12
20.0	5	Pass	33.09	33.08	-0.03
	6	Pass	32.98	32.98	0.00
	7	Pass	33.03	32.99	-0.12
	8	Pass	32.58	32.64	0.18

Table 11 shows the results of PVIN DSEE testing. DUTs 3 and 4 experienced DSEEs with PVIN = 14.5V, the first voltage at which they were tested. It is unknown whether DUTs 3 and 4 would have experienced DSEEs at a lower PVIN voltage; however, four devices passed with PVIN = 13.5V, and no devices failed at that voltage, so PVIN = 13.5V is a reasonable maximal value for operation robust against DSEE.

Table 11. ISL73041SEH PVIN DSEE Test Results For LET = 86.3MeV•cm^2/mg

PVIN (V)	DUT #	Result	I_{VDD} (±20%)			I_{PVCC} (±20%)		
			Pre (mA)	Post (mA)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)
11.5	5	Pass	3.320	3.330	0.30	30.23	30.22	-0.03
	6	Pass	3.360	3.370	0.30	30.00	29.99	-0.03
12.5	5	Pass	3.330	3.330	0.00	30.46	30.45	-0.03
	6	Pass	3.370	3.360	-0.30	30.16	30.15	-0.03
13.5	1	Pass	3.481	3.483	0.06	30.47	30.73	0.83
	2	Pass	3.419	3.433	0.41	31.16	31.14	-0.05
	5	Pass	3.339	3.341	0.06	31.05	31.03	-0.07
	6	Pass	3.367	3.352	-0.45	30.80	30.80	0.00
14.5	1	Pass	3.480	3.450	-0.86	31.40	31.39	-0.03
	2	Pass	3.431	3.433	0.06	30.92	30.93	0.03
	3	Fail	3.240	246	7493	31.23	494	1482
	4	Fail	3.250	249	7562	31.36	505	1510
	5	Pass	3.342	3.350	0.24	31.28	31.30	0.06
	6	Pass	3.352	3.390	1.13	31.05	31.06	0.03
15.5	1	Pass	3.450	3.450	0.00	31.63	31.63	0.00
	2	Pass	3.430	3.460	0.87	31.16	31.17	0.03
	5	Fail	3.350	258	7601	31.56	563	1683
	6	Pass	3.390	3.380	-0.29	31.32	31.19	-0.42
16.5	1	Pass	3.450	3.470	0.58	31.83	31.85	0.06
	2	Pass	3.460	3.440	-0.58	31.40	31.37	-0.10
17.5	1	Pass	3.470	3.520	1.44	32.61	32.64	0.09
	2	Pass	3.440	3.420	-0.58	31.75	31.69	-0.19

Table 12 shows the results of AVCC/PVCC DSEE testing. No devices experienced DSEE while under beam; therefore, testing indicates that you should operate the device with a maximal value of PVCC = 6.5V and AVCC = 6.3V to be robust against DSEE.

Table 12. ISL73041SEH AVCC/PVCC DSEE Test Results For LET = 86.3MeV·cm^2/mg

PV_{CC} (V)	AV_{CC} (V)	DUT #	Result	V_{OUT} (±2%)			I_{VDD} (±20%)			I_{AVCC} (±20%)			I_{PVCC} (±20%)		
				Pre (V)	Post (V)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)
5.7	5.7	9	Pass	3.011	3.011	0.00	0.354	0.354	0.00	3.310	3.307	-0.09	37.46	37.46	0.01
		10	Pass	3.010	3.011	0.03	0.257	0.254	-1.17	3.377	3.375	-0.06	37.50	37.51	0.03

Table 12. ISL73041SEH AVCC/PVCC DSEE Test Results For LET = 86.3MeV·cm²/mg (Cont.)

PV_{CC} (V)	AV_{CC} (V)	DUT #	Result	V_{OUT} (±2%)			I_{VDD} (±20%)			I_{AVCC} (±20%)			I_{PVCC} (±20%)		
				Pre (V)	Post (V)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)
5.9	5.9	9	Pass	3.012	3.014	0.07	0.351	0.354	0.85	3.438	3.420	-0.52	38.87	38.87	0.00
		10	Pass	3.012	3.011	-0.03	0.248	0.252	1.61	3.509	3.510	0.03	38.91	38.92	0.02
		11	Pass	3.006	3.006	0.00	0.354	0.351	-0.85	3.690	3.690	0.00	38.20	38.22	0.05
		12	Pass	3.008	3.007	-0.03	0.257	0.257	0.00	3.520	3.510	-0.28	38.78	38.79	0.03
6.1	6.1	9	Pass	3.016	3.014	-0.07	0.354	0.354	0.00	3.570	3.580	0.28	40.23	39.58	-1.62
		10	Pass	3.012	3.014	0.07	0.251	0.251	0.00	3.660	3.650	-0.27	40.28	40.27	-0.02
		11	Pass	3.007	3.008	0.03	0.354	0.351	-0.85	3.860	3.860	0.00	39.61	39.58	-0.08
		12	Pass	3.009	3.007	-0.07	0.257	0.257	0.00	3.670	3.670	0.00	40.17	39.55	-1.54
6.3	6.3	9	Pass	3.015	3.016	0.03	0.371	0.371	0.00	3.780	3.780	0.00	41.00	41.11	0.27
		10	Pass	3.015	3.015	0.00	0.266	0.266	0.00	3.860	3.860	0.00	41.67	41.01	-1.58
		11	Pass	3.007	3.006	-0.03	0.371	0.371	0.00	4.080	4.077	-0.07	40.99	40.56	-1.05
		12	Pass	3.009	3.009	0.00	0.287	0.284	-1.05	3.880	4.010	3.35	41.09	41.12	0.07
6.5	6.3	9	Pass	3.016	3.015	-0.03	0.371	0.371	0.00	3.770	3.760	-0.27	42.48	42.53	0.12
		10	Pass	3.015	3.016	0.03	0.266	0.266	0.00	3.850	3.860	0.26	42.46	42.47	0.02
		11	Pass	3.007	3.007	0.00	0.371	0.371	0.00	4.070	4.082	0.29	41.75	42.08	0.79
		12	Pass	3.011	3.012	0.03	0.284	0.284	0.00	4.009	3.999	-0.25	42.51	42.44	-0.16
6.7	6.3	11	Pass	3.009	3.006	-0.10	0.371	0.371	0.00	4.071	4.060	-0.27	43.51	43.48	-0.07
		12	Pass	3.012	3.013	0.03	0.287	0.284	-1.05	3.980	4.000	0.50	43.81	44.04	0.52

DSEE testing indicates that you should operate the device with the following maximal parameter set: VDD = 20V, PVIN =13.5V, PVCC = 6.5V, and AVCC = 6.3V.

No SEFIs were observed during DSEE testing.

2.2.2 SET Results

The results of the SET testing of the ISL73041SEH are displayed in Table 13. The results are summarized in Table 14.

Table 13. ISL73041SEH SET Test Results For LET = 86.3MeV•cm²/mg

Test Condition	RDU and RDL Resistors (kΩ)	VDD =PVIN (V)	Run #	DUT #	Fluence (ions/cm²)	Number of Shoot-Through Events	Number of Pulse Width Deviation Events	Number of Missing Pulse Events
#1	10	4.75	101	13	1.0E7	0	94	0
				14	1.0E7	0	69	0
			105	15	1.0E7	0	144	0
				16	1.0E7	0	36	31

Table 13. ISL73041SEH SET Test Results For LET = 86.3MeV•cm^2/mg (Cont.)

Test Condition	RDU and RDL Resistors (kΩ)	VDD =PVIN (V)	Run #	DUT #	Fluence (ions/cm^2)	Number of Shoot-Through Events	Number of Pulse Width Deviation Events	Number of Missing Pulse Events
#2	GND	4.75	102	13	1.0E7	0	113	0
				14	1.0E7	0	48	0
			106	15	1.0E7	0	238	55
				16	1.0E7	0	104	29
#3	10	13.2	103	13	1.0E7	0	10	0
				14	1.0E7	0	746	0
			107	15	1.0E7	0	602	12
				16	1.0E7	0	459	21
#4	GND	13.2	104	13	1.0E7	0	1	0
				14	1.0E7	0	933	0
			108	15	1.0E7	0	768	24
				16	1.0E7	0	529	17

Table 14. ISL73041SEH SET Results For LET = 86.3MeV•cm^2/mg

Test Condition	# of DUTs	RDU and RDL Resistors (kΩ)	VDD = PVIN (V)	Total Fluence (ions/cm^2)	Shoot-Through		Pulse Width Deviation		Missing Pulse	
					# of Events	σ (cm^2)	# of Events	σ (cm^2)	# of Events	σ (cm^2)
#1	4	10	4.75	4.0E7	0	2.5E-8	343	8.6E-6	31	7.8E-7
#2	4	GND	4.75	4.0E7	0	2.5E-8	503	1.3E-5	84	2.1E-6
#3	4	10	13.2	4.0E7	0	2.5E-8	1817	4.5E-5	33	8.3E-7
#4	4	GND	13.2	4.0E7	0	2.5E-8	2231	5.6E-5	40	1E-6
Worst Case						2.5E-8		5.6E-5		2.1E-6

There were zero shoot-through events; therefore, the cross-section for shoot-through events for all test conditions is 2.5E-8cm^2, which is the reciprocal of the total fluence.

PHS pulse width deviation events were observed in all four test conditions. The sensitivity of the driver under each test condition to PHS pulse width deviation events can be described by the cross-section, the magnitude of the PHS pulse width deviation, and the amount of time until subsequent PHS pulse width deviations were within the ±65ns window. Figure 13, Figure 15, Figure 17, and Figure 19 show for each test condition the proportional distributions of the maximum PHS pulse width deviation observed in each event. In these figures, the ±65ns window is indicated by vertical red lines. Some calculated PHS pulse width deviations may be within the ±65ns window because the criterion for the trigger was the difference between the average width of the PHS pulses before the beam was turned on and the width of the PHS pulse under the beam.

In contrast, the criterion for this analysis is the difference between the average PHS pulse width of eight cycles that proceeded the trigger and the pulse width of the PHS pulses during or after the SET trigger. The pulse width deviation measurements should be treated as approximations. Figure 14 and Figure 16 show, for TC #1 and TC

#2, the proportional distribution of the number of PHS pulses before the PHS pulse width deviation returned to the acceptable range of within ±65ns. If an event had 0 PHS pulses before recovery, the next PHS pulse following the SET had a pulse width deviation within the ±65ns window compared to the average pulse width of eight PHS pulses preceding the SET. The conversion factor between the number of PHS pulses before recovery and the time before recovery is 2µs/PHS pulse. Figure 19 shows the waveforms of a typical PHS pulse width deviation event. Figure 20 shows the waveforms of the worst-case, greatest PHS pulse width deviation event. Table 15 summarizes the PHS pulse width deviation results for each test condition.

For TC #1, the greatest observed PHS pulse width deviation was 517ns, and the longest recovery time was ten PHS pulses before recovery, corresponding to a duration of 20µs. 3.5% of the pulse width deviations were within the ±65ns window. The driver recovered by the next pulse 66.5% of the time.

For TC #2, the greatest observed pulse width deviation was 406ns, and the longest recovery time was eleven pulses before recovery, corresponding to a duration of 22µs. 20.3% of the pulse width deviations were within the ±65ns window. The driver recovered by the next pulse 65.3% of the time.

For TC #3, the greatest observed pulse width deviation was 409ns. 99.5% of the pulse width deviations were within the ±65ns window. The driver always recovered by the next pulse.

For TC #4, the greatest observed pulse width deviation was 307ns. 99.8% of the pulse width deviations were within the ±65ns window. The driver recovered by the next pulse 99.9% of the time. The other 0.1% of the time, the driver recovered after one pulse.

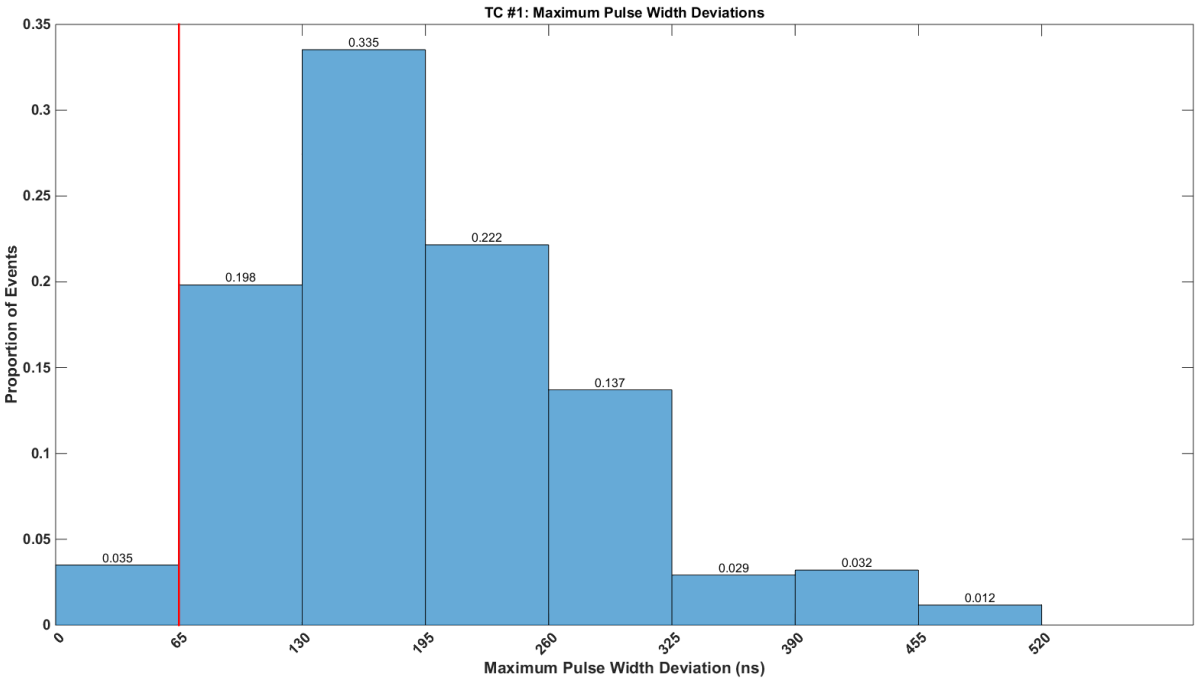

Figure 13. ISL73041SEH TC #1: Maximum Pulse Width Deviations

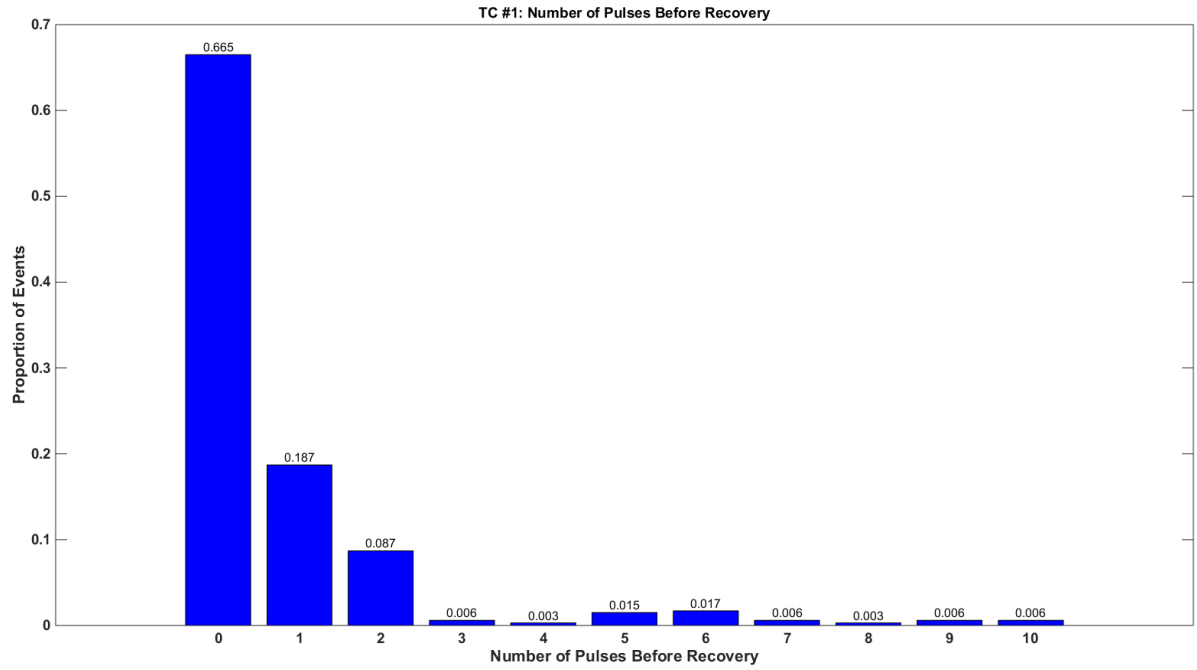

Figure 14. ISL73041SEH TC #1: Pulses Until Recovery

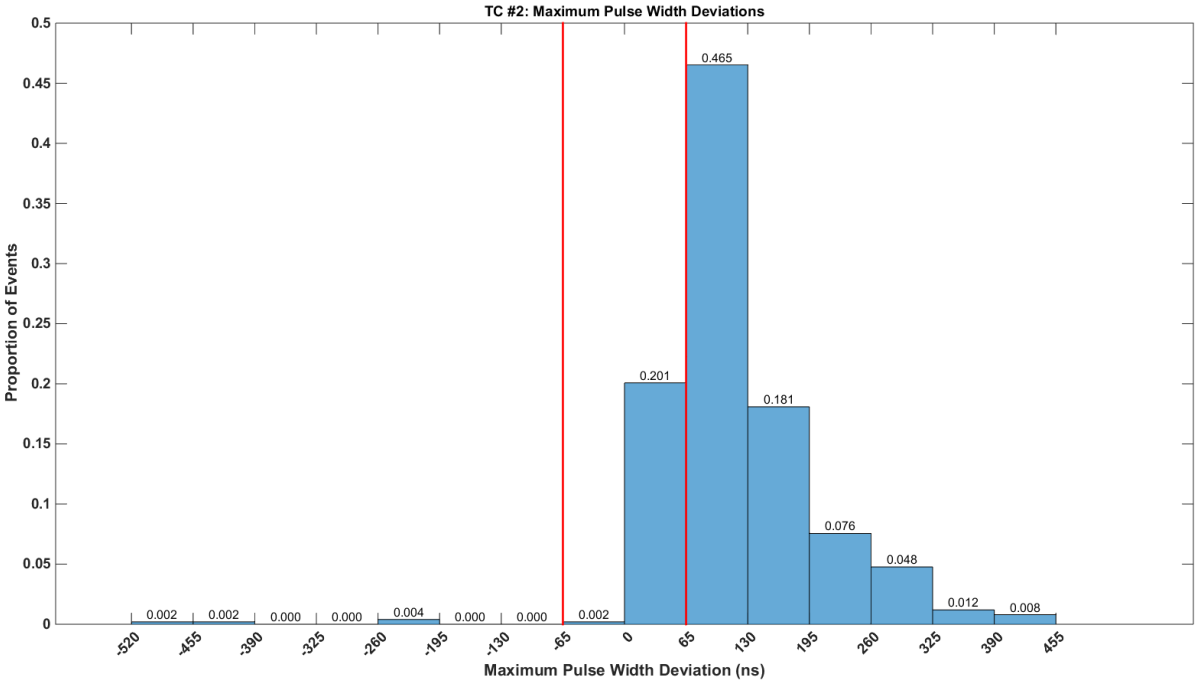

Figure 15. ISL73041SEH TC #2: Maximum Pulse Width Deviations

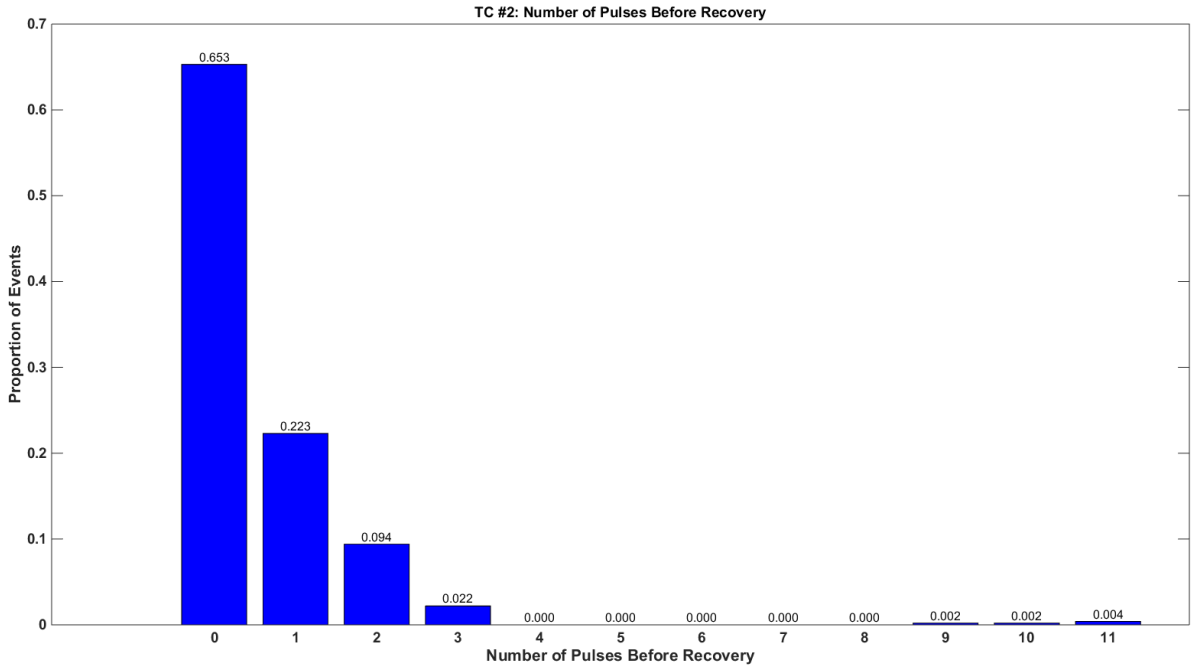

Figure 16. ISL73041SEH TC #2: Pulses Until Recovery

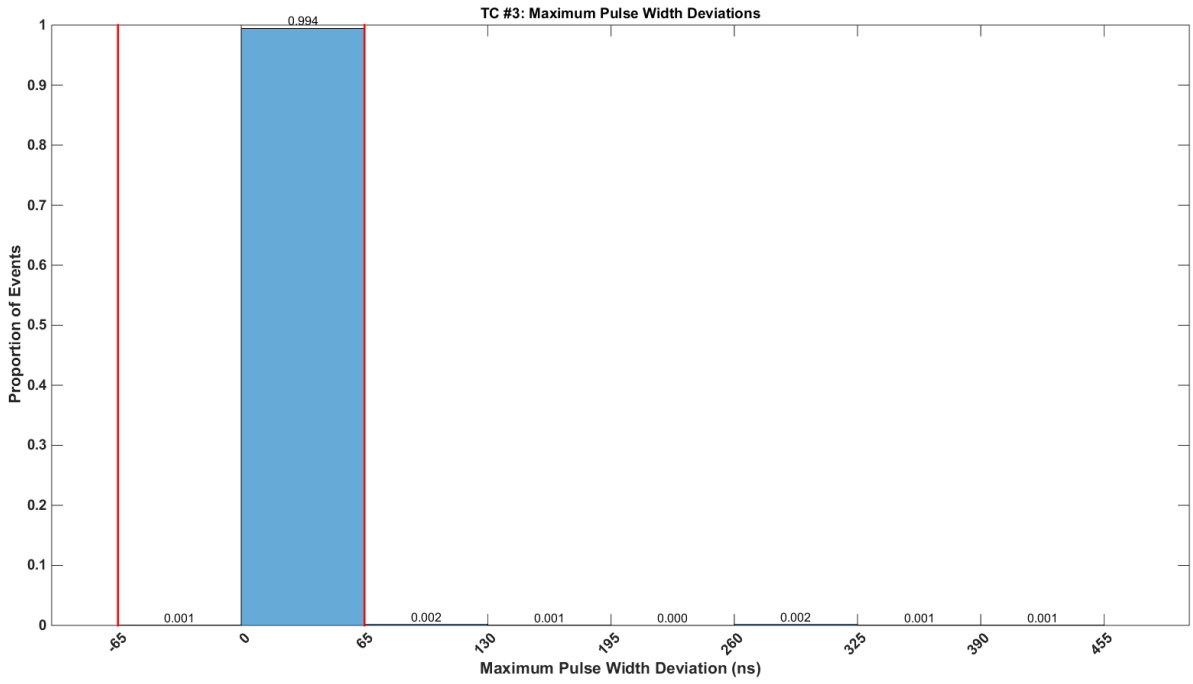

Figure 17. ISL73041SEH TC #3: Maximum Pulse Width Deviations

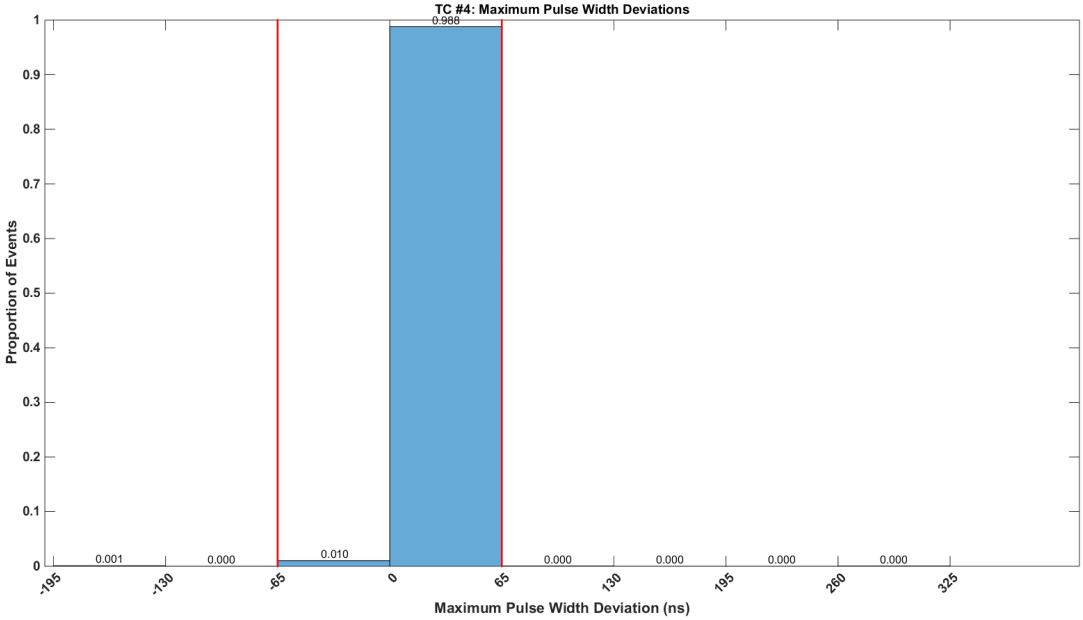

Figure 18. ISL73041SEH TC #4: Maximum Pulse Width Deviations

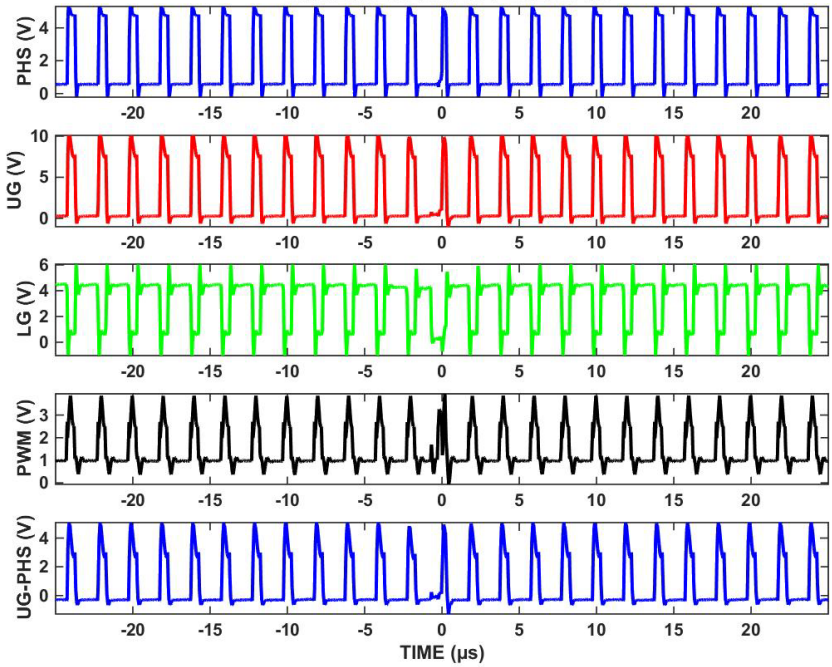

Figure 19. ISL73041SEH Typical Event, TC #2, Run 106, Pulse Width Deviation of -224ns

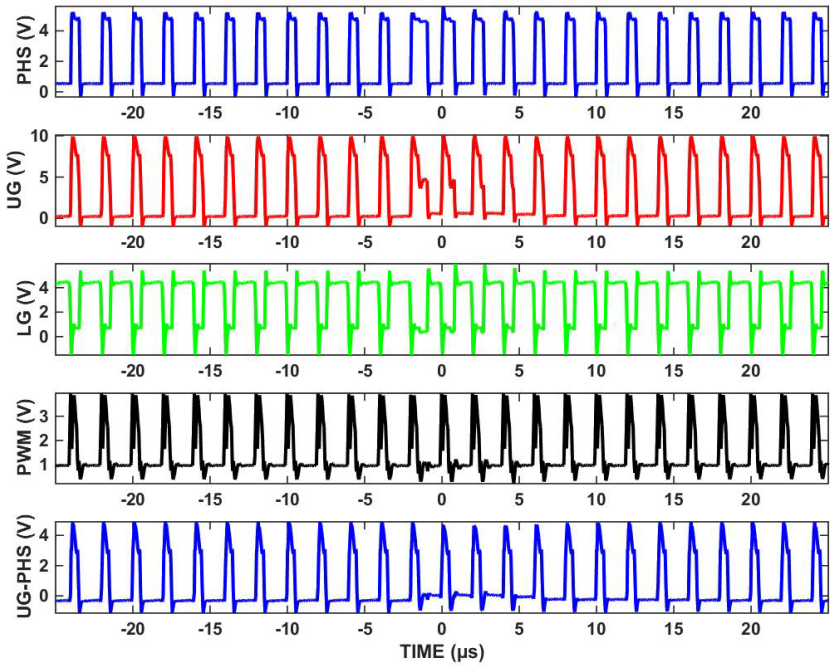

Figure 20. ISL73041SEH Worst-case Event, TC #1, Run 105, Pulse Width Deviation of 517ns

Table 15. ISL73041SEH Pulse Width Deviation SET Results For LET = 86.3MeV•cm^2/mg

Test Condition	# of DUTs Tested	Total Fluence (ions/cm^2)	Pulse Width Deviation		Max SET Pulse Width Deviation (ns)	Max Recovery Time	
			# of Events	σ (cm^2)		# of Pulses	Time (µs)
#1	4	4.0E7	343	8.6E-6	517	10	20
#2	4	4.0E7	503	1.3E-5	406	11	22
#3	4	4.0E7	1817	4.5E-5	409	0	0
#4	4	4.0E7	2231	5.6E-5	307	1	2
Worst Case	-	-	-	5.6E-5	517	11	22

Some PHS pulse width deviation events were extreme enough to constitute a missing pulse event. There were three types of missing pulse events:

- Events in which LG pulses were missed
- Events in which UG-PHS pulses were missed
- Events in which both UG-PHS and LG pulses were missed.

There were no events in which only LG pulses were missing detected during testing with normal incidence gold, although several such events were detected when testing with praseodymium. Those events had waveforms similar to Figure 11.

The waveforms for events in which UG-PHS pulses were missing were similar to Figure 21. UG-PHS pulses were missing in these events, but the LG pulses were unaffected. A maximum of two UG-PHS pulses were missed. The maximum time until the driver recovered after the missing pulse event was 2µs. Table 16 is a summary of the missing UG-PHS events.

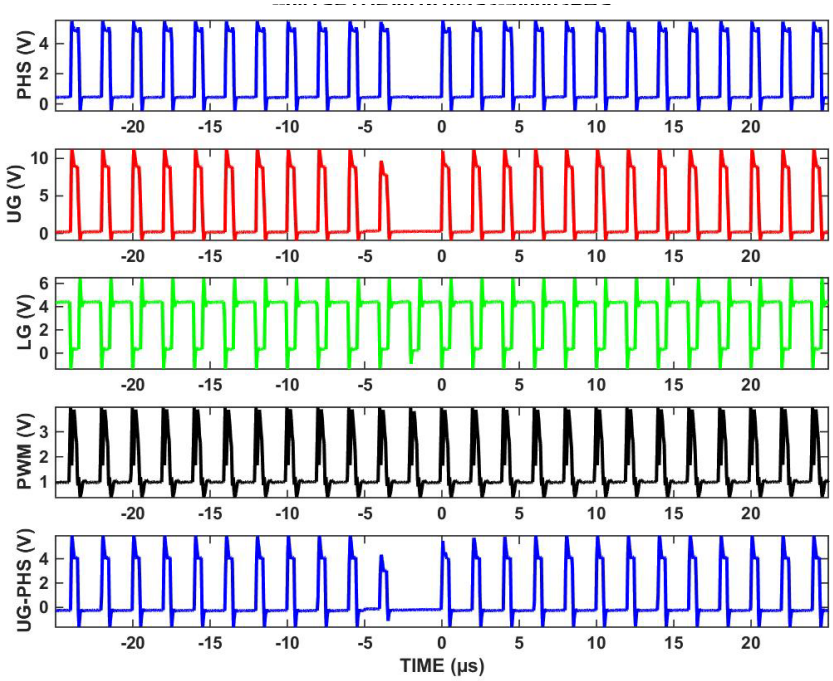

Figure 21. Typical Missing UG-PHS Pulse Event

Table 16. ISL73041SEH Missing UG-PHS Pulse SET Results For LET = 86.3MeV•cm^2/mg

Test Condition	# of DUTs Tested	Total Fluence (ions/cm^2)	Missing UG-PHS Pulse		Max # of Pulses Missed per Event	Max Recovery Time	
			# of Events	σ (cm^2)		# of Pulses	Time (µs)
#1	4	4.0E7	31	7.8E-7	1	0	0
#2	4	4.0E7	70	1.8E-6	2	0	0
#3	4	4.0E7	21	5.3E-7	2	1	2
#4	4	4.0E7	18	4.5E-7	2	1	2
Worst Case	-	-	-	1.8E-6	2	1	2

The waveforms for events in which UG-PHS and LG pulses were missing were similar to Figure 22. UG-PHS pulses were missing in these events and the corresponding LG pulses were severely distorted or missing. A maximum of two UG-PHS pulses were missed. The maximum time until the driver recovered after the missing pulse event was 2µs. Table 17 is a summary of the missing UG-PHS and LG events.

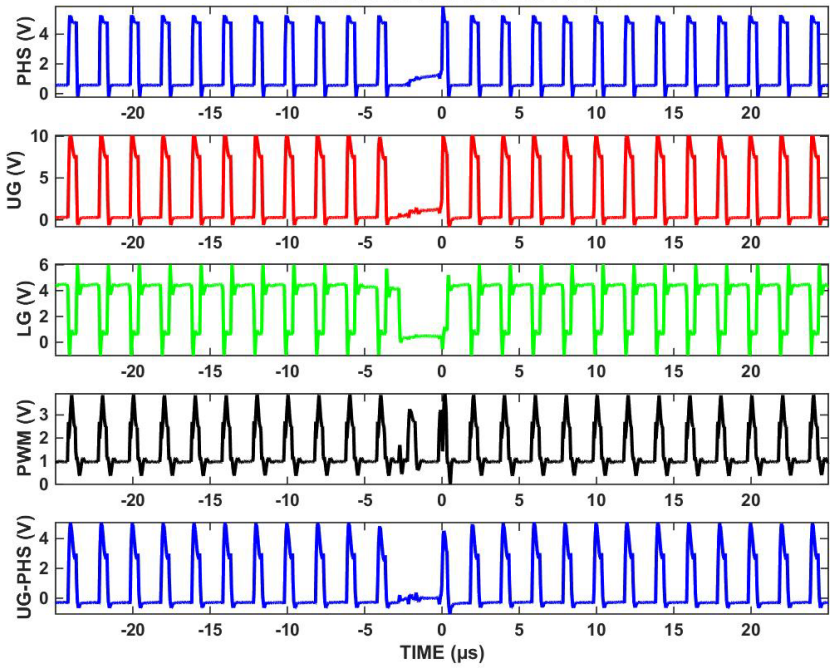

Figure 22. Typical Missing UG-PHS Pulse and LG Pulse Event

Table 17. ISL73041SEH Missing UG-PHS and LG Pulses SET Results For LET = 86.3MeV•cm^2/mg

Test Condition	# of DUTs Tested	Total Fluence (ions/cm^2)	Missing UG-PHS and LG Pulses		Max # of Pulses Missed per Event	Max Recovery Time	
			# of Events	σ (cm^2)		# of Pulses	Time (µs)
#1	4	4.0E7	0	2.5E-8	-	-	-
#2	4	4.0E7	14	3.5E-7	1	0	0
#3	4	4.0E7	12	3.0E-7	2	1	2
#4	4	4.0E7	24	6.0E-7	2	1	2
Worst Case	-	-	-	6.0E-7	2	1	2

3. Discussion and Conclusion

Since SEE testing is performed with the devices under test decapsulated, the results of this report also apply to the ISL71441SLH as the only difference between the parts are that the ISL73041SEH has a ceramic package and the ISL71441SLH has a plastic package.

3.1 LET of 67.5MeV•cm^2/mg

The ISL73041SEH proved to be free of Destructive Single Event Effects (DSEE) including SEL with VDD = 20V, PVIN = 16.5V, and PVCC = AVCC = 6.3V at a die temperature of 125°C when irradiated with normal incidence praseodymium at a LET of 67.5MeV•cm^2/mg. For DSEE testing, the ISL73041SEH drove ISL70020SEH GaN FETs at a PWM 25% duty cycle/500kHz.

A SEFI was defined as an event in which FLTb pulled low. SEFIs were monitored for during DSEE testing. No SEFIs were observed during testing.

The ISL73041SEH was tested for two types of SETs over four test conditions. The first type of SET was an event which caused shoot-through. The trigger on shoot-through events was erroneously set such that shoot-through results were only reliable when VDD = VPIN = 13.2V. The driver experienced zero shoot-through SETs when VDD = VPIN = 13.2V. The second type of SET was an event in which the PHS pulse width deviated beyond ±65ns from the average PHS pulse width before turning on the beam. Some of these deviations were extreme enough to constitute a complete missing pulse event. The largest cross section for a PHS pulse width deviation events was 8.3E-6cm^2. The largest deviation from the average PHS pulse width was 1362ns and the maximum number of subsequent PHS pulses until pulse width deviations were within ±65ns from the average pulse width was ten PHS pulses. The largest cross section for a missing pulse event was 1.8E-7cm^2. The maximum number of pulses missed in an event was two pulses, and the maximum number of subsequent PHS pulses until pulse width deviations were within ±65ns from the average pulse width was five PHS pulses. For testing, each device was irradiated to a fluence of 1E7ions/cm^2 with normal incidence praseodymium at a LET of 67.5MeV•cm^2/mg. SET testing was performed with a die temperature of 25°C.

Praseodymium was used for the SEE testing because the cyclotron did not have gold ion capabilities at the time of testing.

3.2 LET of 86.3MeV•cm^2/mg

The ISL73041SEH did not experience any Destructive Single Event Effects (DSEE) including SEL with VDD = 20V, PVIN = 13.5V, PVCC = 6.5V, and AVCC = 6.3V at a die temperature of 125°C when irradiated with normal incidence gold at a LET of 86.3MeV•cm^2/mg. For DSEE testing, the ISL73041SEH drove ISL70020SEH GaN FETs at a PWM 25% duty cycle/500kHz.

A SEFI was defined as an event in which FLTb pulled low. SEFIs were monitored for during DSEE testing. No SEFIs were observed during DSEE testing.

The ISL73041SEH was tested for two types of SETs over four test conditions. The first type of SET was an event which caused shoot-through. The driver experienced zero shoot-through SETs. The second type of SET was an event in which the PHS pulse width deviated beyond ±65ns from the average PHS pulse width before turning on the beam. Some deviations were extreme enough to constitute a complete missing pulse event. The largest cross section for a PHS pulse width deviation events was 5.6E-5cm^2. The largest deviation from the average PHS pulse width was 517ns and the maximum number of subsequent PHS pulses until pulse width deviations were within ±65ns from the average pulse width was eleven PHS pulses. The largest cross section for a missing pulse event was 2.1E-6cm^2. The maximum number of pulses missed in an event was two pulses. The maximum number of subsequent PHS pulses until pulse width deviations were within ±65ns from the average pulse width was one PHS pulses. For testing, each device was irradiated to a fluence of 1E7ions/cm^2 with normal incidence gold at a LET of 86.3MeV•cm^2/mg. SET testing was performed with a die temperature of 25°C.

4. Revision History

Revision	Date	Description
1.03	Dec 16, 2024	Added ISL71441SLH references.
1.02	Feb 27, 2024	Updated LETs in the active silicon ranges on page 1. Changed VSENSE to PVIN on page 5 and changed the wording from PVIN was tied to VDD to PVIN was set to the same voltage as VDD. Added Figure 1 and updated Figure 2.
1.01	May 31, 2023	Added the LET = 86.3MeV•cm^2/mg information throughout the document.
1.00	Feb 3, 2023	Initial release.

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