

## ISL73847SLH

Single Event Effects (SEE) Testing of the ISL73847SLH Synchronous Buck Controller

### Introduction

The intense proton and heavy ion environment encountered in space applications can cause a variety of Destructive Single Event Effects (DSEE) in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Latch-Up (SEL), Single Event Gate Rupture (SEGR), and Single Event Burnout (SEB). SEE can lead to system-level performance issues including disruption, degradation, and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. This report discusses the results of SEE testing performed on the [ISL73847SLH](#) product. The ISL73847SLH is offered with radiation assurance screening to 75krad(Si) at 10mrad(Si)/s.

### SEE Test Result Overview

The ISL73847SLH proved to be free of DSEE including SEL at a VDD voltage of 25.0V and a case temperature of 125°C when irradiated with normal incidence Gold (<sup>197</sup>Au) at a Linear Energy Transfer (LET) of 86MeV·cm<sup>2</sup>/mg. The device was also free of DSEE including SEL at a VCC voltage of 6.7V. Additionally, the ISL73847SLH proved to be free of SEFIs at a ISENSE voltage of 10V. The 2-phase buck output of 1.0V was loaded to a total of 5A.

The buck regulator was tested for SEE at switching frequencies ( $f_{SW}$ ) of 500kHz and 1000kHz, each requiring separate board assemblies. The 500kHz configuration used an output inductor ( $L_{OUTX}$ ) of 1μH an output capacitor ( $C_{OUT}$ ) of 880μF. No SET deviations exceeding ±20mV (±2% on the 1.0V output with 5.0A load) were captured. The 1000kHz configuration used an output inductor ( $L_{OUTX}$ ) of 0.56μH an output capacitor ( $C_{OUT}$ ) of 880μF.

One SET event with a deviation greater than ±20mV was observed, which showed as a missing pulse on PWM output. The DSEE testing were performed on twelve devices, four each for VDD, VCC, and ISENSE testing. The SET testing was performed on two devices at a  $f_{SW}$  of 500kHz and another two at an  $f_{SW}$  of 1000kHz. Each of the device runs were irradiated with normal incidence gold for a LET of 86MeV·cm<sup>2</sup>/mg to a fluence of 1E7particle/cm<sup>2</sup>. See [Table 2](#), [Table 3](#), [Table 4](#), and [Table 5](#) for more details.

### Product Description

The ISL73847SLH is a synchronous buck controller that can operate as a single or dual-phase controller. It is intended to work with the ISL71441x (half-bridge GaN FET driver) to generate point-of-load voltage rails for radiation-hardened space applications.

It accepts an input voltage range of 4.5V to 19V with a programmable output switching frequency between 250kHz and 1.5MHz set with a single resistor. The output can regulate a voltage upwards of 600mV and is limited on the top end by the minimum off-time and selected switching frequency.

The wide input voltage range makes it a suitable power supply option for a high current FPGA core and other general-purpose power solutions. The ISL73847SLH uses current mode modulation, which simplifies loop compensation and provides excellent power supply rejection. Additionally, the output is remotely sensed to compensate for any voltage drop in the load conditions. Together this results in a robust power supply solution that requires minimal components while achieving high current density.

The ISL73847SLH also features a tri-level output that provides excellent protection against faults by driving a mid-scale voltage to signal the power stage to enter a Hi-Z condition.

The ISL73847SLH operates across the military temperature range from -55°C to +125°C and is available in a 24 Ld WSOIC (300 mils).

## Contents

<b>1. SEE Testing</b>	<b>3</b>
1.1 Objective	3
1.2 Facility	3
1.3 Setup	3
<b>2. Results</b>	<b>4</b>
2.1 Destructive Single Event Effects Data	4
2.2 Single Event Transient Data	7
<b>3. SEE Testing Summaries</b>	<b>9</b>
3.1 Destructive Single Event Effects	9
3.2 Single Event Transients	10
<b>4. Revision History</b>	<b>10</b>

# 1. SEE Testing

## 1.1 Objective

The testing was intended to find the limits of the pin voltages set by the onset of DSEE at a LET of 86MeV·cm<sup>2</sup>/mg normal incidence Gold (<sup>197</sup>Au). Additional testing was performed to identify and quantify SETs and SEFIs occurring on the output voltages. The irradiation for the SEE studies was completed with normal incidence Gold (<sup>197</sup>Au) at a LET of 86MeV·cm<sup>2</sup>/mg.

## 1.2 Facility

SEE testing was completed at the Texas A&M University (TAMU) Radiation Effects Facility of the Cyclotron Institute in College Station, Texas. This facility has a K500 superconducting cyclotron that can supply a wide range of ion species and flux. The testing referred to in this report was performed in April 2022 using the K500 cyclotron.

## 1.3 Setup

The ISL73847SLH was evaluated for SEE using a general-purpose engineering evaluation board that allowed the use of the 2-phase synchronous buck application configurations. The specific configurations changed with the type of testing. DSEE testing was performed using the 2-phase buck configuration operating at 500kHz. The SET testing was performed using the 2-phase buck configuration operating at 500kHz and 1000kHz.

The ISL73847SLH DUT (Device Under Test) irradiation setup is shown in [Figure 1](#). The ISL73847SLH was configured for 2-phase operation at two PWM frequencies, each of which used a different board assembly. The board assembly configured for the switching frequency of 500kHz and  $V_{OUT} = 1.0V$  used an  $L_{OUTX}$  of 1.0μH and  $C_{OUT}$  of 880μF (4x KEMET T530D227M010ATE006-T with maximum ESR of 6mΩ each) The compensation component values were  $R_{COMP} = 4.22k$ ,  $C_{COMP} = 10n$ ,  $C_{POLE} = 330pF$ ,  $R_{SLOPE} = 37.4k$ , and  $R_{DROOP} = 604Ω$ . The board assembly configured for the switching frequency of 1000kHz and  $V_{OUT} = 1.0V$  used a  $L_{OUTX}$  of 560nH. The rest of the components remained the same as for the 500kHz case.

The DSEE tests were performed on VDD, VCC, and ISENSE pins while monitoring the supply currents before and after irradiation. The VDD test started with VDD set to 23V, then VDD was incremented by 1V until the part exhibited permanent changes or until 25V was achieved. The VCC test started with VCC set to 6.1V, then VCC was incremented by 0.2V until the part exhibited permanent changes or until 6.7V was achieved. The ISENSE test started with  $V_{OUT} = ISENSE$  at 12V, then  $V_{OUT} = ISENSE$  was incremented by 0.5V until the part exhibited permanent changes or until 13V was achieved. The monitored parameters for the buck are listed in [Table 1](#).

**Table 1. Monitored Parameters and Failure Criteria for the ISL73847SLH DSEE Testing**

Parameter Monitored	Deviation from Pre SEE testing for the following parameters	Post SEE Testing Failure Criteria
Buck Output Voltage	$V_{OUT} = 1.0V$	±2%
Enable pin current	$I_{VENPG} = 2.2mA$	±25%
VDD Supply current	$I_{VDD} = 10mA$	±25%

During the SET testing, the VDD supply operated at both 4.5V and 13.2V. The PVIN supply also operated at 4.5V and 13.2V during the SET testing. Scope 1 was set to trigger on events where  $V_{OUT}$  exceeded the ±2% window for SET events. Scope 2 was set to trigger on PGOOD events at a threshold of 2.25V on both edges. For detailed test conditions, see [Table 5](#).

## 2. Results

### 2.1 Destructive Single Event Effects Data

The ISL73847SLH was tested for DSEE with normal incidence Gold ( $^{197}\text{Au}$ ) at LET of  $86\text{MeV}\cdot\text{cm}^2/\text{mg}$  and a case temperature of  $125^\circ\text{C} \pm 10^\circ\text{C}$ . The buck output of 1.0V was loaded to 5A..

Table 2 through Table 4 show a quick summary of the DSEE (including SEL) tests for the buck. Four devices were tested at  $86\text{MeV}\cdot\text{cm}^2/\text{mg}$  and passed with no DSEE to a fluence of  $1\text{E}7$  particles/ $\text{cm}^2$  on each of the four parts. DSEE testing on a DUT was terminated when either a device failure or a change in the bias current for the pin under test was observed.

During the VDD DSEE testing, the DUT was irradiated starting with an initial VDD voltage of 23V with 1V increments until 25V was reached. No DSEE was seen at 25V. The results of the DSEE test are summarized in the Table 2.

Table 2. DSEE Test Results for VDD<sup>[1][2][3][4]</sup>

Run	DUT	V <sub>DD</sub> (V)	V <sub>OUT</sub> (V)		I <sub>VENPG</sub> (mA)		I <sub>VDD</sub> (mA)	
			Pre (V)	Post (V)	Pre (mA)	Post (mA)	Pre (mA)	Post (mA)
400	1	23	0.980	0.98	2.1	2.06	10.03	10.04
401	1	24	0.979	0.98	2.2	2.24	10.04	10.60
402	1	25	0.980	0.98	2.4	2.42	10.06	10.09
403	2	23	0.980	0.98	2.1	2.05	9.10	10.02
404	2	24	0.984	0.98	2.2	2.23	10.02	10.02
405	2	25	0.983	0.99	2.4	2.42	10.03	10.03
406	3	23	0.971	0.97	2.1	2.05	9.92	9.94
407	3	24	0.971	0.97	2.2	2.22	9.94	9.94
408	3	25	0.970	0.97	2.4	2.41	9.94	9.94
409	4	23	0.982	0.99	2.1	2.06	9.88	9.89
410	4	24	0.985	0.99	2.2	2.24	9.89	9.94
411	4	25	0.985	0.99	2.4	2.42	9.94	9.93

1. L<sub>OUT</sub>/PHASE = 1 $\mu\text{H}$ , C<sub>OUT</sub>/PHASE = 440 $\mu\text{F}$ , SYNC1 = LOW, C<sub>VCC</sub> = 0.68 $\mu\text{F}$ , C<sub>SS</sub> = 22nF, R<sub>COMP</sub> = 4.22k, C<sub>COMP</sub> = 10nF, R<sub>PG</sub> = 5k, R<sub>SLOPE</sub> = 37.4k, EN = HIGH.
2. Switching Frequency set to 500kHz with R<sub>FS</sub> = 92.4k.
3. DUT Biasing: P<sub>VIN</sub> = 5V, V<sub>BUS</sub> = 6V, I<sub>OUT</sub> = 5A.
4. Normal Incidence Gold ( $^{197}\text{Au}$ ) at LET =  $86\text{MeV}\cdot\text{cm}^2/\text{mg}$  and  $125^\circ\text{C} \pm 10^\circ\text{C}$  Case Temperature, with a run fluence of  $1.00\text{E}+07$  particles/ $\text{cm}^2$ .

During the VCC DSEE testing, the DUT was irradiated starting with an initial VCC voltage of 6.1V with 0.2V increments until 6.7V was reached. No DSEE was seen at 6.7V. The results of the DSEE test are summarized in [Table 3](#).

**Table 3. DSEE Test Results for VCC [1][2][3][4]**

Run	DUT	VCC (V)	VOUT (V)		I_VENPG (mA)		I_VCC (mA)	
			Pre (V)	Post (V)	Pre (nA)	Post (nA)	Pre (mA)	Post (mA)
412	5	6.1	0.988	0.99	950.0	950.00	11.66	11.68
413	5	6.3	0.989	0.99	950.0	940.00	12.30	12.26
414	5	6.5	0.991	0.99	940.0	960.00	13.02	13.01
415	5	6.7	0.991	0.99	960.0	970.00	13.92	13.89
416	6	6.1	0.973	0.97	1100.0	1100.00	11.79	11.78
417	6	6.3	0.975	0.98	1100.0	1100.00	12.42	12.41
418	6	6.5	0.976	0.98	1100.0	1100.00	13.11	13.16
419	6	6.7	0.973	0.97	1100.0	1100.00	14.05	14.04
420	7	6.5	0.974	0.97	1200.0	1200.00	13.07	13.07
421	7	6.7	0.970	0.97	1200.0	1200.00	13.96	13.94
422	8	6.5	0.987	0.99	600.0	600.00	13.05	13.02
423	8	6.7	0.986	0.99	600.0	600.00	13.91	13.88

1.  $I_{OUT}/PHASE = 1\mu H$ ,  $C_{OUT}/PHASE = 440\mu F$ ,  $SYNCl = LOW$ ,  $C_{VCC} = 0.68\mu F$ ,  $C_{SS} = 22nF$ ,  $R_{COMP} = 4.22k$ ,  $C_{COMP} = 10nF$ ,  $R_{PG} = 5k$ ,  $R_{SLOPE} = 37.4k$ ,  $EN = HIGH$ .
2. Switching Frequency set to 500kHz with  $R_{FS} = 92.4k$ .
3. DUT Biasing:  $V_{DD} = V_{CC}$ ,  $PVIN = 5V$ ,  $V_{BUS} = 6V$ ,  $I_{OUT} = 5A$ .
4. Normal Incidence Gold ( $^{197}Au$ ) at LET = 86MeV·cm<sup>2</sup>/mg and 125°C ±10°C Case Temperature, with a run fluence of 1.00E+07particles/cm<sup>2</sup>.

During the ISENSE common-mode voltage DSEE testing, the DUT was irradiated starting with an initial  $V_{OUT}$  of 12V, which was incremented by 0.5V until 13.0V was reached. No DSEEs were observed when  $V_{OUT}$  was 12V on four devices. One device experienced a failure unrelated to ISENSE at 12.5V. The DSEE test setup had a scope set to monitor the  $V_{OUT}$  during the test. A few SEFI were observed at an ISENSE voltage of 12V. It should be noted that the SEFI characterization is only done during the SET testing. However, to determine the ISENSE threshold at which no SEFI are seen we tested a derivative device with the same ISENSE structure and found that the no SEFIs were observed at ISENSE = 10V and below. The results of the DSEE test are summarized in [Table 4](#).

**Table 4. DSEE Test Results for ISENSE[1][2][3][4]**

Run	DUT	$V_{OUT}$ (V)	$V_{OUT}$ (V)		I_VDD (mA)	
			Pre	Post	Pre	Post
424	9	12.0	12.068	12.080	48.000	48.000
425	9	12.5	12.570	0.000	48.500	48.000
426	10	12.0	11.985	12.010	47.700	48.000

Table 4. DSEE Test Results for ISENSE<sup>[1][2][3][4]</sup> (Cont.)

Run	DUT	V <sub>OUT</sub> (V)	V <sub>OUT</sub> (V)		I <sub>VDD</sub> (mA)	
			Pre	Post	Pre	Post
427	10	12.5	12.584	12.564	48.000	48.000
428	10	13.0	13.051	13.043	48.000	48.000
429	11	12.0	11.990	11.990	48.000	48.000
430	11	12.5	12.590	12.610	48.000	48.000
431	11	13.0	12.990	13.020	49.000	49.000
432	12	12.0	12.000	12.001	47.000	48.000
433	12	12.5	12.502	12.540	48.000	48.000
434	12	13.0	13.040	12.050	48.000	48.000

1. L<sub>OUT</sub>/PHASE = 10μH, C<sub>OUT</sub>/PHASE = 100μF, SYNC1 = LOW, C<sub>VCC</sub> = 0.68μF, C<sub>SS</sub> = 22nF, R<sub>COMP</sub> = 4.22k, C<sub>COMP</sub> = 10nF, R<sub>PG</sub> = 5k, R<sub>SLOPE</sub> = 37.4k, EN = HIGH.
2. Switching Frequency set to 500kHz with R<sub>FS</sub> = 92.4k.
3. DUT Biasing: V<sub>DD</sub> = V<sub>CC</sub> = 5V, P<sub>VIN</sub> = 25V, V<sub>BUS</sub> = 6V, I<sub>OUT</sub> = 5A.
4. Normal Incidence Gold (<sup>197</sup>Au) at LET = 86MeV·cm<sup>2</sup>/mg and 125°C ±10°C Case Temperature, with a run fluence of 1.00E+07particles/cm<sup>2</sup>.

Both before and after irradiation three parameters (Table 1) were monitored to look for signs of DSEE. Table 2 through Table 4 show the results of DSEE testing for the device. Failures to the criteria at the top of the columns are indicated with a reduced sample count. For example with ISENSE = 12V, it had 4 of 4 devices passing; however, with ISENSE = 12.5V, 3 of 4 devices passed. The failed device did not show any change in the supply current; however, the V<sub>OUT</sub> post radiation had no output voltage

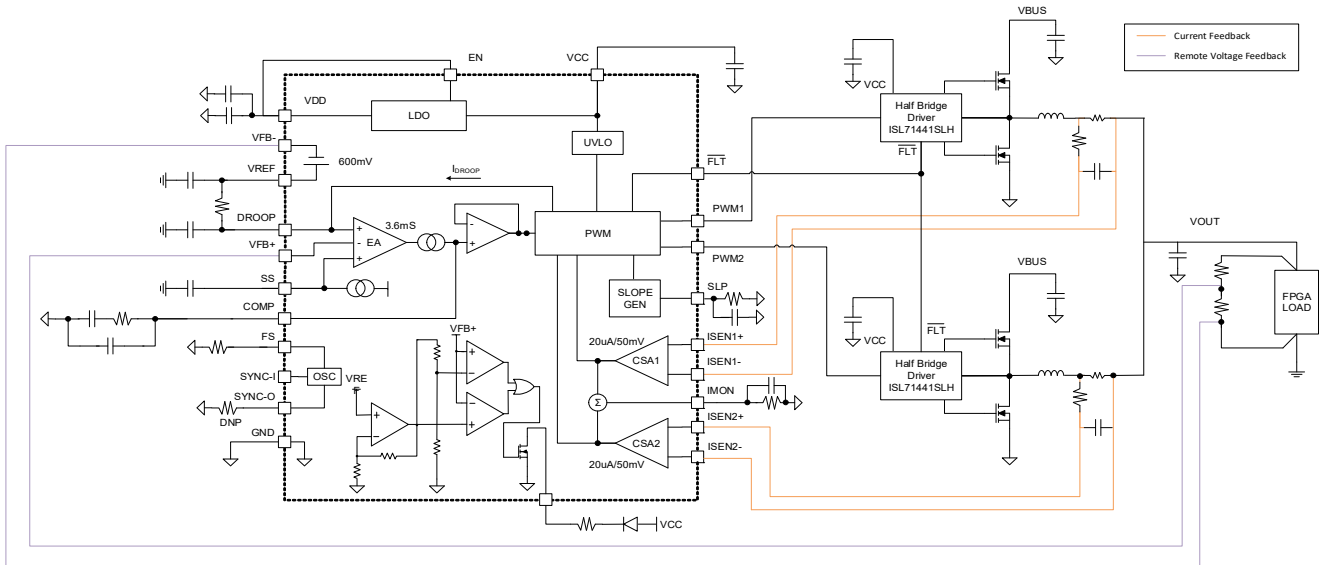


Figure 1. ISL73847SLH DUT SEE Irradiation Setup

## 2.2 Single Event Transient Data

The SET testing was performed on two devices at a  $f_{SW}$  of 500kHz and another two at an  $f_{SW}$  of 1000kHz. Each of the device runs were irradiated with normal incidence Gold ( $^{197}\text{Au}$ ) for a LET of  $86\text{MeV}\cdot\text{cm}^2/\text{mg}$  to a fluence of  $1\text{E}7\text{particle}/\text{cm}^2$ . The results of the tests performed for various conditions are in [Table 5](#).

**Table 5. SET Test Results** [1][2][3][4]

Run	Switching Frequency (kHz)	DUT	$V_{DD}$ (V)	$P_{VIN}$ (V)	$V_{OUT}$ Pre RAD (V)	$L_{OUT}$ ( $\mu\text{H}$ )	Scope1 CH1 = $V_{OUT}$ , Trigger $\pm 20\text{mV}$	Scope2 CH1 = PG, Trigger $\uparrow\downarrow 2.25\text{V}$
							SET	SEFI
401	500	20	4.5	5.0	0.991	1.0	0	0
402	500	20	4.5	13.2	0.991	1.0	0	0
403	500	20	13.2	13.2	0.991	1.0	0	0
404	500	20	13.2	5.0	0.991	1.0	0	0
406	500	21	4.5	5.0	0.991	1.0	0	0
407	500	21	4.5	13.2	0.991	1.0	0	0
408	500	21	13.2	13.2	0.989	1.0	0	0
409	500	21	13.2	5.0	0.989	1.0	0	0
410	1000	30	4.5	5.0	0.992	0.56	0	0
411	1000	30	13.2	5.0	0.991	0.56	0	0
412	1000	31	4.5	5.0	0.989	0.56	0	0
413	1000	31	13.2	5.0	0.988	0.56	1	0

- $C_{OUT}/\text{PHASE} = 440\mu\text{F}$ ,  $\text{SYNCl} = \text{LOW}$ ,  $C_{VCC} = 0.68\mu\text{F}$ ,  $C_{SS} = 22\text{nF}$ ,  $R_{COMP} = 4.22\text{k}$ ,  $C_{COMP} = 10\text{nF}$ ,  $R_{PG} = 5\text{k}$ ,  $R_{SLOPE} = 37.4\text{k}$ ,  $\text{EN} = \text{HIGH}$ .
- Switching Frequency set to 500kHz with  $R_{FS} = 92.4\text{k}$  and to 1000kHz with  $R_{FS} = 35.7\text{k}$ .
- DUT Biasing:  $V_{BUS} = 6\text{V}$ ,  $I_{OUT} = 5\text{A}$ .
- Normal Incidence Gold ( $^{197}\text{Au}$ ) at  $\text{LET} = 86\text{MeV}\cdot\text{cm}^2/\text{mg}$  and  $125^\circ\text{C} \pm 10^\circ\text{C}$  Case Temperature, with a run fluence of  $1.00\text{E}+07\text{particles}/\text{cm}^2$ .

Figure 2 and Figure 3 show SET captures by backing down the  $\pm 20\text{mV}$  windows to  $\pm 8\text{mV}$  during the DSEE test at  $125^\circ\text{C}$ . No captures however were seen at  $500\text{kHz}$  during the SET testing at  $25^\circ\text{C}$  with a  $\pm 20\text{mV}$  window trigger on  $V_{\text{OUT}}$ .

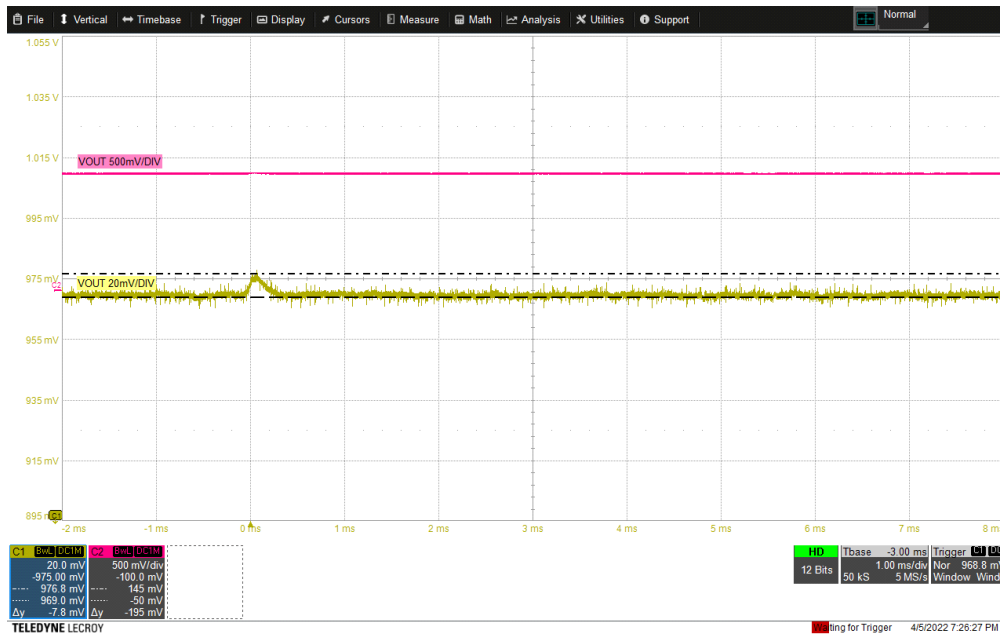


Figure 2.  $V_{\text{OUT}}$  SET =  $\pm 8\text{mV}$  during  $V_{\text{DD}} = 25\text{V}$  DSEE Test

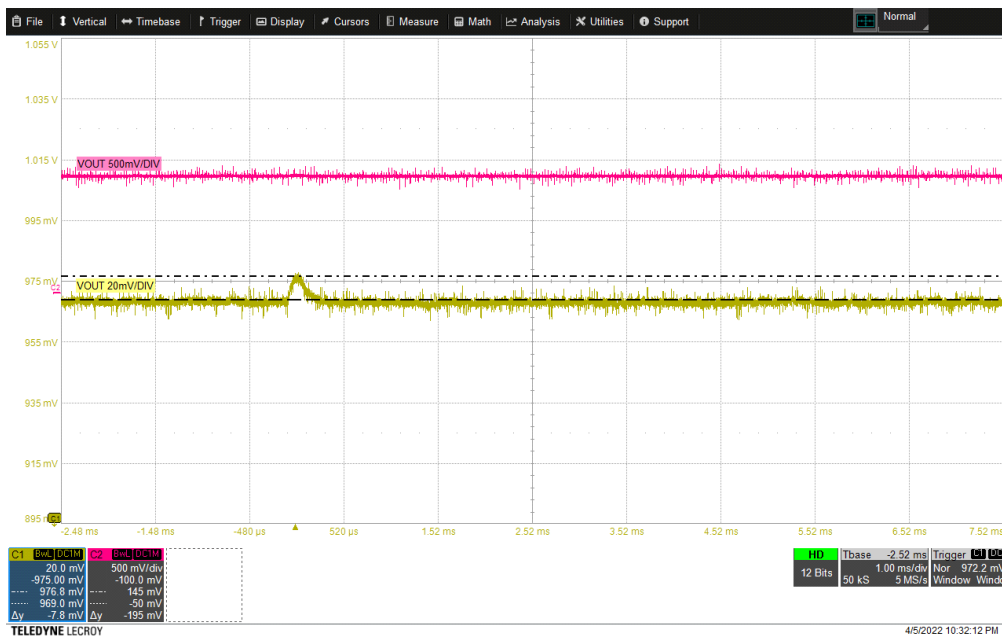


Figure 3.  $V_{\text{OUT}}$  SET =  $\pm 8\text{mV}$  during  $V_{\text{CC}} = 6.7\text{V}$  DSEE Test



Figure 4, shows the missing pulse on PWM2 captured during the test run 413. The signals monitored during the test were:

- PWM1 and PWM2 the drive signals.
- VREF the voltage reference (0.6V).
- SYNC-O is the output of the internal oscillator clock.
- COMP is the output of the error amplifier.
- DROOP the reference voltage to the error amplifier which is modulated in proportion to the current sensed by the controller.

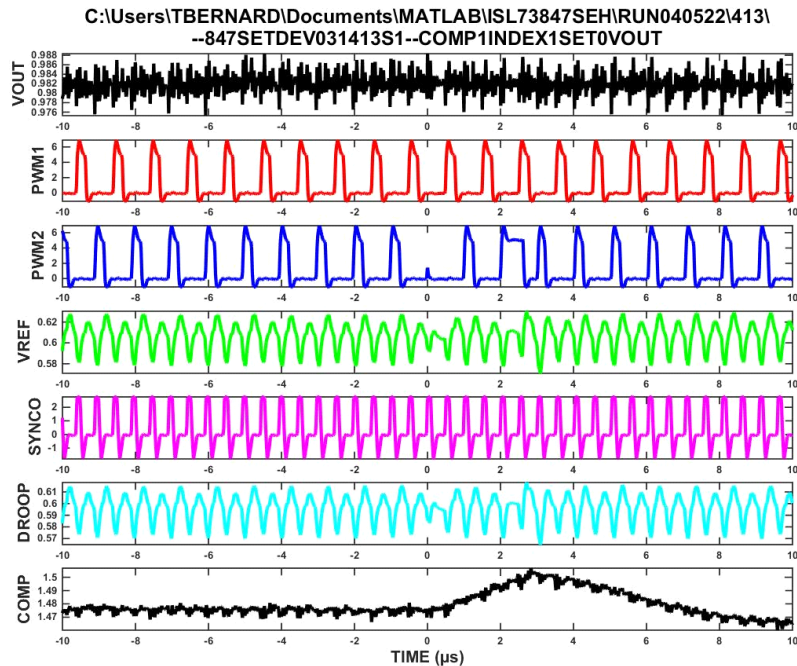


Figure 4. SET, LET86,  $f_{SW} = 1\text{MHz}$ , trigger  $V_{OUT} \pm 20\text{mV}$

### 3. SEE Testing Summaries

#### 3.1 Destructive Single Event Effects

DSEEs including SEL were tested with Gold ( $^{197}\text{Au}$ ) at a LET of  $86\text{MeV}\cdot\text{cm}^2/\text{mg}$  to a Fluence of  $1\text{E}7\text{particles}/\text{cm}^2$  and a temperature of  $125^\circ\text{C}$ , for various values of VDD and VCC. The board assembly used a  $L_{OUTx}$  of  $1.0\mu\text{H}$  and  $C_{OUT}$  of  $880\mu\text{F}$  (4x KEMET T530D227M010ATE006-T with a maximum ESR of  $6\text{m}\Omega$  each). The compensation component values were set at  $R_{COMP} = 4.22\text{k}$ ,  $C_{COMP} = 10\text{n}$ ,  $C_{POLE} = 330\text{pF}$ ,  $R_{SLOPE} = 37.4\text{k}$ , and  $R_{DROOP} = 604\Omega$ .

The  $V_{OUT}$  of  $1\text{V}$  was loaded to  $5\text{A}$ . The VDD and VCC voltages were varied for the respective DSEE tests. Results of the individual tests are that:

- No DSEE including SEL were observed  $V_{DD} = 25\text{V}$  to a fluence of  $1\text{E}7\text{ particles}/\text{cm}^2$  on each of the four units.
- No DSEE including SEL were observed  $V_{CC} = 6.7\text{V}$  to a fluence of  $1\text{E}7\text{ particles}/\text{cm}^2$  on each of the four units.

DSEEs including SEL were tested with Gold ( $^{197}\text{Au}$ ) to a LET of  $86\text{MeV}\cdot\text{cm}^2/\text{mg}$  at a temperature of  $125^\circ\text{C}$  and various values of ISENSE. The board assembly used a  $L_{OUTx}$  of  $10\mu\text{H}$  and  $C_{OUT}$  of  $200\mu\text{F}$  (2x KEMET T521X107M025ATE030 with a maximum ESR of  $30\text{m}\Omega$  each). The compensation component values were set at  $R_{COMP} = 4.22\text{k}$ ,  $C_{COMP} = 47\text{n}$ ,  $C_{POLE} = 330\text{pF}$ ,  $R_{SLOPE} = 76.8\text{k}$ ,  $R_{DROOP} = 0\Omega$ . An incremental voltage was

applied to the VB+ node to vary the  $V_{OUT}$  starting at 12V and thereby the common-mode voltage on the ISENSE pin.

- No SEFI seen at ISENSE = 10V. SEFI was observed at the ISENSE voltage of 12V. To determine the threshold for ISENSE at which no SEFI were seen, we tested a derivative device with the same ISENSE structure. It was found that the no SEFI was observed at ISENSE = 10V.

### 3.2 Single Event Transients

The SEE Testing for the ISL73847SLH was performed at TAMU. The DUT was configured for a switching frequency of 500kHz and was tested for SETs with Gold ( $^{197}\text{Au}$ ) at a LET of  $86\text{MeV}\cdot\text{cm}^2/\text{mg}$  to a fluence of  $1\text{E}7\text{particles}/\text{cm}^2$ . The board assembly used a  $L_{OUTx}$  of  $1.0\mu\text{H}$  and  $C_{OUT}$  of  $880\mu\text{F}$  (4x KEMET T530D227M010ATE006-T with a maximum ESR of  $6\text{m}\Omega$  each) The compensation component values were set at  $R_{COMP} = 4.22\text{k}$ ,  $C_{COMP} = 10\text{n}$ ,  $C_{POLE} = 330\text{pF}$ ,  $R_{SLOPE} = 37.4\text{k}$ , and  $R_{DROOP} = 604\Omega$ . The DUT VDD was biased at 4.5V and 13.2V, and the PVIN was biased at 5V and 13.2V. The  $V_{OUT}$  of 1V was loaded to 5A. The SET trigger capture window was set to  $\pm 20\text{mV}$  ( $\pm 2\%$ ) for  $V_{OUT} = 1.0\text{V}$ . The observation was that no SET was captured at a Fluence of  $1\text{E}7\text{ particles}/\text{cm}^2$  on each of the four parts.

The DUT configured for a switching frequency of 1000kHz was tested for SETs with Gold ( $^{197}\text{Au}$ ) at an LET of  $86\text{MeV}\cdot\text{cm}^2/\text{mg}$  to a fluence of  $1\text{E}7\text{particles}/\text{cm}^2$ . The board assembly used a  $L_{OUTx}$  of  $0.56\mu\text{H}$  and  $C_{OUT}$  of  $880\mu\text{F}$  (4x KEMET T530D227M010ATE006-T with a maximum ESR of  $6\text{m}\Omega$  each) The compensation component values were set the same as the 500kHz case. The DUT VDD was biased at 4.5V and 13.2V, and the PVIN was biased at 5V and 13.2V. The  $V_{OUT}$  of 1V was loaded to 5A. The SET trigger capture window was set to  $\pm 20\text{mV}$  ( $\pm 2\%$ ) for  $V_{OUT} = 1.0\text{V}$ . The observation was that a single SET event was captured at a Fluence of  $1\text{E}7\text{ particles}/\text{cm}^2$  on run 413. See [Table 5](#) and [Figure 4](#) for more details. The missing pulse was observed on PWM2, while PWM1 was normal. The trigger event was noise spike at the trigger point, the  $V_{OUT}$  did not show movement in the  $\pm 20\text{mV}$  window. It should be noted that the conditions for run 411 were the same as that of 413 and we did not observe an SET event.

Based on CRÈME simulations for a GEO orbit, statistically speaking, the part would expect to experience a particle with  $\text{LET} \geq 86\text{MeV}\cdot\text{cm}^2/\text{mg}$  once about every 58000 years. In a typical LEO, it would be about once every 2 million years.

## 4. Revision History

Revision	Date	Description
1.00	Dec 16, 2024	Initial release.

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).