ISL7457SRH

Low Dose Rate Total Dose Testing of the ISL7457SRH Quad CMOS Driver

Introduction

This report provides results of a Low Dose Rate (LDR) total ionizing dose (TID) test of the ISL7457SRH radiation hardened non-inverting quad CMOS driver. The test was conducted to determine the sensitivity of the part to LDR irradiation and to determine if the part displays bias sensitivity in that environment. The ISL7457SRH does not have a corresponding -EH version and is lot acceptance tested (RLAT) at High Dose Rate (HDR) only. The present LDR data was developed in 2014 and used small sample sizes; it is provided for guidance only as the part is not specified for LDR performance. The dose rate used for this test was 0.01rad(Si)/s.

Related Literature

For a full list of related documents, visit our website:

- MIL-STD-883 test method 1019
- ISL7457SRH datasheet
- DLA Standard Microcircuit Drawing (SMD) 5962-08230

Contents

1. Product Description

The ISL7457SRH is a total dose and SEE hardened non-inverting quad CMOS driver. It is capable of running at clock rates up to 40MHz and features 2A typical peak drive capability and a nominal ON-resistance of 3.5Ω. The ISL7457SRH is ideal for driving highly capacitive loads such as storage and vertical clocks in CCD applications and is also well suited for level-shifting and clock-driving applications.

Each of the four ISL7457SRH outputs can be independently switched to either the high (VH) or low (VL) supply pin, depending on the logic state of the related input pin. The inputs are compatible with both 3.3V and 5V CMOS logic. The Output Enable (OE) pin can put the outputs into a high-impedance state. This is especially useful in CCD applications that disable the driver during power-down. The ISL7457SRH also features fast rise and fall times, which are typically matched to within 1ns. The propagation delay is also matched between rising and falling edges to typically within 1.5ns. Figure 1 provides a functional diagram.

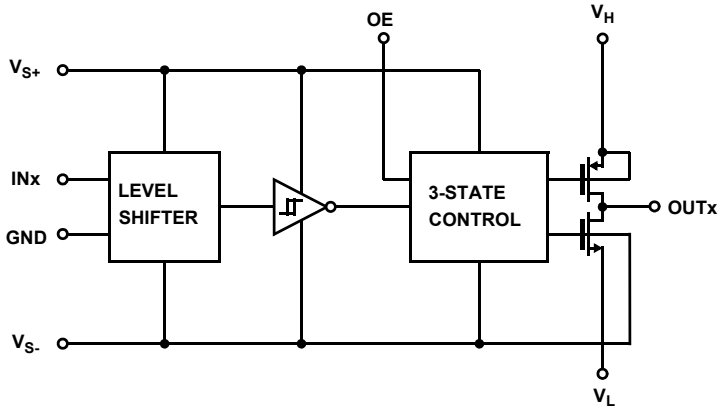

Figure 1. ISL7457SRH Functional Diagram

The ISL7457SRH is radiation hardened to a TID rating of 10krad(Si) at HDR (50 – 300rad(Si)/s) only. This document reports limited TID response data for 15krad(Si) at LDR for the biased and unbiased cases, with the 15krad(Si) level representing an overtest. The ISL7457SRH is acceptance tested on a wafer-by-wafer basis to 10krad(Si) at HDR only.

The part has also been tested for single-event effects (SEE), see the ISL7457SRH device page for the applicable report.

The ISL7457SRH is implemented in a commercial CMOS process and is available in a 16 Ld hermetic ceramic flatpack or in die form. The part is specified across the military temperature range of -55°C to +125°C.

2. Test Description

2.1 Irradiation Facilities

LDR testing used a J. L. Shepherd and Associates Model 484 research-type LDR irradiator located in the Renesas Palm Bay, FL facility. The irradiations were performed at 0.010rad(Si)/s per MIL-STD-883 Method 1019. The Model 484 has a limited interaction volume and the sample sizes that can be accommodated are similarly limited.

2.2 Test Fixturing

Figure 2 shows the configuration used for biased low and HDR irradiation and anneal. **Note:** The supply voltage VS is +15V, R_1 = 15kΩ, R_2 = 10kΩ and C_1 = 100nF

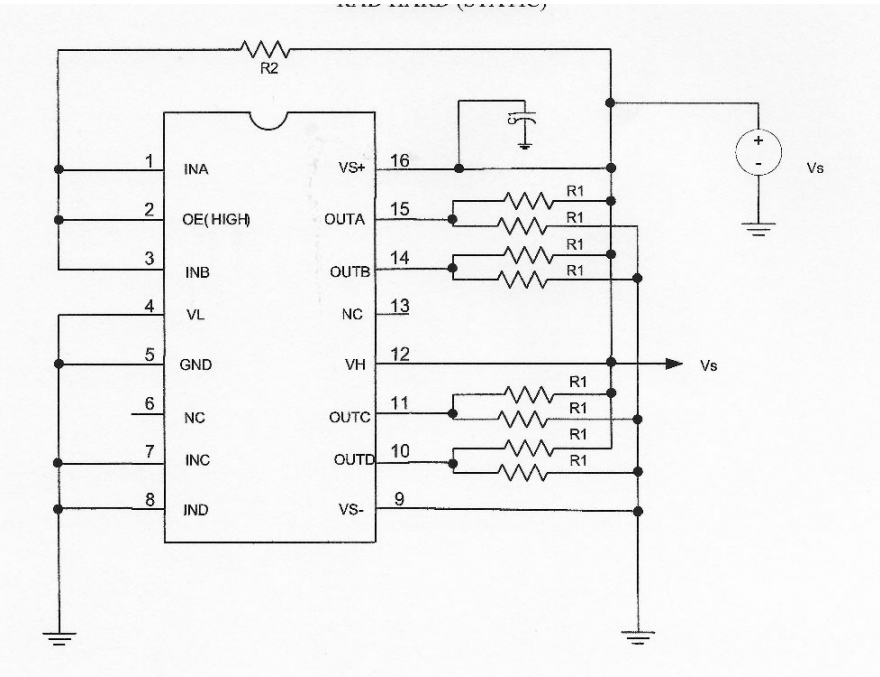

Figure 2. Irradiation Bias Configuration Used for the ISL7457SRH

2.3 Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using production automated test equipment (ATE) with data logging at each downpoint. Downpoint electrical testing was performed at room temperature. Three control units were used to ensure repeatable data.

2.4 Experimental Matrix

Testing proceeded in accordance with MIL-STD-883 Test Method 1019. The experimental matrix consisted of two samples irradiated at LDR with all pins grounded and two samples irradiated at LDR under bias. Samples of the ISL7457SRH were packaged in production 16 Ld ceramic flatpacks and were processed through the standard burn-in screens before irradiation, as required by MIL-STD-883. Samples were screened to the SMD 5962-08230 limits at room, low, and high temperature before the start of total dose testing.

2.5 Downpoints

The downpoints for both sample groups were 0krad(Si), 10krad(Si), and 15krad(Si).

3. Results

Total dose testing of the ISL7457SRH showed no reject devices to the SMD post-radiation limits after 10krad(Si), which is the SMD total dose specification. After 15krad(Si) both biased irradiation samples failed the positive output leakage parameter; as the ATE test program was inadvertently set to stop on first fail no further electrical data exists for these two samples.

3.1 Attributes Data

Table 1. Attributes Data

Part	Dose Rate (rad(Si)/s)	Bias	Sample Size	Downpoint	Pass[1]	Fail
ISL7457SRH	0.01	Biased	2	Pre-irradiation	2	0
				10krad(Si)	2	0
				15krad(Si)	0	2
ISL7457SRH	0.01	Grounded	2	Pre-irradiation	2	0
				10krad(Si)	2	0
				15krad(Si)	2	0

1. A pass indicates a sample that passes all SMD limits.

3.2 Variables Data

Figure 3 through Figure 18 show the total dose response of selected DC and AC parameters at all downpoints. The plots show the average as a function of total dose for each of the two irradiation conditions.

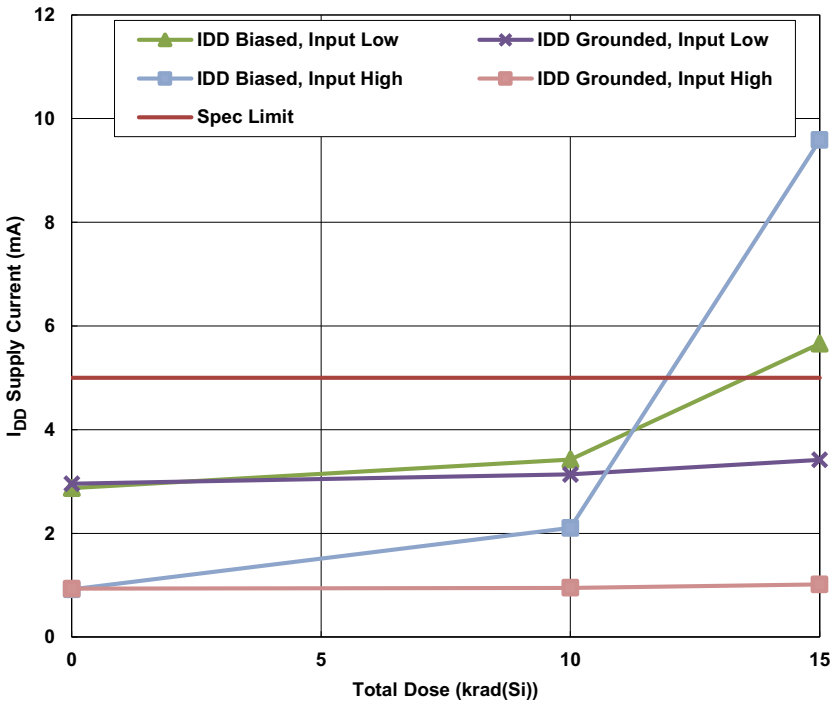

Figure 3. ISL7457SRH quad CMOS driver positive power supply current at 5V supply, input low and high cases, as a function of LDR total dose irradiation for the unbiased (grounded) and biased cases. The dose rate was 0.01rad(Si)/s. Sample sizes were two each for the unbiased and biased groups. The post-radiation SMD limit is 5mA maximum.

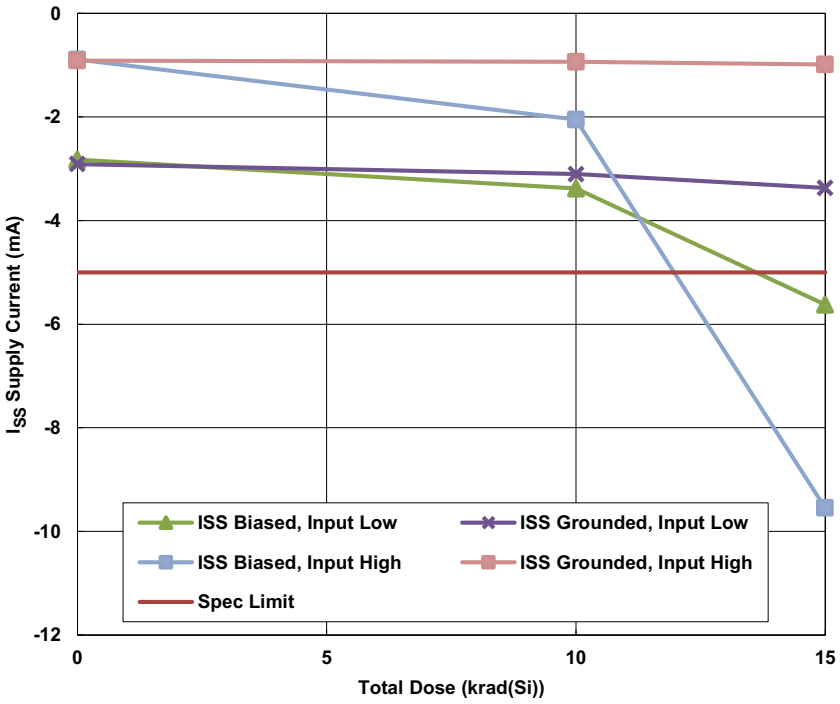

Figure 4. ISL7457SRH quad CMOS driver negative power supply current at 5V supply, input low and high cases, as a function of LDR total dose irradiation for the unbiased (grounded) and biased cases. The dose rate was 0.01rad(Si)/s. Sample sizes were two each for the unbiased and biased groups. The post-radiation SMD limit is -5mA minimum.

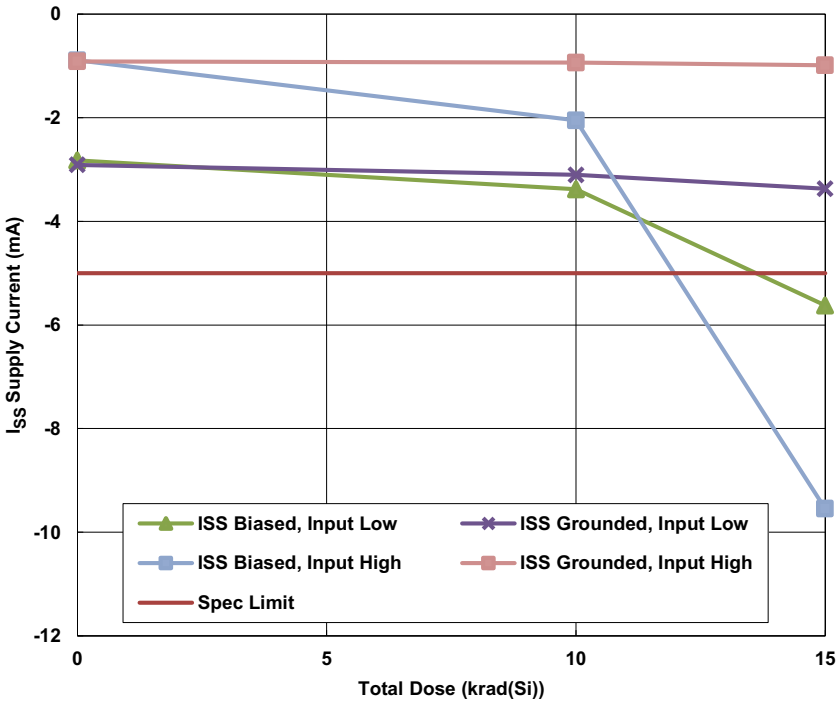

Figure 5. ISL7457SRH quad CMOS driver positive output leakage current at 16.5V supply as a function of LDR total dose irradiation for the unbiased (grounded) and biased cases. The dose rate was 0.01rad(Si)/s. Sample sizes were two each for the unbiased and biased groups. The post-radiation SMD limit is 1.2mA maximum.

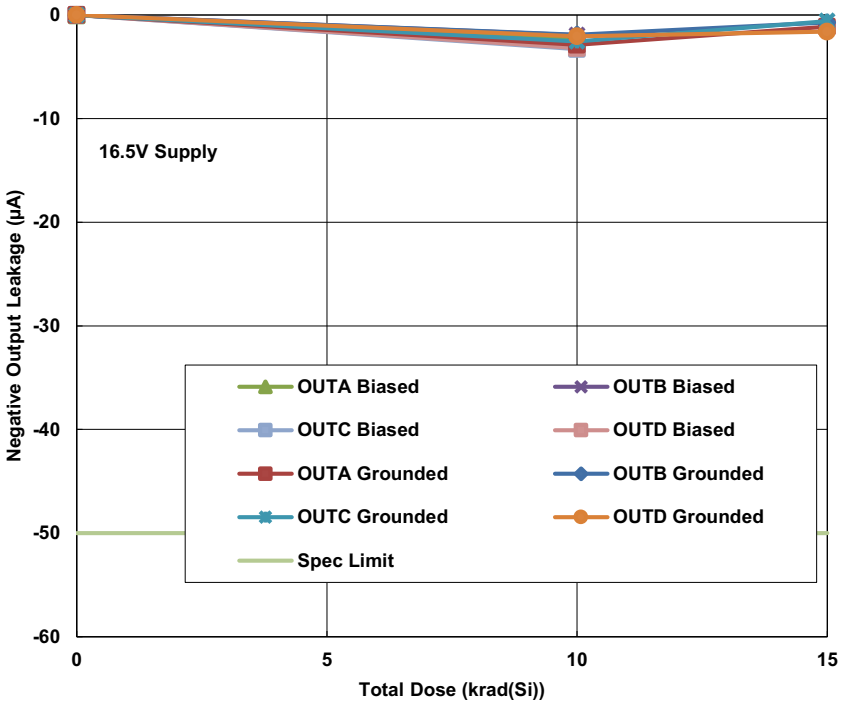

Figure 6. ISL7457SRH quad CMOS driver negative output leakage current at 16.5V supply as a function of LDR total dose irradiation for the unbiased (grounded) and biased cases. The dose rate was 0.01rad(Si)/s. Sample sizes were two each for the unbiased and biased groups. The post-radiation SMD limit is -50µA minimum.

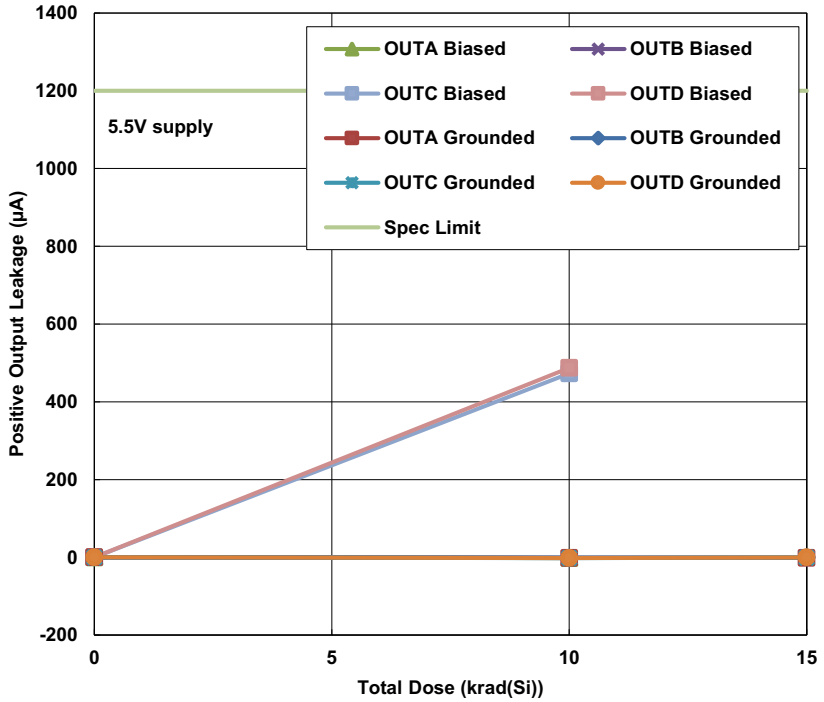

Figure 7. ISL7457SRH quad CMOS driver positive output leakage current at 5V supply as a function of LDR total dose irradiation for the unbiased (grounded) and biased cases. The dose rate was 0.01rad(Si)/s. Sample sizes were two each for the unbiased and biased groups. The post-radiation SMD limit is 1.2mA maximum.

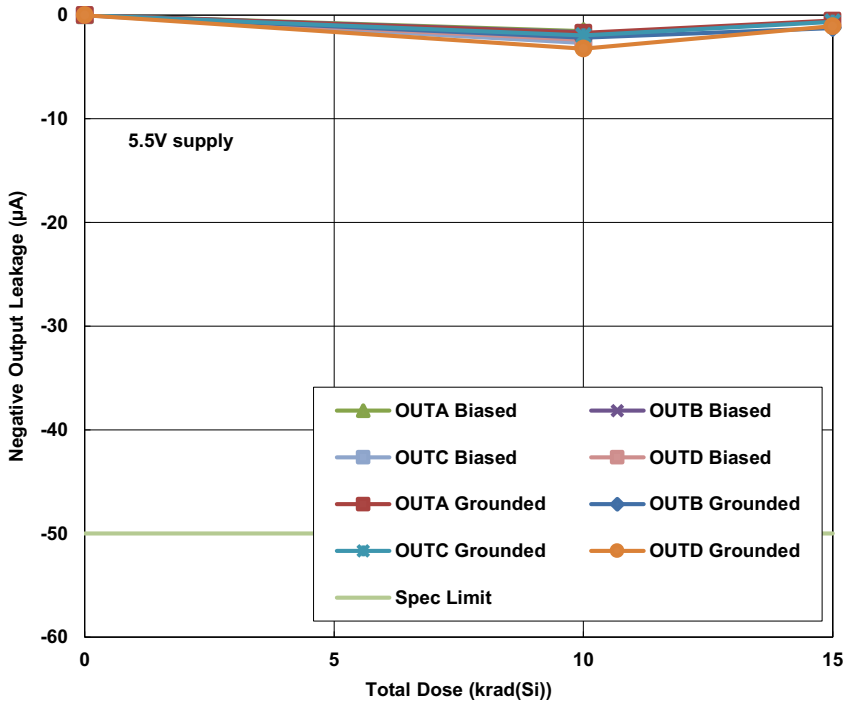

Figure 8. ISL7457SRH quad CMOS driver negative output leakage current at 5V supply as a function of LDR total dose irradiation for the unbiased (grounded) and biased cases. The dose rate was 0.01rad(Si)/s. Sample sizes were two each for the unbiased and biased groups. The post-radiation SMD limit is -50µA minimum.

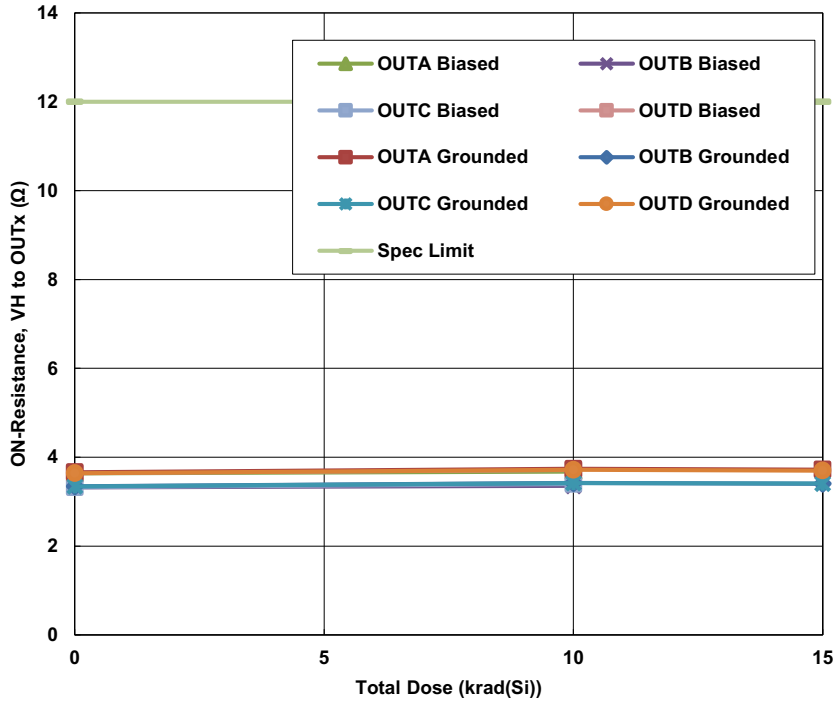

Figure 9. ISL7457SRH quad CMOS driver ON-resistance, VH to OUTx at 5V supply, as a function of LDR total dose irradiation for the unbiased (grounded) and biased cases. The dose rate was 0.01rad(Si)/s. Sample sizes were two each for the unbiased and biased groups. The post-radiation SMD limit is 12Ω maximum.

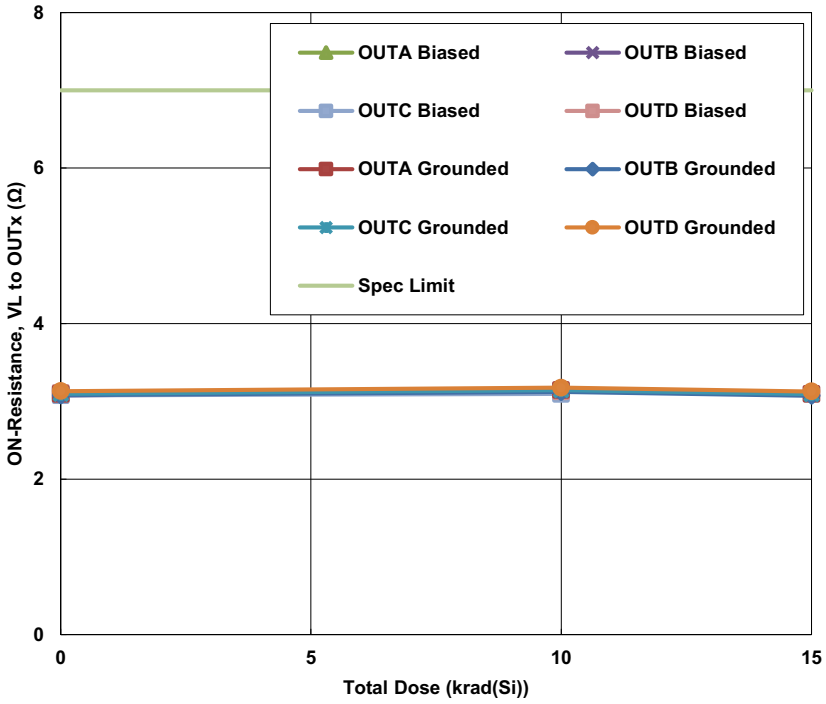

Figure 10. ISL7457SRH quad CMOS driver ON-Resistance, VL to OUTx at 5V supply, as a function of LDR total dose irradiation for the unbiased (grounded) and biased cases. The dose rate was 0.01rad(Si)/s. Sample sizes were two each for the unbiased and biased groups. The post-radiation SMD limit is 7Ω maximum.

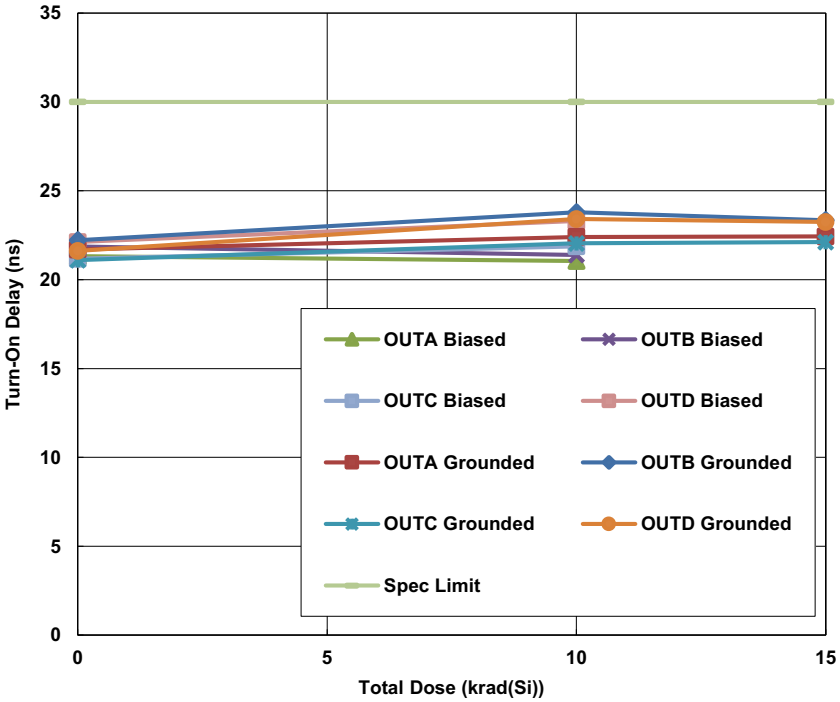

Figure 11. ISL7457SRH quad CMOS driver turn-on delay time at 5V supply as a function of LDR total dose irradiation for the unbiased (grounded) and biased cases. The dose rate was 0.01rad(Si)/s. Sample sizes were two each for the unbiased and biased groups. The post-radiation SMD limit is 30ns maximum.

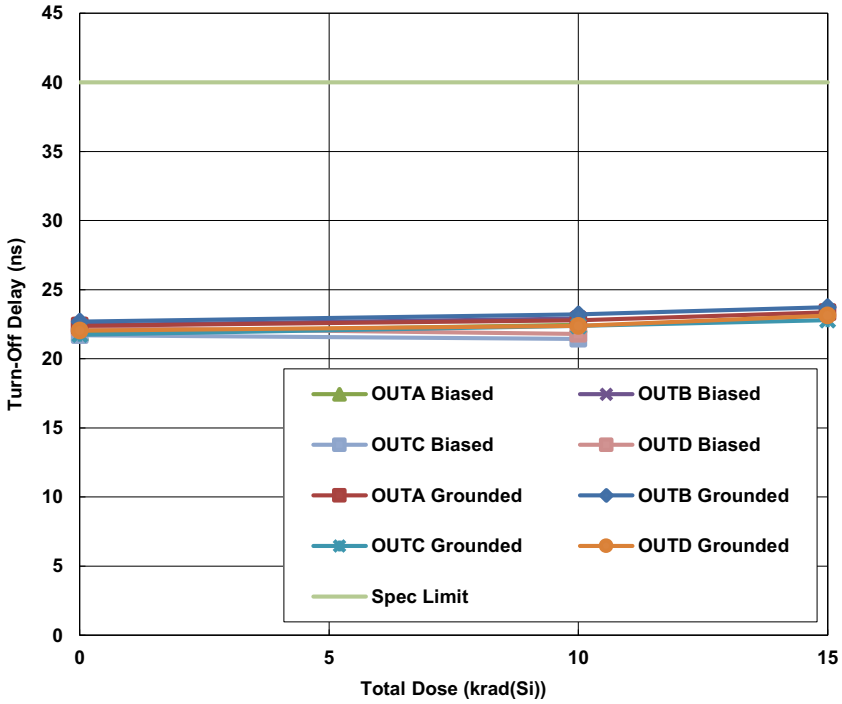

Figure 12. ISL7457SRH quad CMOS driver turn-off delay time at 5V supply as a function of LDR total dose irradiation for the unbiased (grounded) and biased cases. The dose rate was 0.01rad(Si)/s. Sample sizes were two each for the unbiased and biased groups. The post-radiation SMD limit is 40ns maximum.

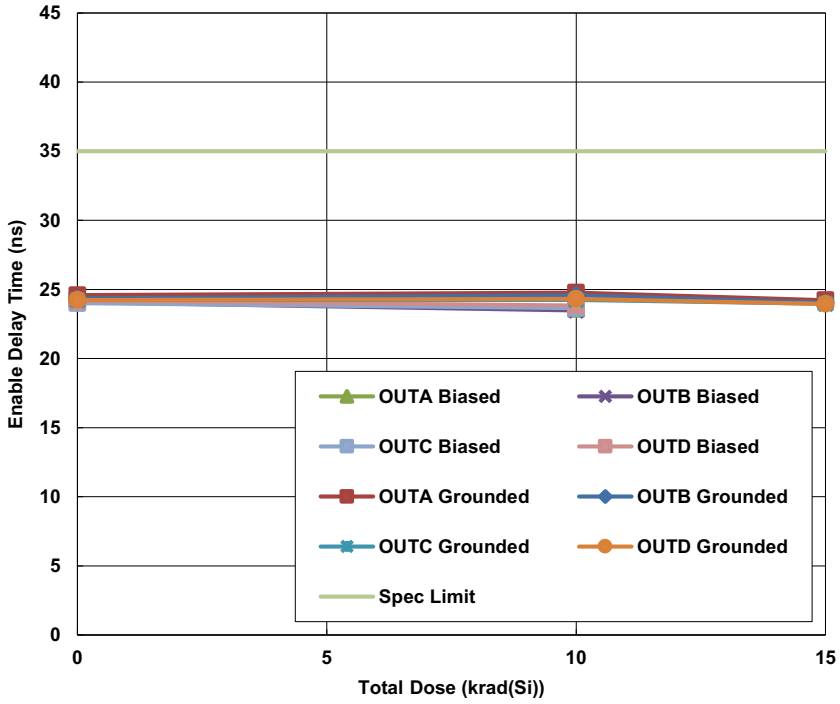

Figure 13. ISL7457SRH quad CMOS driver enable delay time at 5V supply as a function of LDR total dose irradiation for the unbiased (grounded) and biased cases. The dose rate was 0.01rad(Si)/s. Sample sizes were two each for the unbiased and biased groups. The post-radiation SMD limit is 35ns maximum.

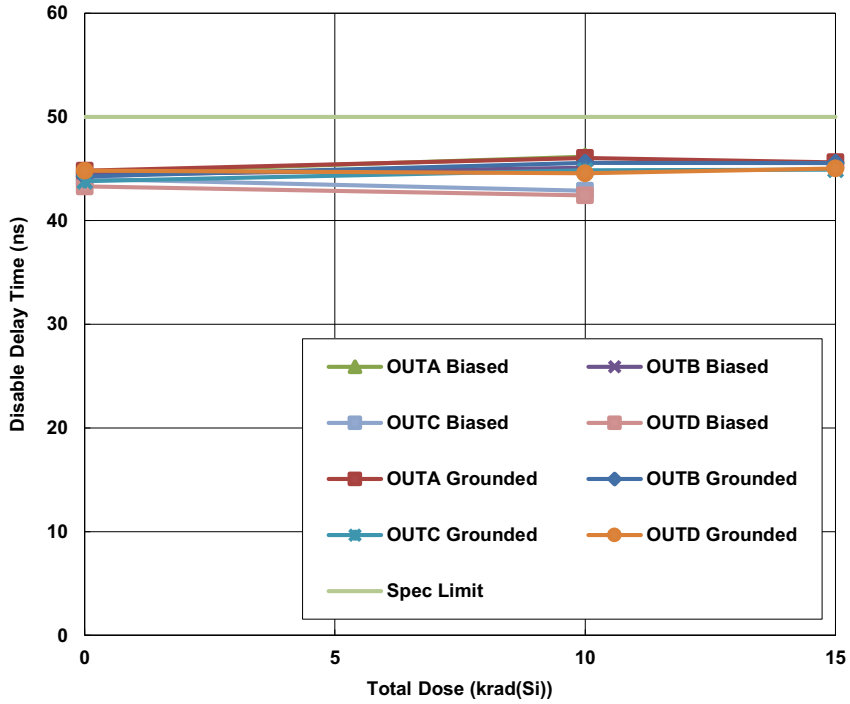

Figure 14. ISL7457SRH quad CMOS driver disable delay time at 5V supply as a function of LDR total dose irradiation for the unbiased (grounded) and biased cases. The dose rate was 0.01rad(Si)/s. Sample sizes were two each for the unbiased and biased groups. The post-radiation SMD limit is 50ns maximum.

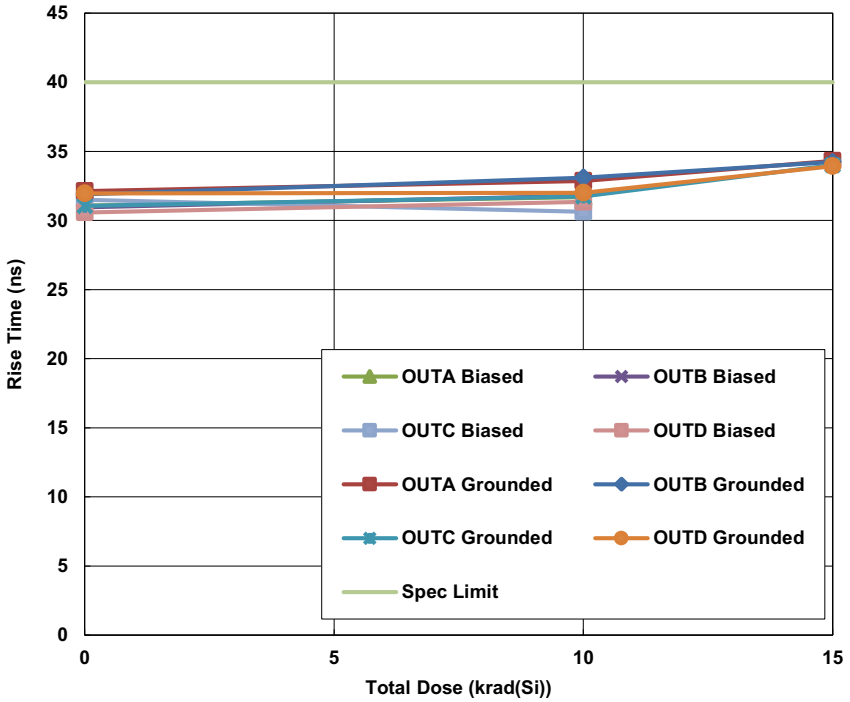

Figure 15. ISL7457SRH quad CMOS driver rise time at 5V supply as a function of LDR total dose irradiation for the unbiased (grounded) and biased cases. The dose rate was 0.01rad(Si)/s. Sample sizes were two each for the unbiased and biased groups. The post-radiation SMD limit is 40ns maximum.

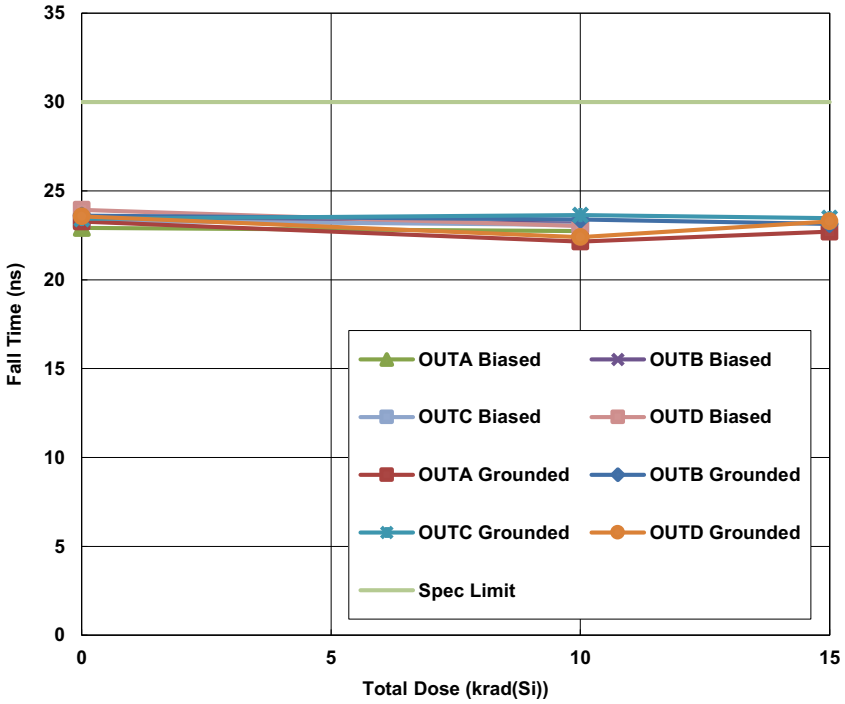

Figure 16. ISL7457SRH quad CMOS driver fall time at 5V supply as a function of LDR total dose irradiation for the unbiased (grounded) and biased cases. The dose rate was 0.01rad(Si)/s. Sample sizes were two each for the unbiased and biased groups. The post-radiation SMD limit is 30ns maximum.

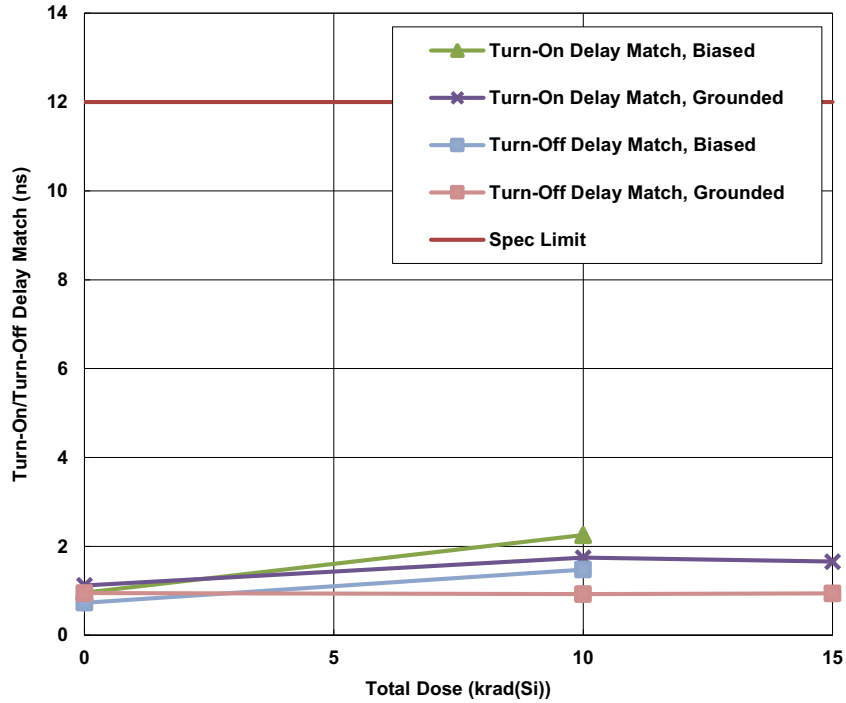

Figure 17. ISL7457SRH quad CMOS driver turn-on and turn-off delay match at 5V supply as a function of LDR total dose irradiation for the unbiased (grounded) and biased cases. The dose rate was 0.01rad(Si)/s. Sample sizes were two each for the unbiased and biased groups. The post-radiation SMD limit is 12ns maximum.

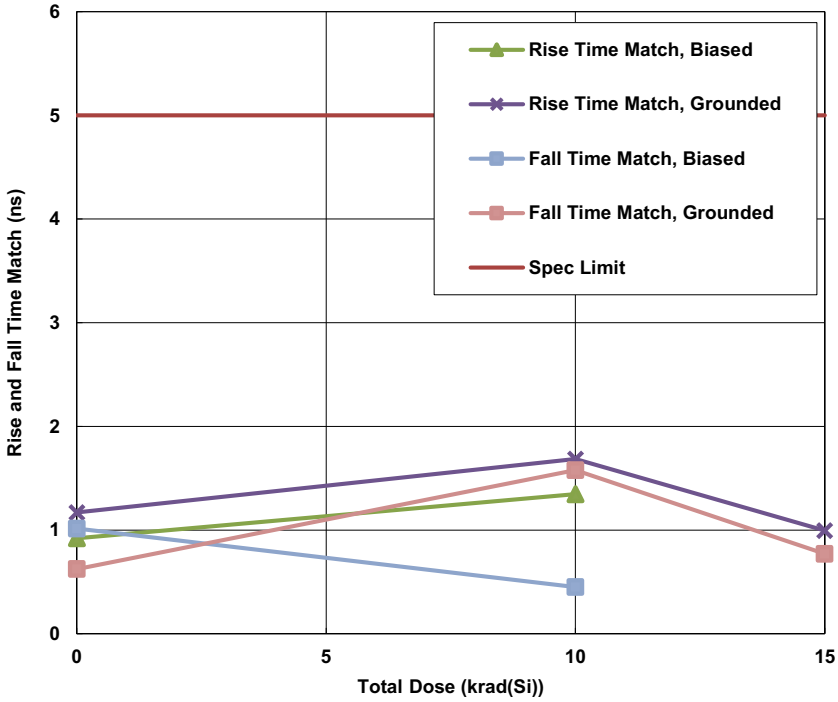

Figure 18. ISL7457SRH quad CMOS driver rise and fall time match at 5V supply as a function of LDR total dose irradiation for the unbiased (grounded) and biased cases. The dose rate was 0.01rad(Si)/s. Sample sizes were two each for the unbiased and biased groups. The post-radiation SMD limit is 5ns maximum.

4. Discussion and Conclusion

This document reports the results of LDR TID testing for the ISL7457SRH radiation hardened quad CMOS driver. This was a limited test as the part is not specified for LDR performance and an -EH version (indicating RLAT at both HDR and LDR) is not available or planned. The results of this test are therefore intended as customer guidance only. Samples were tested at LDR under biased and unbiased conditions, as outlined in MIL-STD-883 TM 1019. Testing was completed to 15krad(Si), which represents a 50% overtest across the 10krad(Si) SMD and datasheet TID rating. At the 15krad(Si) level both biased samples were found to be effectively nonfunctional, with the positive and negative supply current well beyond the 5mA maximum post-irradiation SMD limit. Unfortunately, these high current levels caused the ATE to ‘top on first fail, meaning this dataset contains no further 15krad(Si) parametric data for the two failed samples; that data is missing from the curves shown in Figure 5 through Figure 18. All four samples showed good stability of both DC and AC parameters after 10krad(Si). For these parameters, no differences between biased and unbiased irradiation were noted, and the part is not considered bias sensitive when operated within the SMD total dose limits.

The ISL7457SRH is built in a United Microelectronics Corporation (UMC) foundry process that is basically CMOS; however, the part contains a bandgap reference using parasitic PNP transistors, a standard procedure for many designs. The generated reference current is used to bias the four drivers. The presence of these bipolar devices is the likely reason for the observed LDR response of the ISL7457SRH.

5. Revision History

Revision	Date	Description
1.0	Jun 23, 2021	Initial release

Appendix: Reported Parameters and Figures

Table 2. Key Total Dose Parameters

Fig	Parameter	SMD Symbol	Low Limit	High Limit	Unit
3	Positive Supply Current (5V Supply)	I_{S+}	-	5	mA
4	Negative Supply Current (5V Supply)	I_{S-}	-5	-	mA
5	Positive Output Leakage (16.5V Supply)	I_{LEAK+}	-	1.2	mA
6	Negative Output Leakage (16.5V Supply)	I_{LEAK-}	-50	-	µA
7	Positive Output Leakage (5V Supply)	I_{LEAK+}	-	1.2	mA
8	Negative Output Leakage (5V Supply)	I_{LEAK-}	-50	-	µA
9	ON-Resistance, VH to OUTx (5V Supply)	R_{OH}	-	12	Ω
10	ON-Resistance, VL to OUTx (5V Supply)	R_{OL}	-	7	Ω
11	Turn-On Delay Time (5V Supply)	t_D+	-	30	ns
12	Turn-Off Delay Time (5V Supply)	t_D-	-	40	ns
13	Enable Delay Time (5V Supply)	t_{ENABLE}	-	35	ns
14	Disable Delay Time (5V Supply)	$t_{DISABLE}$	-	50	ns
15	Rise Time (5V Supply)	t_R	-	40	ns
16	Fall Time (5V Supply)	t_F	-	30	ns
17	Turn-On/Turn-Off Delay Match (5V Supply)	t_{DD}	-	12	ns
18	Rise/Fall Time Match (5V Supply)	t_{RF}	-	5	ns

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(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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