CS+ Code Generator for RL78
(CS+ for CC) (CS+ for CA, CX) V2.17.00
Release Note

R20UT4473EJ0100
Rev.1.00
Dec 06, 2018

Thank you for using the CS+ integrated development environment. This document describes the restrictions and points for caution. Read this document before using the product.

Contents

Chapter 1. Target Devices

Below is a list of devices supported by the Code Generator for RL78/G10 V1.05.02.03	
PIN	Device name
10pin	R5F10Y14, R5F10Y16, R5F10Y17
16pin	R5F10Y44, R5F10Y46, R5F10Y47
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/G10 User's Manual: Hardware	R01UH0384JJ0311 Rev.3.11
	R01UH0384EJ0311 Rev.3.11

Below is a list of devices supported by the Code Generator for RL78/G11 V1.02.02.04	
PIN	Device name
10pin	R5F1051A
16pin	R5F1054A
20pin	R5F1056A
24pin	R5F1057A
25pin	R5F1058A
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/G11 User's Manual: Hardware	R01UH0637JJ0110 Rev.1.10
	R01UH0637EJ0110 Rev.1.10

Below is a list of devices supported by the Code Generator for RL78/G12 V2.04.03.01	
PIN	Device name
20pin	R5F10266, R5F10267, R5F10268, R5F10269, R5F1026A R5F10366, R5F10367, R5F10368, R5F10369, R5F1036A
24pin	R5F10277, R5F10278, R5F10279, R5F1027A R5F10377, R5F10378, R5F10379, R5F1037A
30pin	R5F102A7, R5F102A8, R5F102A9, R5F102AA R5F103A7, R5F103A8, R5F103A9, R5F103AA
The Code Generator is based on the following documents.	
Manual Name	Document Number
RL78/G12 User's Manual: Hardware	R01UH0200JJ0210 Rev.2.10
	R01UH0200EJ0210 Rev.2.10

Below is a list of devices supported by the Code Generator for RL78/G13 V2.05.03.01	
PIN	Device name
20pin	R5F1006A, R5F1006C, R5F1006D, R5F1006E R5F1016A, R5F1016C, R5F1016D, R5F1016E
24pin	R5F1007A, R5F1007C, R5F1007D, R5F1007E R5F1017A, R5F1017C, R5F1017D, R5F1017E
25pin	R5F1008A, R5F1008C, R5F1008D, R5F1008E R5F1018A, R5F1018C, R5F1018D, R5F1018E
30pin	R5F100AA, R5F100AC, R5F100AD, R5F100AE, R5F100AF, R5F100AG R5F101AA, R5F101AC, R5F101AD, R5F101AE, R5F101AF, R5F101AG
32pin	R5F100BA, R5F100BC, R5F100BD, R5F100BE, R5F100BF, R5F100BG R5F101BA, R5F101BC, R5F101BD, R5F101BE, R5F101BF, R5F101BG
36pin	R5F100CA, R5F100CC, R5F100CD, R5F100CE, R5F100CF, R5F100CG R5F101CA, R5F101CC, R5F101CD, R5F101CE, R5F101CF, R5F101CG
40pin	R5F100EA, R5F100EC, R5F100ED, R5F100EE, R5F100EF, R5F100EG, R5F100EH R5F101EA, R5F101EC, R5F101ED, R5F101EE, R5F101EF, R5F101EG, R5F101EH
44pin	R5F100FA, R5F100FC, R5F100FD, R5F100FE, R5F100FF, R5F100FG, R5F100FH R5F100FJ, R5F100FK, R5F100FL R5F101FA, R5F101FC, R5F101FD, R5F101FE, R5F101FF, R5F101FG, R5F101FH R5F101FJ, R5F101FK, R5F101FL
48pin	R5F100GA, R5F100GC, R5F100GD, R5F100GE, R5F100GF, R5F100GG, R5F100GH R5F100GJ, R5F100GK, R5F100GL R5F101GA, R5F101GC, R5F101GD, R5F101GE, R5F101GF, R5F101GG, R5F101GH R5F101GJ, R5F101GK, R5F101GL
52pin	R5F100JC, R5F100JD, R5F100JE, R5F100JF, R5F100JG, R5F100JH R5F100JJ, R5F100JK, R5F100JL R5F101JC, R5F101JD, R5F101JE, R5F101JF, R5F101JG, R5F101JH R5F101JJ, R5F101JK, R5F101JL
64pin	R5F100LC, R5F100LD, R5F100LE, R5F100LF, R5F100LG, R5F100LH R5F100LJ, R5F100LK, R5F100LL R5F101LC, R5F101LD, R5F101LE, R5F101LF, R5F101LG, R5F101LH R5F101LJ, R5F101LK, R5F101LL
80pin	R5F100MF, R5F100MG, R5F100MH, R5F100MJ, R5F100MK, R5F100ML R5F101MF, R5F101MG, R5F101MH, R5F101MJ, R5F101MK, R5F101ML
100pin	R5F100PF, R5F100PG, R5F100PH, R5F100PJ, R5F100PK, R5F100PL R5F101PF, R5F101PG, R5F101PH, R5F101PJ, R5F101PK, R5F101PL
128pin	R5F100SH, R5F100SJ, R5F100SK, R5F100SL R5F101SH, R5F101SJ, R5F101SK, R5F101SL

The Code Generator is based on the following documents.

Manual Name	Document Number
RL78/G13 User's Manual: Hardware	R01UH0146JJ0330 Rev.3.30
	R01UH0146EJ0330 Rev.3.30

Below is a list of devices supported by the Code Generator for RL78/G14 V2.05.03.02	
PIN	Device name
30pin	R5F104AA, R5F104AC, R5F104AD, R5F104AE, R5F104AF, R5F104AG
32pin	R5F104BA, R5F104BC, R5F104BD, R5F104BE, R5F104BF, R5F104BG
36pin	R5F104CA, R5F104CC, R5F104CD, R5F104CE, R5F104CF, R5F104CG
40pin	R5F104EA, R5F104EC, R5F104ED, R5F104EE, R5F104EF, R5F104EG, R5F104EH
44pin	R5F104FA, R5F104FC, R5F104FD, R5F104FE, R5F104FF, R5F104FG, R5F104FH R5F104FJ
48pin	R5F104GA, R5F104GC, R5F104GD, R5F104GE, R5F104GF, R5F104GG, R5F104GH R5F104GJ, R5F104GK, R5F104GL
52pin	R5F104JC, R5F104JD, R5F104JE, R5F104JF, R5F104JG, R5F104JH R5F104JJ
64pin	R5F104LC, R5F104LD, R5F104LE, R5F104LF, R5F104LG, R5F104LH R5F104LJ, R5F104LK, R5F104LL
80pin	R5F104MF, R5F104MG, R5F104MH, R5F104MJ, R5F104MK, R5F104ML
100pin	R5F104PF, R5F104PG, R5F104PH, R5F104PJ, R5F104PK, R5F104PL
The Code Generator is based on the following documents.	
Manual Name	Document Number
RL78/G14 User's Manual: Hardware	R01UH0186JJ0330 Rev.3.30
	R01UH0186EJ0330 Rev.3.30

Below is a list of devices supported by the Code Generator for RL78/G1A V2.04.01.02	
PIN	Device name
25pin	R5F10E8A, R5F10E8C, R5F10E8D, R5F10E8E
32pin	R5F10EBA, R5F10EBC, R5F10EBD, R5F10EBE
48pin	R5F10EGA, R5F10EGC, R5F10EGD, R5F10EGE
64pin	R5F10ELC, R5F10ELD, R5F10ELE
The Code Generator is based on the following documents.	
Manual Name	Document Number
RL78/G1A User's Manual: Hardware	R01UH0305JJ0200 Rev.2.00
	R01UH0305EJ0200 Rev.2.00

Below is a list of devices supported by the Code Generator for RL78/G1C V1.03.02.01	
PIN	Device name
32pin	R5F10JBC, R5F10KBC
48pin	R5F10JGC, R5F10KGC
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/G1C User's Manual: Hardware	R01UH0348JJ0100 Rev.1.00
	R01UH0348EJ0100 Rev.1.00

Below is a list of devices supported by the Code Generator for RL78/G1E V1.04.02.04	
PIN	Device name
64pin	R5F10FLC, R5F10FLD, R5F10FLE
80pin	R5F10FMC, R5F10FMD, R5F10FME
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/G1E User's Manual: Hardware	R01UH0353JJ0101 Rev.1.01

Below is a list of devices supported by the Code Generator for RL78/G1G V1.01.01.03	
PIN	Device name
30pin	R5F11EA8, R5F11EAA
32pin	R5F11EB8, R5F11EBA
44pin	R5F11EF8, R5F11EFA
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/G1G User's Manual: Hardware	R01UH0499JJ0100 Rev.1.00
	R01UH0499EJ0100 Rev.1.00

Below is a list of devices supported by the Code Generator for RL78/G1F V1.01.02.03	
PIN	Device name
24pin	R5F11B7C, R5F11B7E
32pin	R5F11BBC, R5F11BBE
36pin	R5F11BCC, R5F11BCE
48pin	R5F11BGC, R5F11BGE
64pin	R5F11BLC, R5F11BLE
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/G1F User's Manual: Hardware	R01UH0516JJ0100 Rev.1.00
	R01UH0516EJ0100 Rev.1.00

Below is a list of devices supported by the Code Generator for RL78/G1D V1.01.02.03	
PIN	Device name
48pin	R5F11AGG, R5F11AGH, R5F11AGJ
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/G1D User's Manual: Hardware	R01UH0515JJ0100 Rev.1.00
	R01UH0515EJ0100 Rev.1.00

Below is a list of devices supported by the Code Generator for RL78/G1H V1.01.02.03	
PIN	Device name
64pin	R5F11FLJ, R5F11FLK, R5F11FLL
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/G1H User's Manual: Hardware	R01UH0575JJ0100 Rev.1.00
	R01UH0575EJ0100 Rev.1.00

Below is a list of devices supported by the Code Generator for RL78/H1D V1.00.00.05	
PIN	Device name
48pin	R5F11NGG, R5F11NGF
64pin	R5F11NLG, R5F11PLG, R5F11NLF, R5F11PLF
80pin	R5F11RMG, R5F11NMG, R5F11NMF, R5F11NME
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/H1D User's Manual: Hardware	R01UH0756JJ0080 Rev.0.80
	R01UH0756EJ0080 Rev.0.80

Below is a list of devices supported by the Code Generator for RL78/L12 V2.04.02.01	
PIN	Device name
32pin	R5F10RBC, R5F10RBA, R5F10RB8
44pin	R5F10RFC, R5F10RFA, R5F10RF8
48pin	R5F10RGC, R5F10RGA, R5F10RG8
52pin	R5F10RJC, R5F10RJA, R5F10RJ8
64pin	R5F10RLC, R5F10RLA
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/L12 User's Manual: Hardware	R01UH0330JJ0200 Rev.2.00
	R01UH0330EJ0200 Rev.2.00

Below is a list of devices supported by the Code Generator for RL78/L13 V1.04.02.03	
PIN	Device name
64pin	R5F10WLA, R5F10WLC, R5F10WLD, R5F10WLE, R5F10WLF, R5F10WLG
80pin	R5F10WMA, R5F10WMC, R5F10WMD, R5F10WME, R5F10WMF, R5F10WMG
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/L13 User's Manual: Hardware	R01UH0382JJ0100 Rev.1.00
	R01UH0382EJ0100 Rev.1.00

Below is a list of devices supported by the Code Generator for RL78/L1A V1.01.02.03	
PIN	Device name
80pin	R5F11MMD, R5F11MME, R5F11MMF
100pin	R5F11MPE, R5F11MPF, R5F11MPG
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/L1A User's Manual: Hardware	R01UH0636JJ0100 Rev.1.00
	R01UH0636EJ0100 Rev.1.00

Below is a list of devices supported by the Code Generator for RL78/L1C V1.03.01.04	
PIN	Device name
80pin	R5F110MJ, R5F110MH, R5F110MG, R5F110MF, R5F110ME, R5F111MJ, R5F111MH, R5F111MG, R5F111MF, R5F111ME
100pin	R5F110PJ, R5F110PH, R5F110PG, R5F110PF, R5F110PE, R5F111PJ, R5F111PH, R5F111PG, R5F111PF, R5F111PE
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/L1C User's Manual: Hardware	R01UH0409JJ0100 Rev.1.00
	R01UH0409EJ0100 Rev.1.00

Below is a list of devices supported by the Code Generator for RL78/F12 V2.04.03.01	
PIN	Device name
20pin	R5F1096E, R5F1096D, R5F1096C, R5F1096B, R5F1096A, R5F10968
30pin	R5F109AE, R5F109AD, R5F109AC, R5F109AB, R5F109AA
32pin	R5F109BE, R5F109BD, R5F109BC, R5F109BB, R5F109BA
48pin	R5F109GE, R5F109GD, R5F109GC, R5F109GB, R5F109GA
64pin	R5F109LE, R5F109LD, R5F109LC, R5F109LB, R5F109LA
The Code Generator is based on the following documents.	
Manual Name	Document Number
RL78/F12 User's Manual: Hardware	R01UH0231JJ0111 Rev.1.11
	R01UH0231EJ0111 Rev.1.11

Below is a list of devices supported by the Code Generator for RL78/F13 V2.03.03.01	
PIN	Device name
20pin	R5F10A6A, R5F10A6C, R5F10A6D, R5F10A6E
30pin	R5F10AAA, R5F10AAC, R5F10AAD, R5F10AAE R5F10BAC, R5F10BAD, R5F10BAE, R5F10BAF, R5F10BAG
32pin	R5F10ABA, R5F10ABC, R5F10ABD, R5F10ABE R5F10BBC, R5F10BBD, R5F10BBE, R5F10BBF, R5F10BBG
48pin	R5F10AGA, R5F10AGC, R5F10AGD, R5F10AGE, R5F10AGF, R5F10AGG R5F10BGC, R5F10BGD, R5F10BGE, R5F10BGF, R5F10BGG
64pin	R5F10BLC, R5F10ALD, R5F10ALE, R5F10ALF, R5F10ALG R5F10BLC, R5F10BLD, R5F10BLE, R5F10BLF, R5F10BLG
80pin	R5F10AME, R5F10AMF, R5F10AMG R5F10BME, R5F10BMF, R5F10BMG
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/F13,F14 User's Manual: Hardware	R01UH0368JJ0210 Rev.2.10
	R01UH0368EJ0210 Rev.2.10

Below is a list of devices supported by the Code Generator for RL78/F14 V2.03.03.01	
PIN	Device name
30pin	R5F10PAD, R5F10PAE
32pin	R5F10PBD, R5F10PBE
48pin	R5F10PGD, R5F10PGE, R5F10PGF, R5F10PGG, R5F10PGH, R5F10PGJ
64pin	R5F10PLE, R5F10PLF, R5F10PLG, R5F10PLH, R5F10PLJ
80pin	R5F10PME, R5F10PMF, R5F10PMG, R5F10PMH, R5F10PMJ
100pin	R5F10PPE, R5F10PPF, R5F10PPG, R5F10PPH, R5F10PPJ
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/F13,F14 User's Manual: Hardware	R01UH0368JJ0210 Rev.2.10
	R01UH0368EJ0210 Rev.2.10

Below is a list of devices supported by the Code Generator for RL78/F15 V1.01.03.01	
PIN	Device name
48pin	R5F113GL, R5F113GK
64pin	R5F113LL, R5F113LK
80pin	R5F113ML, R5F113MK
100pin	R5F113PL, R5F113PK, R5F113PJ, R5F113PH, R5F113PG
144pin	R5F113TL, R5F113TK, R5F113TJ, R5F113TH, R5F113TG
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/F15 User's Manual: Hardware	R01UH0559JJ0100 Rev.1.00
	R01UH0559EJ0100 Rev.1.00

Below is a list of devices supported by the Code Generator for RL78/F1E V1.01.02.01	
PIN	Device name
64pin	R5F11KLE, R5F11LLE, R5F11KLF, R5F11LLF, R5F11KLG, R5F11LLG
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/F1E User's Manual: Hardware	R01UH0611JJ0050 Rev.0.50
	R01UH0611EJ0050 Rev.0.50

Below is a list of devices supported by the Code Generator for RL78/I1A V2.04.03.01	
PIN	Device name
20pin	R5F1076C
30pin	R5F107AC, R5F107AE
38pin	R5F107DE
The Code Generator is based on the following documents.	
Manual Name	Document Number
RL78/I1A User's Manual: Hardware	R01UH0169JJ0210 Rev.2.10
	R01UH0169EJ0210 Rev.2.10

Below is a list of devices supported by the Code Generator for RL78/I1B V1.03.02.03	
PIN	Device name
80pin	R5F10MME, R5F10MMG
100pin	R5F10MPE, R5F10MPG
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/I1B User's Manual: Hardware	R01UH0407JJ0100 Rev.1.00
	R01UH0407EJ0100 Rev.1.00

Below is a list of devices supported by the Code Generator for RL78/I1D V1.01.02.05	
PIN	Device name
20pin	R5F11768, R5F1176A
24pin	R5F11778, R5F1177A
30pin	R5F117A8, R5F117AA, R5F117AC
32pin	R5F117BA, R5F117BC
48pin	R5F117GA, R5F117GC
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/I1D User's Manual: Hardware	R01UH0474JJ0100 Rev.1.00
	R01UH0474EJ0100 Rev.1.00

Below is a list of devices supported by the Code Generator for RL78/I1E V1.03.02.03	
PIN	Device name
32pin	R5F11CBC
36pin	R5F11CCC
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/I1E User's Manual: Hardware	R01UH0524JJ0100 Rev.1.00
	R01UH0524EJ0100 Rev.1.00

Below is a list of devices supported by the Code Generator for RL78/I1C V1.01.03.02	
PIN	Device name
64pin	R5F11NLE, R5F11NLG
80pin	R5F11NME, R5F11NMG, R5F11NMJ
100pin	R5F11NPJ
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/I1C User's Manual: Hardware	R01UH0587JJ0051 Rev.0.51
	R01UH0587EJ0051 Rev.0.51

Please check a checkbox of Code Generator plug-in at additional tab of Plug-in management dialog to use Code Generator for target device.

How to open of Plug-in management dialog: [Tool(T)]-[Plug-in Management(P)…] menu of CS+

Plug-in name	Supported device
Code Generator Plug-in	78K0, 78K0R, V850, a part of RL78(*) *: RL78/I1A, RL78/G12, RL78/G13, RL78/G14, RL78/G1A, RL78/F12, RL78/L12, RL78/F13, RL78/F14, RL78/F15
Code Generator/PinView Plug-in	RL78 except the above, RX

Chapter 2. User's Manuals

Please read the following user's manuals together with this document.

Manual Name	Document Number
CS+ Code Generator Peripheral Function Operation	R20UT3104EJ0110
CS+ Code Generator Pin View	R20UT3105EJ0110
CS+ RL78 Pin Configurator	R20UT3106EJ0100
Code Generator RL78 API Reference	R20UT4323EJ0100
CS+ V7.00.00 Message (CS+ for CC)	R20UT4309EJ0100
CubeSuite+ V2.02.00 Message (CS+ for CA,CX)	R20UT2871EJ0100

Chapter 3. Uninstallation

There are two ways to uninstall this product.

- Use the integrated uninstaller from Renesas (uninstalls all CS+ components)
- Use the Windows uninstaller (only uninstalls this product only)

To use the Windows uninstaller, select "CS+ for CC Code Generator for RL78" or "CS+ for CA,CX Code Generator for RL78" from "Programs and Features" of the control panel.

Chapter 4. Changes

This chapter describes change to CS+ Code Generator for RL78 (CS+ for CC) (CS+ for CA, CX) V2.17.00.

List of Changes

No	Description	Version *1
		RL78/I1A V2.04.03.01
1	The issue of setting Serial UART4 has been corrected	○

○: Applicable, -: Not Applicable(finish of correction), /: Outside of function

Note 1: Version is described in the generated code.

4.1 Details of Changes

4.1.1 The issue of setting Serial UART4 has been corrected

Please refer to 7.2.24 for the detail.

Chapter 5. Points for Cautions

This chapter describes points for caution regarding the CS+ Code Generator for RL78 (CS+ for CC) (CS+ for CA, CX) V2.17.00.

5.1 List of Cautions

List of Changes (1/2)

No	Description	Version *1												
		RL78/G10 V1.05.02.03	RL78/G11 V1.02.02.04	RL78/G12 V2.04.03.01	RL78/G13 V2.05.03.01	RL78/G14 V2.05.03.02	RL78/G1A V2.04.01.02	RL78/G1C V1.03.02.01	RL78/G1D V1.01.02.03	RL78/G1E V1.04.02.04	RL78/G1F V1.01.02.03	RL78/G1G V1.01.01.03	RL78/G1H V1.01.02.03	RL78/H1D V1.00.00.05
1	Cautions when using a DTC function (CS+ for CA,CX)	/	/	/	/	○	/	/	/	/	/	/	/	/
2	Cautions of Pin Configurator (CS+ for CA,CX)	/	/	○	○	○	○	/	/	/	/	/	/	/
3	Cautions of timer array unit input clock sauce	/	/	/	/	/	/	/	/	/	/	/	/	/
4	Cautions of a high-speed on-chip oscillator (CS+ for CA,CX)	/	/	○	○	○	○	/	/	/	/	/	/	/
5	Cautions of High Speed DTC chain transfer	/	/	/	/	/	/	/	/	/	/	/	/	/
6	Cautions of CPU and peripheral clock setting	/	/	/	/	/	/	/	/	/	/	/	/	/

○: Applicable, -: Not Applicable(finish of correction), /: Outside of function

List of Changes (2/2)

No	Description	Version *1												
		RL78/F12 V2.04.03.01	RL78/F13 V2.03.03.01	RL78/F14 V2.03.03.01	RL78/F15 V1.01.03.01	RL78/F1E V1.01.02.01	RL78/I1A V2.04.03.01	RL78/I1B V1.03.02.03	RL78/I1C V1.01.02.04	RL78/I1D V1.01.02.05	RL78/I1E V1.03.02.03	RL78/L12 V2.04.02.01	RL78/L13 V1.04.02.03	RL78/L1A V1.01.02.03	RL78/L1C V1.03.01.04
1	Cautions when using a DTC function (CS+ for CA,CX)	/	/	○	○	○	/	/	/	/	/	/	/	○	/
2	Cautions of Pin Configurator (CS+ for CA,CX)	○	○	○	○	/	○	/	/	/	/	○	/	/	/
3	Cautions of timer array unit input clock sauce	○	○	○	/	/	/	/	/	/	/	/	/	/	/
4	Cautions of a high-speed on-chip oscillator (CS+ for CA,CX)	○	○	○	/	/	○	/	/	/	/	○	/	/	/
5	Cautions of High Speed DTC chain transfer	/	○	○	○	/	/	/	/	/	/	/	/	/	
6	Cautions of CPU and peripheral clock setting	/	○	○	○	/	/	/	/	/	/	/	/	/	

○: Applicable, -: Not Applicable(finish of correction), /: Outside of function

Note 1: Version is described in the generated code.

5.2 Cautions Details

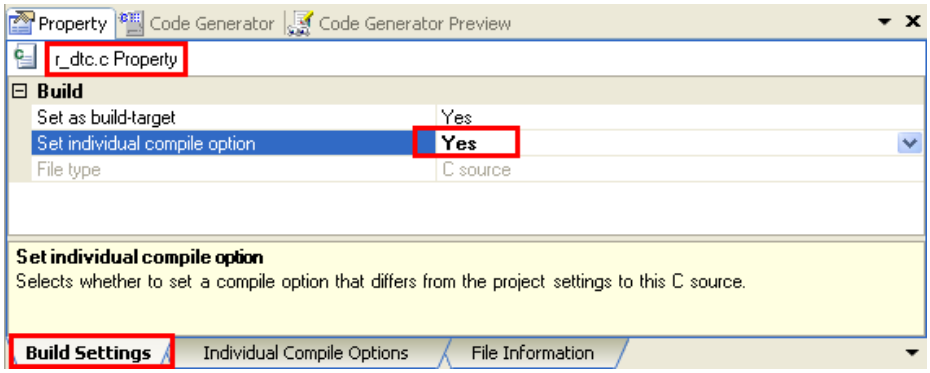
5.2.1 Cautions when using a DTC function (CS+ for CA,CX)

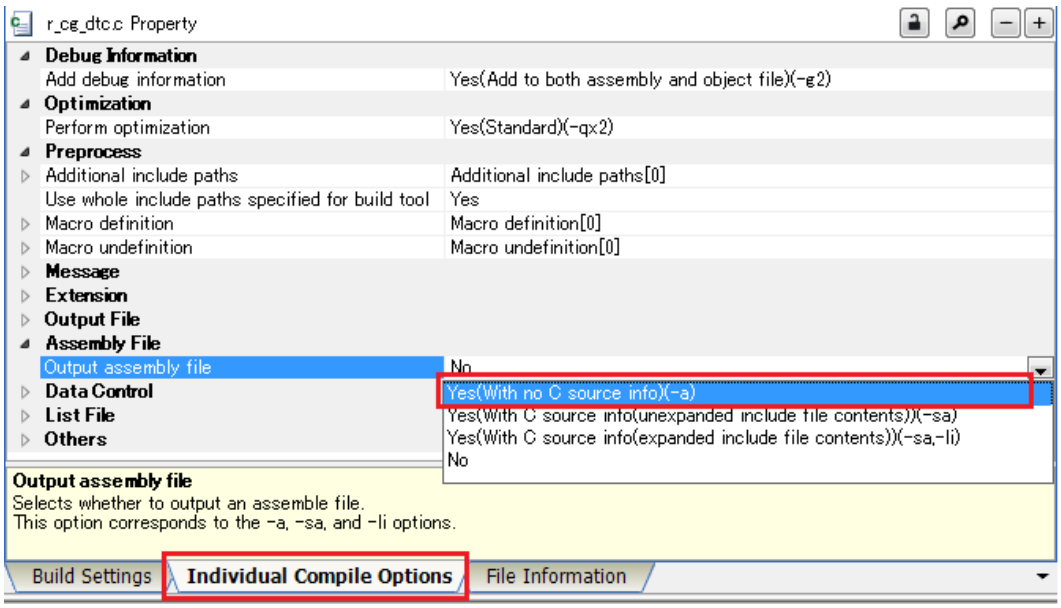
When DTC is used, the following warning message is displayed and an object file is not generated.

CC78K0R warning W0837: Output assembler source file , not object file

[Workaround]

Set up the following individual option of building.





5.2.2 Cautions of Pin Configurator (CS+ for CA,CX)

There is a pin which is not reflected even if it performs reflection to pin configurator from code generator.

Even if it sets up using a code generator PIOR function, it is not reflected to pin configurator.

[Workaround] Edit terminal information with pin configurator.

5.2.3 Cautions of timer array unit input clock sauce

When the clock sauce of a timer input is set as a RTC1HZ output by setup of a timer array unit, a setup about the output of the RTC1HZ terminal of a real-time clock becomes invalid. The code which outputs RTC1HZ then is not generated.

[Workaround] When you set to a RTC1HZ signal by setup of a timer array unit, please choose a setup which uses a real-time clock and add the code which outputs RTC1HZ.

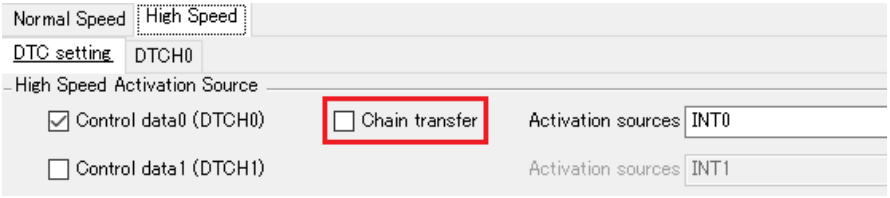
5.2.4 Cautions of a high-speed on-chip oscillator (CS+ for CA,CX)

When a high-speed on-chip oscillator clock is set up by CubeSuite+ RL78, 78K0R, and 78K0 code generator V2.01.00 or earlier, If it is read by CubeSuite+V2.03.00, a clock frequency setup of a high-speed on-chip oscillator may not be right.

[Workaround] Re-set up the frequency right in that case.

5.2.5 Cautions of High Speed DTC chain transfer

Although there are chain transfer setting items of High Speed DTC, code corresponding to chain transfer is not supported.



[Workaround] It cannot be used for chain transfer.

5.2.6 Cautions of CPU and peripheral clock setting

When High-speed OCO clock setting is set to 48/24/12/6/3MHz and is selected as PLL clock, setting of 32MHz is prohibited in CPU and peripheral clock (fCLK), but it can be set.

[Workaround] Do not set 32MHz in CPU and peripheral clock (fCLK).

Chapter 6. Restrictions

This section describes the restrictions on CS+ Code Generator for RL78 (CS+ for CC) (CS+ for CA, CX) V2.17.00.

6.1 List of Restrictions

List of Restrictions (1/2)

No	Description	version *1												
		RL78/G10 V1.05.02.03	RL78/G11 V1.02.02.04	RL78/G12 V2.04.03.01	RL78/G13 V2.05.03.01	RL78/G14 V2.05.03.02	RL78/G1A V2.04.01.02	RL78/G1C V1.03.02.01	RL78/G1D V1.01.02.03	RL78/G1E V1.04.02.04	RL78/G1F V1.01.02.03	RL78/G1G V1.01.01.03	RL78/G1H V1.01.02.03	RL78/H1D V1.00.00.05
1	Restrictions of the coding rule of MISRA-C.	○	○	○	○	○	○	○	○	○	○	○	○	○
2	Restrictions of High-speed on-chip oscillator frequency select register	○	○	○	○	○	○	○	○	○	○	○	○	○
3	Restrictions of internal low-speed or internal high-speed oscillator trimming	○	○	○	○	○	○	○	○	○	○	○	○	○
4	Restriction of a serial array unit	/	/	/	/	/	/	/	/	/	/	/	/	/
5	Restrictions of Flash memory CRC operation function (high-speed CRC)	/	○	○	○	○	○	○	○	○	○	○	○	○
6	Restrictions of Port mode select register (PMS)	/	○	/	/	○	/	○	○	○	○	○	○	○
7	Cautions of the LIN-bus function of UART	/	○	○	○	○	○	○	○	○	○	○	○	○
8	Cautions of extension code, wakeup function and multimaster of serial interface IICA or IIC0	○	○	○	○	○	○	○	○	○	○	○	○	○
9	Cautions of CAN controllers	/	/	/	/	/	/	/	/	/	/	/	/	/
10	Cautions of Safety Functions	○	○	○	○	○	○	○	○	○	○	○	○	○
11	Restriction of USB	/	/	/	/	/	/	○	/	/	/	/	/	/
12	Restriction of RI78V4 project	/	/	/	/	/	/	/	/	/	/	/	/	/
13	Fast Mode Plus setting in IICA slave	○	○	○	○	○	○	○	○	○	○	○	○	○
14	24-pin device TAU0 channel 1 setting restriction	/	/	/	/	/	/	/	/	/	○	/	/	/
15	Restriction on setting value of option byte C1H	/	/	/	/	/	/	/	/	/	/	/	/	/
16	Restriction on real-time clock API function	/	/	/	/	/	/	/	/	/	○	/	○	/
17	Mistake in unit for 'Gain setting' of ΔΣ A/D CONVERTER	/	/	/	/	/	/	/	/	/	/	/	/	○

○: Applicable, /: Not Applicable

Note 1: Version is described in the generated code.

List of Restrictions (2/2)

No	Description	version *1													
		RL78/F12 V2.04.03.01	RL78/F13 V2.03.03.01	RL78/F14 V2.03.03.01	RL78/F15 V1.01.03.01	RL78/F1E V1.01.02.01	RL78/I1A V2.04.03.01	RL78/I1B V1.03.02.03	RL78/I1C V1.01.02.04	RL78/I1D V1.01.02.05	RL78/I1E V1.03.02.03	RL78/L12 V2.04.02.01	RL78/L13 V1.04.02.03	RL78/L1A V1.01.02.03	RL78/L1C V1.03.01.04
1	Restrictions of the coding rule of MISRA-C.	○	○	○	○	○	○	○	○	○	○	○	○	○	○
2	Restrictions of High-speed on-chip oscillator frequency select register	○	○	○	○	○	/	○	○	○	○	○	○	○	○
3	Restrictions of internal low-speed or internal high-speed oscillator trimming	○	○	○	○	○	○	○	○	○	○	○	○	○	○
4	Restriction of a serial array unit	/	/	/	/	/	○	/	/	/	/	/	/	/	/
5	Restrictions of Flash memory CRC operation function (high-speed CRC)	○	○	○	○	○	○	○	○	○	○	○	○	○	○
6	Restrictions of Port mode select register (PMS)	/	○	○	○	○	○	○	○	○	○	/	○	○	○
7	Cautions of the LIN-bus function of UART	○	○	○	○	○	○	○	○	○	○	○	○	○	○
8	Cautions of extension code, wakeup function and multimaster of serial interface IICA or IIC0	○	○	○	○	○	○	○	○	○	○	○	○	○	○
9	Cautions of CAN controllers	/	○	○	○	○	/	/	/	/	/	/	/	/	/
10	Cautions of Safety Functions	○	○	○	○	○	○	○	○	○	○	○	○	○	○
11	Restriction of USB	/	/	/	/	/	/	/	/	/	/	/	/	/	○
12	Restriction of RI78V4 project	/	/	/	/	/	/	/	/	/	/	/	/	/	/
13	Fast Mode Plus setting in IICA slave	○	○	○	○	○	○	○	○	○	○	○	○	○	○
14	24-pin device TAU0 channel 1 setting restriction	/	/	/	/	/	/	/	/	/	/	/	/	/	/
15	Restriction on setting value of option byte C1H	/	/	/	/	○	/	/	/	/	/	/	/	/	/
16	Restriction on real-time clock API function	/	/	/	/	○	/	/	/	/	○	/	/	/	/
17	Mistake in unit for 'Gain setting' of ΔΣ A/D CONVERTER	/	/	/	/	/	/	/	/	/	/	/	/	/	/

○: Applicable, /: Not Applicable

Note 1: Version is described in the generated code.

6.2 Restrictions Details

6.2.1 Restrictions of the coding rule of MISRA-C

Compliance with the MISRA-C (Guidelines for the Use of the C Language in Vehicle Based Software) coding convention is not supported for source code output by the code generator.

6.2.2 Restrictions of High-speed on-chip oscillator frequency select register

Code generator is not equivalent to a setup of high-speed on-chip oscillator frequency select register.

6.2.3 Restrictions of internal low-speed or internal high-speed oscillator trimming

Code generator is not equivalent to a setup of internal low-speed or internal high-speed oscillator trimming register.

6.2.4 Restriction of a serial array unit

Code generator is not equivalent to a setup of single-wire UART mode and DMX512 communication.

6.2.5 Restrictions of Flash memory CRC operation function (high-speed CRC)

Code generator does not correspond to a flash memory CRC operation function (high-speed CRC). Please refer to application note r01an0736ej.
https://www.renesas.com/search/keyword-search.html#genre=document&q=r01an0736ej

6.2.6 Restrictions of Port mode select register (PMS)

Code generator does not correspond to a port mode select register (PMS).

6.2.7 Restrictions of the LIN-bus function of UART

The code generator is not supporting the LIN-bus functions of serial interface UART0 or UART2 or UART3 or UART6 or UARTF.

6.2.8 Restrictions of extension code, multimaster, wakeup function of serial interface IICA or IIC0

The code generator is not supporting the extension code, multimaster, wakeup function of serial interface IIC.

6.2.9 Cautions of CAN controllers

The code generator is not supporting the CAN Controllers.

6.2.10 Cautions of Safety Functions

RAM parity error detection function of Safety Functions is not supported.

6.2.11 Restriction of USB

The code generator is not supporting the USB host, USB function.

6.2.12 Restriction of RI78V4 project

The Code generator can't be used in a project of RI78V4. But code generator is shown to a project of RI78V4. Even if a code is generated, RI78V4 will be an unsupported purpose build error.

6.2.13 Fast Mode Plus setting in IICA slave

If the Fast Mode Plus is set when using the IICA slave, IICA Low level range setting register (IICWLn, n= channel number), and IICA High level range setting register (IICWHLn) are not set correctly.

[Workaround] There is no workaround.

After doing code generator, please rewrite the numerical value of the register setting of IICWLn, IICWHn in the R_IICAn_Create function. I depend on a system for the numerical value. Please change device UM to reference.

6.2.14 24-pin device TAU0 channel 1 setting restriction

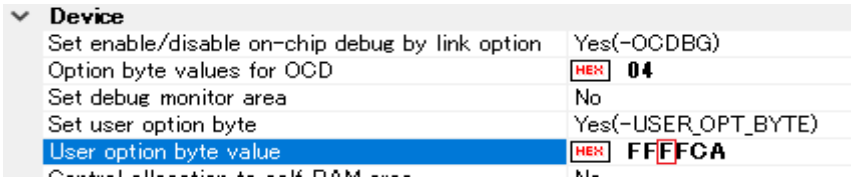
In the 24-pin device, interval timer is only selectable for the TAU0 channel 1 setting.

[Workaround] There is no workaround.

In the 32-pin device, other timer functions besides “Interval timer” are selectable for the TAU0 channel 1 setting. Refer to the setting to make a correction.

6.2.15 Restriction on setting value of option byte C1H

The set value of option byte C1H is wrong.



Wrong: CLKMB = 0 when " Unused" is set, CLKMB = 1 when "Used" is set.

Right: CLKMB = 1 when " Unused" is set, CLKMB = 0 when "Used" is set.

[Workaround] After generating the code, set the CLKMB of C1H to the correct value from the properties of the Build Tool (Link Options - Device - User option byte value).

6.2.16 Restriction on real-time clock API function

An unnecessary wait time code is output in the R_RTC_Set_AlarmOn().

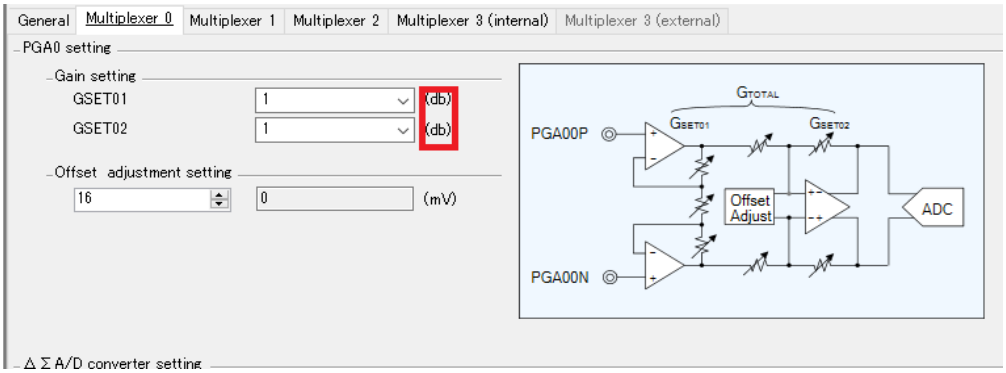
```
/* Change the waiting time according to the system */
for (w_count = 0U; w_count < RTC_WAITTIME_2FRTC; w_count++)
{
    NOP();
}
```

[Workaround] There is no workaround.

Delete the wait time code in the R_RTC_Set_AlarmOn () function after generating the code.

6.2.17 Mistake in unit for 'Gain setting' of ΔΣ A/D CONVERTER

The unit of Multiplexer 0/1/2/3(Internal)/3(external) are 'db' but it should be 'Gain'.



[Workaround] Please interpret ‘db’ as ‘Gain’ when use GSET01 and/or GSET02.

Chapter 7. Correction History

This section describes correction history of RENESAS TOOL NEWS.

7.1 List of RENESAS TOOL NEWS

Issue Date	Document No.	Description	Device Concerned	Fixed version
May 21, 2012	120521/tn2	With generating codes for the R5F1007x and R5F1017x MCUs, RL78/G13 group	RL78/G13	V1.00.06
Aug. 01, 2012	120801/tn3	With using the code generators for the RL78/G13 and RL78/G14 groups of MCUs	RL78/G13, RL78/G14	V1.00.06
Sep. 01, 2012	120901/tn1	With using the code generator for the RL78/G12 group	RL78/G12	V1.00.06
Feb. 01, 2013	130201/tn1	With using the code generator for the RL78/G14 group of MCUs	RL78/G14	V2.00.00
Jul. 01, 2013	130701/tn1	When edited source codes disappear	RL78/F12, RL78/F13, RL78/F14, RL78/F15, RL78/G10, RL78/G12, RL78/G13, RL78/G14, RL78/G1A, RL78/G1C, RL78/G1D, RL78/G1E, RL78/G1F, RL78/G1G, RL78/G1H, RL78/I1A, RL78/I1D, RL78/I1E, RL78/L12, RL78/L13, RL78/L1C	V2.11.00
		When the port cannot be set properly	RL78/G1A	V2.00.01
Aug. 01, 2013	130801/tn1	With using the code generator for the RL78/G12 group of MCUs	RL78/G12	V2.00.01

Issue Date	Document No.	Description	Device Concerned	Fixed version
Oct. 16, 2013	131016/tn1	2. When a RL78/G13 product in a 100-pin package is selected	RL78/G13	V2.03.00
		3. With the key input interrupt setting	RL78/L12	V2.03.00
		4. With A/D converter operation setting	RL78/G1A	V2.03.00
		5. When the timer KB20 is in use	RL78/L13	V2.03.00
Apr. 16, 2014	140416/tn5	With selecting the 20-pin, 30-pin, or 32-pin package for the RL78/F13 or RL78/F14 group	RL78/F13, RL78/F14	V2.04.00
		With using the remote control carrier wave mask signal in the RL78/L12 or RL78/L13 group	RL78/L12, RL78/L13	V2.04.00
		With processing to reflect the pin configurator when the A/D converter is set in the RL78/G12 group	RL78/G12	V2.04.00
		With the case when ports that are not available in the MCU are displayed in the RL78/G14 group	RL78/G14	V2.04.00
Jul. 01, 2014	140701/tn1	With setting port 2	RL78/L13	V2.07.00
		With setting an interval timer	RL78/G10, RL78/G12, RL78/G13, RL78/G14, RL78/G1A, RL78/G1C, RL78/L12, RL78/L13, RL78/L1C, RL78/I1A	V2.07.00
Aug. 16, 2014	140816/tn1	With setting of P20 and P21 of port2	RL78/L1C	V2.05.00
		With setting of port1	RL78/G14	V2.05.00
Nov. 01, 2014	141101/tn2	1. Point for Caution on Settings for CPU Stack Pointer Monitoring	RL78/F13	V2.07.00
		2. Point for Caution on Writing to the Serial Flag Clear Trigger Register (SIR) When Using 3-wire Serial (CSI) Transfer	RL78/F12	V2.07.00
Dec. 16, 2014	141216/tn3	1. Code Generated for Comparator Settings	RL78/I1A	V2.07.00
		2. DTC Settings	RL78/F13, F14	V2.07.00

Issue Date	Document No.	Description	Device Concerned	Fixed version
		3. Setting the Voltage Detection Circuit to "Interrupt Mode"	RL78/L12, RL78/I1A, RL78/G1A, RL78/F13, RL78/F14	V2.07.00
		4. Saving Projects with Settings for the A/D Convertor	RL78/L1C	V2.07.00
		5. Reflection of Pin Configurations in Generated Code	RL78/G12, G13, G14	V2.07.00
Jul. 16, 2015	150716/tn2	1. Clock Generation Circuit (PLL Circuit Operation)	RL78/F13, RL78/F14, RL78/G1C, RL78/L1C	V2.11.00
		2. Setting P40 of Port 4	RL78/F12, RL78/F13, RL78/F14, RL78/G10, RL78/G12, RL78/G13, RL78/G14, RL78/G1A, RL78/G1C, RL78/G1E, RL78/G1F, RL78/G1G, RL78/I1A, RL78/I1D, RL78/L1C, RL78/L12, RL78/L13	V2.11.00
		3. Code Generated for UART0 and UARTF	RL78/F12	V2.11.00
Nov. 16, 2015	151116/tn2	1. Indication of Channels of Serial Interface IICA	RL78/G14	V2.11.00
		2. Procedure for Setting the PLL Clock	RL78/F13, RL78/F14, RL78/F15	V2.11.00
Jan. 16, 2016	160116/tn5	Transfer of data with a length of 10 or more bits through an element of a serial array unit configured as a CSI or data with a length of 16 bits through an element configured as a UART	RL78/F12, RL78/F13, RL78/F14, RL78/F15, RL78/D1A	V2.11.00
Feb. 16, 2016	160216/tn5	1. Using the error interrupt of serial array unit 4 as UART4 or DALI4	RL78/I1A	V2.11.00
		2. Using serial array unit 4 as DALI4	RL78/I1A	V2.11.00
Mar. 16, 2016	160316/tn1	Pin settings for the IICA serial interface when setting the PIOR to change the assignment of pin functions	RL78/G12	V2.11.00

Issue Date	Document No.	Description	Device Concerned	Fixed version
Jun. 16, 2016	R20TS0038EJ0100	Scan Mode of A/D Converter	RL78/F12, RL78/F13, RL78/F14, RL78/F15, RL78/G1A	V2.12.00
Aug. 01, 2016	R20TS0045EJ0100	Peripheral I/O redirection register 0 (PIOR0)	RL78/G1F	V2.12.00
Mar. 1, 2017	R20TS0139EJ0100	1. Input of Ports P10 and P11	RL78/G13 (20/24/25pin product.)	V2.14.00
		2. Port Settings Related to Reset Processing	RL78/F12 (20pin product)	V2.14.00
Dec. 16, 2017	R20TS0244EJ0100	When Continuous Transfer Mode is Selected in the CSI Configuration	RL78/D1A, RL78/F12, RL78/F13, RL78/F14, RL78/F15, RL78/L12	V2.16.00
Mar. 16, 2018	R20TS0290EJ0100	When Opening a Project for RL78/G11 Created by a Previous Version of Code Generator	RL78/G11 (20-pin R5F1056A)	V2.16.00
May. 16, 2018	R20TS0313EJ0100	Writing to Port-Related Registers for Unused Pins	RL78/I1D	V2.16.00
Nov. 16, 2018	R20TS0370EJ0100	When setting the Serial UART4	RL78/I1A	V2.17.00

7.2 Details of RENESAS TOOL NEWS

7.2.1 RENESAS TOOL NEWS Document No.120521/tn2 (CS+ for CA,CX)

This issue has been corrected in CubeSuite+ Code Generator for RL78,78K0R,78K0 V1.00.06.

・ With generating codes for the R5F1007x and R5F1017x MCUs, RL78/G13 group

If you generate the C source file r_cg_port.c, which sets the pin statuses of Port 0 of the R5F1007x and R5F1017x MCUs, RL78/G13 group, an incorrect line is generated as follows:

PMC0 = _00_PMCn0_DI_ON | _00_PMCn1_DI_ON | ;

Here, an expression is omitted at the last end, so when the build is executed by using this file, an error arises.

For details of the problem, refer to the URL below.
https://www.renesas.com /doc/toolnews/eng/2012/120521tn2_e.pdf

7.2.2 RENESAS TOOL NEWS Document No.120801/tn3 (CS+ for CA,CX)

This issue has been corrected in CubeSuite+ Code Generator for RL78,78K0R,78K0 V1.00.06.

(1) The code generator for RL78/G13 group
a. If code is generated so that timers TAUx (x is 1 to 7) of an 80-, 100-, or 128-pin MCU can output square waves, the values of the TOM1 and TOL1 registers, which control TAUx, are not set but those of the TOM0 and TOL0 registers are set.
b. If you make settings of ports, the TTL checkboxes for the P10 and P11 pins are not displayed.

(2) The code generator for RL78/G14 group
a. In the code for setting registers PIOR01 and PIOR04 to 1s in an arrangement of pin assignments, incorrect pins are assigned to INTP10 and INTP11 as follows:

Incorrect:	Correct:
P110 assigned to INTP10	P100 assigned to INTP10
P111 assigned to INTP11	P110 assigned to INTP11

b. If code is generated in an 80- or 100-pin MCU, no functions except "interval" can be selected in the functional selection of timer TAU1.
c. If the code is generated for making settings of UART2 and any of the ports except 13 and 14, an error arises in building it.

For details of the problem, refer to the URL below.
https://www.renesas.com/en-us/doc/toolnews/eng/2012/120801tn3_e.pdf

7.2.3 RENESAS TOOL NEWS Document No.120901/tn1 (CS+ for CA,CX)

This issue has been corrected in CubeSuite+ Code Generator for RL78,78K0R,78K0 V1.00.06.

With using the code generator for the RL78/G12 group

The following problem arises in the code generator for the RL78/G12 group included in the product concerned:
- If you make settings of the key interrupt flag and the triggering edge, the settings cannot properly be reflected to the KRCTL register by the generated code.
KRCTL |= _00_KR_FLAG_UNUSED;
KRCTL |= _01_KR_EDGE_RISING;
The correct codes are as follows:
KRCTL |= _01_KR_FLAG_USED;
KRCTL |= _00_KR_EDGE_FALLING;

For details of the problem, refer to the URL below.
https://www.renesas.com/en-us/doc/toolnews/eng/2012/120901tn1_e.pdf

7.2.4 RENESAS TOOL NEWS Document No.130201/tn1 (CS+ for CA,CX)

This issue has been corrected in CubeSuite+ Code Generator for RL78,78K0R,78K0 V2.00.00.

With using the code generator for the RL78/G14 group of MCUs

(1) With generating incorrect code for cyclic register
If you select PWM from among the operating modes of the RD timer and 64 MHz from among the clock frequencies of the high-speed on-chip oscillator, the code generator generates incorrect code; that is, the value (duty ratio) of the cyclic register is erroneous.
(2) With using alternate-function pins
When the PWM mode is used, every pin for the PWM output, which is an alternate-function pin, cannot be used for the other function. So if you make settings for using these pins for the other functions than PWM, the code generator express an alarm (symbol "!").
However, if you have selected the PWM mode in the RD timer, this alarm is not expressed on the information setting area of the [Port].

For details of the problem, refer to the URL below.
https://www.renesas.com/en-us/doc/toolnews/eng/2013/130201tn1_e.pdf

7.2.5 RENESAS TOOL NEWS Document No.130701/tn1 (CS+ for CC)(CS+ for CA,CX)

This issue has been corrected in CS+ Code Generator for RL78 (CS+ for CC) (CS+ for CA, CX) V2.11.00 (Number 1) and CubeSuite+ Code Generator for RL78,78K0R,78K0 V2.01.00 (Number 2).

・ When edited source codes disappear

If you select Merge File in Generate File Mode in the property of code generator and the source codes are written between each comment below, the file will be merged.
/* Start user code. Do not edit comment generated here */
/* End user code. Do not edit comment generated here */
However, if the number of braces ("{" and "}") in the edited source codes (including the comments) are not the same, the edited source codes may disappear when you run the code generator.

・ When the port cannot be set properly

The port may not be set properly in the code generator for the RL78/G1A group, which is included in the product concerned.

For details of the problem, refer to the URL below.
https://www.renesas.com/en-us/doc/toolnews/eng/2013/130701tn1_e.pdf

7.2.6 RENESAS TOOL NEWS Document No.130801/tn1 (CS+ for CA,CX)

This issue has been corrected in CubeSuite+ Code Generator for RL78,78K0R,78K0 V2.00.01.

・ With using the code generator for the RL78/G12 group of MCUs

In the code generator for the RL78/G12 group, which is included in the product concerned, the following problem has been found:
- Incorrect value set in the option byte (0C1H)

In the 20-pin product of the RL78/G12 group, the option byte (0C1H) is not set to a correct value.

For details of the problem, refer to the URL below.
https://www.renesas.com/en-us/doc/toolnews/eng/2013/130801tn1_e.pdf

7.2.7 RENESAS TOOL NEWS Document No.131016/tn1 (CS+ for CA,CX)

This issue has been corrected in CubeSuite+ Code Generator for RL78,78K0R,78K0 V2.03.00.

・ When a RL78/G13 product in a 100-pin package is selected (RL78/G13 Group)

When a product of the RL78/G13 group in a 100-pin package is selected, starting the pin configuration tool after changing the package type from FB to FA in the pin configuration tool property terminates the CubeSuite+.

・ With the key input interrupt setting (RL78/L12 Group)

The setting of Key interrupt flag and Detection edge may not be saved. When saving the project after making the new setting and then reloading the project, the setting reverts to the original setting as the new one had not been saved.

・ With A/D converter operation setting (RL78/G1A Group)

The Conversion time mode of the Conversion time setting may not be saved.
When saving the project after making the new setting and then reloading the project, the setting reverts to the original setting as the new one had not been saved.

・ When the timer KB20 is in use (RL78/L13 Group)

When the timer KB20 is in use, the settings for Standalone mode (period controlled by external trigger input) and Interleave PFC (power factor correction) output mode may prevent the correct output of the API functions.

For details of the problem, refer to the URL below.
https://www.renesas.com/en-us/doc/toolnews/eng/2013/131016tn1_e.pdf

7.2.8 RENESAS TOOL NEWS Document No.140416/tn5 (CS+ for CA,CX)

This issue has been corrected in CS+ Code Generator for RL78 (CS+ for CC) (CS+ for CA, CX) V2.04.00.

- With selecting the 20-pin, 30-pin, or 32-pin package for the RL78/F13 or RL78/F14 group

When the 20-pin, 30-pin, or 32-pin package is selected for the RL78/F13 or RL78/F14 group and a divided frequency is selected for CPU and peripheral clock (fCLK) in the clock generator settings, the register settings are not output.

- With using the remote control carrier wave mask signal in the RL78/L12 or RL78/L13 group

There is an error in the R_TAU0_Channel2_Stop function for output when PWM output (remote control carrier wave mask signal) is selected in timer channel 2.

- With processing to reflect the pin configurator when the A/D converter is set in the RL78/G12 group

When the Reflect in PIN button is pressed after A/D converter settings are made, the error message below might be displayed for some pins. This indicates failure of reflection in the Pin Configurator.

E0300004: The setting of pin No. XXX was not changed.

Note: XXX indicates the pin number.

- With the case when ports that are not available in the MCU are displayed in the RL78/G14 group

When an RL78/G14 group MCU in the 80-pin package is selected, the settings for the P80 and P81 ports, which are not available in the selected MCU, are displayed.

For details of the problem, refer to the URL below.
https://www.renesas.com/en-us/doc/toolnews/eng/2014/140416tn5_e.pdf

7.2.9 RENESAS TOOL NEWS Document No.140701/tn1 (CS+ for CC)(CS+ for CA,CX)

This issue has been corrected in CS+ Code Generator for RL78 (CS+ for CC) (CS+ for CA, CX) V2.07.00.

・ With setting port 2 (target: RL78/L13 group)

For port 2, even if input to or output from port pins P20 to P27, which are multiplexed with analog pin functions, is selected, the generated code will not reflect the settings of the port mode control register (PMC register).

・ With setting an interval timer
(targets: RL78/G10, RL78/G12, RL78/G13, RL78/G14, RL78/G1A, RL78/G1C, RL78/L12, RL78/L13, RL78/L1C, and RL78/I1A groups)

On the Channel 1 and Channel 3 tabbed pages when "Timer" is selected in the tree view, selecting "Higher and lower 8 bits" under "Interval mode setting" leads to "Generates INTTM01 when counting is started" being grayed out to indicate that it has become non-selectable.

For details of the problem, refer to the URL below.
https://www.renesas.com/en-us/doc/toolnews/eng/2014/140701tn1_e.pdf

7.2.10 RENESAS TOOL NEWS Document No.140816/tn1 (CS+ for CC)(CS+ for CA,CX)

This issue has been corrected in CS+ Code Generator for RL78 (CS+ for CC) (CS+ for CA, CX) V2.05.00.

・ With setting of P20 and P21 of port 2 (target: RL78/L1C group)

For port 2, even if digital input to or output from port pins P20 and P21, which are multiplexed with analog pin functions, is selected, the generated code will not reflect the corresponding settings of the port mode control register (PMC register).

・ With setting of port 1 (target: RL78/G14 group)

When the port pins listed below are selected for port 1, the Code Generator outputs the unnecessary operator and value "| _33_PMC1_DEFAULT". This is because the initial settings for unused bits in the PMC1 register are incorrect.

- P12
- P13
- P16
- P17

For details of the problem, refer to the URL below.
https://www.renesas.com/en-us/doc/toolnews/eng/2014/140816tn1_e.pdf

7.2.11 RENESAS TOOL NEWS Document No.141101/tn2 (CS+ for CC)(CS+ for CA,CX)

This issue has been corrected in CS+ Code Generator for RL78 (CS+ for CC) (CS+ for CA, CX) V2.07.00.

1. Point for Caution on Settings for CPU Stack Pointer Monitoring
(Applicable When Using Products of the RL78/F13 Group)

The order of statements in the procedure for setting the registers for CPU stack pointer monitor function* is erroneous as shown below.

(1) SPM control register (SPMCTRL) <-- This register should be set after step (3).
(2) SP overflow address setting register (SPOFR)
(3) SP underflow address setting register (SPUFR)

Note: CPU stack pointer monitor function is a security function of the MCU.

2. Point for Caution on Writing to the Serial Flag Clear Trigger Register (SIR) When Using 3-wire Serial (CSI) Transfer
(Applicable When Using Products of the RL78/F12 Group)

There was an erroneous statement in the code for writing to the serial flag clear trigger registers listed below. Bit 2 is set to 1, but the correct setting for bit 2 is 0.
SIR00, SIR02, SIR10, and SIRS0 registers

For details of the problem, refer to the URL below.
https://www.renesas.com/en-us/doc/toolnews/eng/2014/141101tn2_e.pdf

7.2.12 RENESAS TOOL NEWS Document No.141216/tn3 (CS+ for CC)(CS+ for CA,CX)

This issue has been corrected in CS+ Code Generator for RL78 (CS+ for CC) (CS+ for CA, CX) V2.07.00.

1. Code Generated for Comparator Settings
(Applicable Products: RL78/I1A Group)

When a comparator is set, code for clock supply is not output.

2. DTC Settings
(Applicable Products: RL78/F13, RL78/F14 Groups)

(1) A project is not saved after code generation when high-speed transfer by the DTC is set.
(2) DTC activating source numbers are not set correctly for the DTC vector addresses.

3. Setting the Voltage Detection Circuit to "Interrupt Mode"
(Applicable Products: RL78/L12, RL78/I1A, RL78/G1A, RL78/F13, and RL78/F14 Groups)

Operation of the voltage detection circuit is in "reset mode" even if "interrupt mode" is selected.

4. Saving Projects with Settings for the A/D Convertor
(Applicable Products: RL78/L1C Group)

When a project configured with the below settings for the A/D convertor is read, the "A fatal error occurred" dialog box is displayed, after which CS+ operation is terminated.
- Selection of analog input pins from among ANI0-ANI2, ANI5, and ANI6:
  ANI0-ANI1
- VREF(+) setting:
  AVREFP
- VREF(-) setting:
  AVREFM

5. Reflection of Pin Configurations in Generated Code
(Applicable Products: RL78/G12, RL78/G13, and RL78/G14 Groups)

When the "Reflect PIN" button is pressed after setting the input/output modes of port pins, "I/O" is always displayed regardless of the selected input/output modes.

For details of the problem, refer to the URL below.
https://www.renesas.com/en-us/doc/toolnews/eng/2014/141216tn3_e.pdf

7.2.13 RENESAS TOOL NEWS Document No.150716/tn2 (CS+ for CC)(CS+ for CA,CX)

This issue has been corrected in CS+ Code Generator for RL78 (CS+ for CC) (CS+ for CA, CX) V2.11.00.

1. Clock Generation Circuit (PLL Circuit Operation)
(Applicable MCUs: RL78/F13, RL78/F14, RL78/G1C, and RL78/L1C groups)

Generated code includes an error when the PLL circuit is operating as the clock generation circuit. A wait is required immediately after setting the PLL control register (PLLCTL).

2. Setting P40 of Port 4
(Applicable MCUs: RL78/F12, RL78/F13, RL78/F14, RL78/G10, RL78/G12, RL78/G13, RL78/G14, RL78/G1A, RL78/G1C, RL78/G1E, RL78/G1F, RL78/G1G, RL78/I1A, RL78/I1D, RL78/L1C, RL78/L12, and RL78/L13 groups)

Generated code has an error when P40 is set such that the on-chip pull-up resistor for P40 is not connected even though this is included in the settings of the on-chip pull-up resistors for port 4. The code to set the pull-up resistor option register (PU4) of P40 is not generated.

3. Code Generated for UART0 and UARTF
(Applicable MCUs: RL78/F12 group)

(a) Generated code has an error when unit 0 of the serial array unit is used as UART0 and its configuration is set to transmission or transmission and reception. Unnecessary code is output to the function void R_UART0_Creat(void) which is in r_cg_serial.c

(b) Generated code has an error in the setting of the LTXD0 pin when the asynchronous serial interface LIN-UART (UARTF) is set for transmission or transmission and reception.
Incorrect code is output to the function void R_UARTF0_Create(void) which is in r_cg_serial.c.

For details of the problem, refer to the URL below.
https://www.renesas.com/doc/toolnews/eng/2015/150716tn2_e.pdf

7.2.14 RENESAS TOOL NEWS Document No.151116/tn2 (CS+ for CC)(CS+ for CA,CX)

This issue has been corrected in CS+ Code Generator for RL78 (CS+ for CC) (CS+ for CA, CX) V2.11.00.

1. Indication of Channels of Serial Interface IICA
(Applicable MCUs: RL78/G14 group R5F104MK, R5F104PK, R5F104ML, and R5F104PL)

Since the GUI does not indicate the channel 1 IICA serial interface for the above products, graphically setting up its operation is impossible. Accordingly, code for channel 1 cannot be generated.

2. Procedure for Setting the PLL Clock
(Applicable MCUs: RL78/F13, RL78/F14, and RL78/F15 groups)

The generated code for setting the PLL clock in the clock generation circuit differs from the example of PLL settings in User's Manual: Hardware for the MCUs and is thus incorrect.

For details of the problem, refer to the URL below.
https://www.renesas.com/doc/toolnews/eng/2015/151116tn2_e.pdf

7.2.15 RENESAS TOOL NEWS Document No.160116/tn5 (CS+ for CC)(CS+ for CA,CX)

This issue has been corrected in CS+ Code Generator for RL78 (CS+ for CC) (CS+ for CA, CX) V2.11.00.

- Transfer of data with a length of 10 or more bits through an element of a serial array unit configured as a CSI or data with a length of 16 bits through an element configured as a UART

(Applicable MCUs: RL78/F12, RL78/F13, RL78/F14, and RL78/F15 groups)

Generated code has an error when an element of a serial array unit is set up for use as a 3-line serial (CSI) port and the length of data is specified as 10 or more bits, or the unit is set up for use as a UART and the length of data is specified as 16 bits.

For details of the problem, refer to the URL below.
https://www.renesas.com/doc/toolnews/eng/2016/160116tn5_e.pdf

7.2.16 RENESAS TOOL NEWS Document No.160216/tn5 (CS+ for CC)(CS+ for CA,CX)

This issue has been corrected in CS+ Code Generator for RL78 (CS+ for CC) (CS+ for CA, CX) V2.11.00.

1. Using the error interrupt of serial array unit 4 as UART4 or DALI4
(Applicable products: RL78/I1A group)

Since the generated code has an error when error interrupts from serial array unit 4 as UART4 or DALI4 (digital addressable lighting interface) are selected, errors cannot be detected.

2. Using serial array unit 4 as DALI4
(Applicable products: RL78/I1A group)

Since the generated code has an error when the length of units for sending is set to 16 bits or the length for reception is set to 16, 17, or 24 bits, and serial array unit 4 is to be used as DALI4, transfer will not operate correctly.

For details of the problem, refer to the URL below.
https://www.renesas.com/doc/toolnews/eng/2016/160216tn5_e.pdf

7.2.17 RENESAS TOOL NEWS Document No.160316/tn1 (CS+ for CC)(CS+ for CA,CX)

This issue has been corrected in CS+ Code Generator for RL78 (CS+ for CC) (CS+ for CA, CX) V2.11.00.

- Pin settings for the IICA serial interface when setting the PIOR to change the assignment of pin functions

(Applicable MCUs: RL78/G12 group (20- and 24-pin products))

When the IICA pin functions are redirected in the following way by setting the peripheral I/O redirection register (PIOR) to change the pin assignment, the generated code for the pin setting will have an error. This makes the IICA clock and data pins unusable with this setting.

(1) In setting the arrangement of pins for the clock generation circuit, select peripheral I/O redirection by checking PIOR2 bit = 1, and click on the button to fix the given pins as the pins to use.

(2) Operation as a single master or as a slave is selected on the IICA0 tabbed page.

For details of the problem, refer to the URL below.
https://www.renesas.com/doc/toolnews/eng/2016/160316tn1_e.pdf

7.2.18 RENESAS TOOL NEWS Document No. R20TS0038EJ0100 (CS+ for CC)(CS+ for CA,CX)

This issue has been corrected in CS+ Code Generator for RL78 (CS+ for CC) (CS+ for CA, CX) V2.12.00.

・ Scan Mode of A/D Converter

RL78 family: RL78/F12, RL78/F13, RL78/F14, RL78/F15, and RL78/G1A groups

The following error dialog boxes might be displayed when the A/D converter is used in serial scan mode or one-shot scan mode, and three or fewer analog input pins are selected.

For details of the problem, refer to the URL below.
https://www.renesas.com/doc/toolnews/eng/2016/r20ts0038ej0100_cstnno.pdf

7.2.19 RENESAS TOOL NEWS Document No. R20TS0045EJ0100 (CS+ for CC)(CS+ for CA,CX)

This issue has been corrected in CS+ Code Generator for RL78 (CS+ for CC) (CS+ for CA, CX) V2.12.00.

1. Peripheral I/O redirection register 0 (PIOR0)

(Applicable MCUs: RL78/G1F group (32- and 36-pin products))

Regarding the common and clock generation circuit pin assignments, code generated by the tools listed above will have an error when the pin assignment setting of bit PIOR02 in the PIOR register should assign the SCLA0 and SDAA0 functions to pins P14 and P15. Thus, the serial interface IICA cannot be used.

For details of the problem, refer to the URL below.
https://www.renesas.com/doc/toolnews/eng/2016/r20ts0045ej0100-cstnno.pdf

7.2.20 RENESAS TOOL NEWS Document No. R20TS0139EJ0100(CS+ for CC)(CS+ for CA,CX)

This issue has been corrected in CS+ Code Generator for RL78 (CS+ for CC) (CS+ for CA, CX) V2.14.00.

1. Input of Ports P10 and P11.
RL78 family: RL78/G13 group (20, 24 and 25-pin products)
In the port settings for applicable products, Ports P10 and P11 cannot be set for the TTL input buffer because the TTL buffer setting column is not provided for these ports.

2. Port Settings Related to Reset Processing
RL78 family: RL78/F12 group (20-pin products)
The products do not support software processing for port P120 described in the RL78/F12 user's manual.
For details of the problem, refer to the URL below.
https://www.renesas.com/doc/toolnews/eng/2017/r20ts0139ej0100-cstnn.pdf

7.2.21 RENESAS TOOL NEWS Document No. R20TS0244EJ0100 (CS+ for CC)(CS+ for CA,CX)

This issue has been corrected in CS+ Code Generator for RL78 (CS+ for CC) (CS+ for CA, CX) V2.16.00.

1. When Continuous Transfer Mode is Selected in the CSI Configuration
RL78 Family: RL78/D1A, RL78/F12, RL78/F13, RL78/F14, RL78/F15, and RL78/L12 groups

When CSI transmission or CSI transmission/reception is selected in applicable products and "continuous transfer mode" is selected for the "transfer mode settings", an additional setting is required for the output code.

For details of the problem, refer to the URL below.
https://www.renesas.com/doc/toolnews/eng/2017/r20ts0244ej0100-cstnno.pdf

7.2.22 RENESAS TOOL NEWS Document No. R20TS0290EJ0100 (CS+ for CC)(CS+ for CA,CX)

This issue has been corrected in CS+ Code Generator for RL78 (CS+ for CC) (CS+ for CA, CX) V2.16.00.

1. When Opening a Project for RL78/G11 Created by a Previous Version of Code Generator
1.1 Applicable Products
・V2.15.00 of the CS+ Code Generator for RL78 (V6.01 of CS+ for CC)
・V2.15.00 of the CS+ Code Generator for RL78 (V6.01 of CS+ for CA,CX)

1.2 Applicable MCUs
RL78 family: RL78/G11 group (20-pin R5F1056A)

When an attempt is made to open a project for RL78/G11 (R5F1056A) created by any of the following previous versions of code generator using a product shown in section 1.1, an error occurs and the project cannot be opened.

For details of the problem, refer to the URL below.
https://www.renesas.com/doc/toolnews/eng/2018/r20ts0290ej0100-cstnno.pdf

7.2.23 RENESAS TOOL NEWS Document No. R20TS0313EJ0100 (CS+ for CC)(CS+ for CA,CX)

This issue has been corrected in CS+ Code Generator for RL78 (CS+ for CC) (CS+ for CA, CX) V2.16.00.

1. Writing to Port-Related Registers for Unused Pins
RL78 family: RL78/I1D group

When using the applicable products to generate code for the port function, the following unnecessary register settings are made for the unused pins in a port when the mode (input or output) of each pin in the port is set. Because of this, the unused pins in the port output unintended data.

For details of the problem, refer to the URL below.
https://www.renesas.com/doc/toolnews/eng/2018/r20ts0313ej0100-cstnno.pdf

7.2.24 RENESAS TOOL NEWS Document No. R20TS0370EJ0100 (CS+ for CC)(CS+ for CA,CX)

This issue has been corrected in CS+ Code Generator for RL78 (CS+ for CC) (CS+ for CA, CX) V2.17.00.

1. When setting the Serial UART4
1.1 Applicable MCUs
RL78 family: RL78/I1A group

For details of the problem, refer to the URL below.
https://www.renesas.com/search/keyword-search.html#genre=document&q=r20ts0370

Chapter 8. Adding the API working with the Data Flash Library

8.1 The API controlling the Data Flash Library

API Function Name	Function
R_FDL_Create	Performs the initialization processing required to control the Data Flash Library
R_FDL_Open	Starts using the Data Flash Library
R_FDL_Close	Ends using the Data Flash Library
R_FDL_Write	Writes to the Data Flash
R_FDL_Read	Reads from the Data Flash
R_FDL_Erase	Erases from the Data Flash

Any of the following Data Flash Libraries needs to be installed.

Data Flash Library Type04 for the CC-RL Compiler for RL78 Family, Japan Release

Data Flash Library Type04 for the CA78K0R Compiler for RL78 Family, Japan Release

https://www.renesas.com/en-us/products/software-tools/tools/self-programming-library/data-flash-libraries.html

Read the document included in the above before using the devices.

R_FDL_Create

Performs only variable assignment required to control the Data Flash Library Tpye04.

As the function is automatically called from the startup processing, the users do not need a function call.

[File Name]

r_cg_pfdl.c

[Syntax]

```
void R_FDL_Create ( void );
```

[Argument(s)]

None.

[Return value]

None.

R_FDL_Open

Opens the driver to use the Data Flash Library. R_FDL_Write, R_FDL_Read, and R_FDL_Erase commands work in open state.

[File Name]

r_cg_pfdl.c

[Syntax]

```
void R_FDL_Open ( void );
```

[Argument(s)]

None.

[Return value]

None.

R_FDL_Close

Closes the driver of the Data Flash Library. To use the Data Flash Library again, open processing (R_FDL_Open) is required.

[File Name]

r_cg_pfdl.c

[Syntax]

```
void R_FDL_Close ( void );
```

[Argument(s)]

None.

[Return value]

None.

R_FDL_Write

Writes to the Data Flash Library. No blank check is done, but it checks the control state of the data flash memory, and waits when running command (PFDL_BUSY).
FDL works in open state.

[File Name]

r_cg_pfdl.c

[Syntax]

```
pfdl_status_t R_FDL_Write ( pfdl_u16 index, __near pfdl_u08* buffer, pfdl_u16 bytecount );
```

[Argument(s)]

index	write Data Flash address	0000-0FFFh
buffer	buffer of write data	
bytecount	write count	

[Return value]

pfdl_status reffer pfdl.inc

```
        ; operation related status code
PFDL_OK                 .EQU    000H
PFDL_IDLE               .EQU    030H
PFDL_BUSY               .EQU    0FFH
        ; flash access related status code
PFDL_ERR_PROTECTION     .EQU    010H
PFDL_ERR_ERASE          .EQU    01AH
PFDL_ERR_MARGIN         .EQU    01BH
PFDL_ERR_WRITE          .EQU    01CH
PFDL_ERR_PARAMETER      .EQU    005H
```

R_FDL_Read

Reads from the Data Flash. Does not check the control state of the data flash memory. FDL works in open state.

[File Name]

r_cg_pfdl.c

[Syntax]

```
pfdl_status_t R_FDL_Read(pfdl_u16 index, __near pfdl_u08* buffer, pfdl_u16 bytecount );
```

[Argument(s)]

index	read Data Flash address
buffer	buffer of read data
bytecount	read count

[Return value]

pfdl_status reffer pfdl.inc (same R_FDL_Write)

R_FDL_Erase

Erases from the Data Flash. In case of an error, a return value can't write notes to a target block. When writing notes in the block an error generated, it's necessary to carry out this command and make them normally end once again.

[File Name]

r_cg_pfdl.c

[Syntax]

```
pfdl_status_t R_FDL_Erase(pfdl_u16 blockno );
```

[Argument(s)]

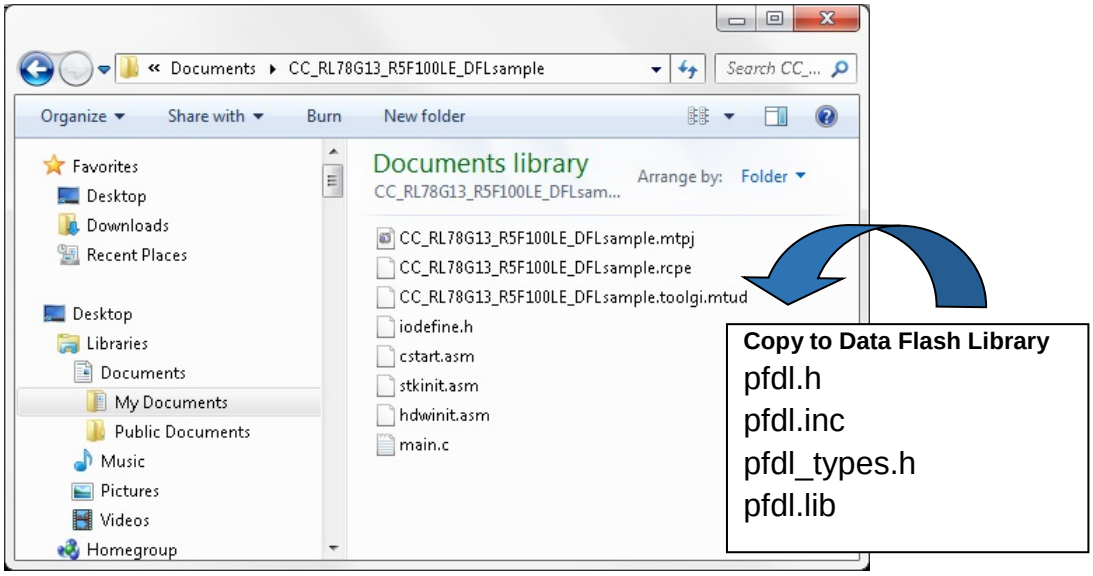
blockno	0-3

[Return value]

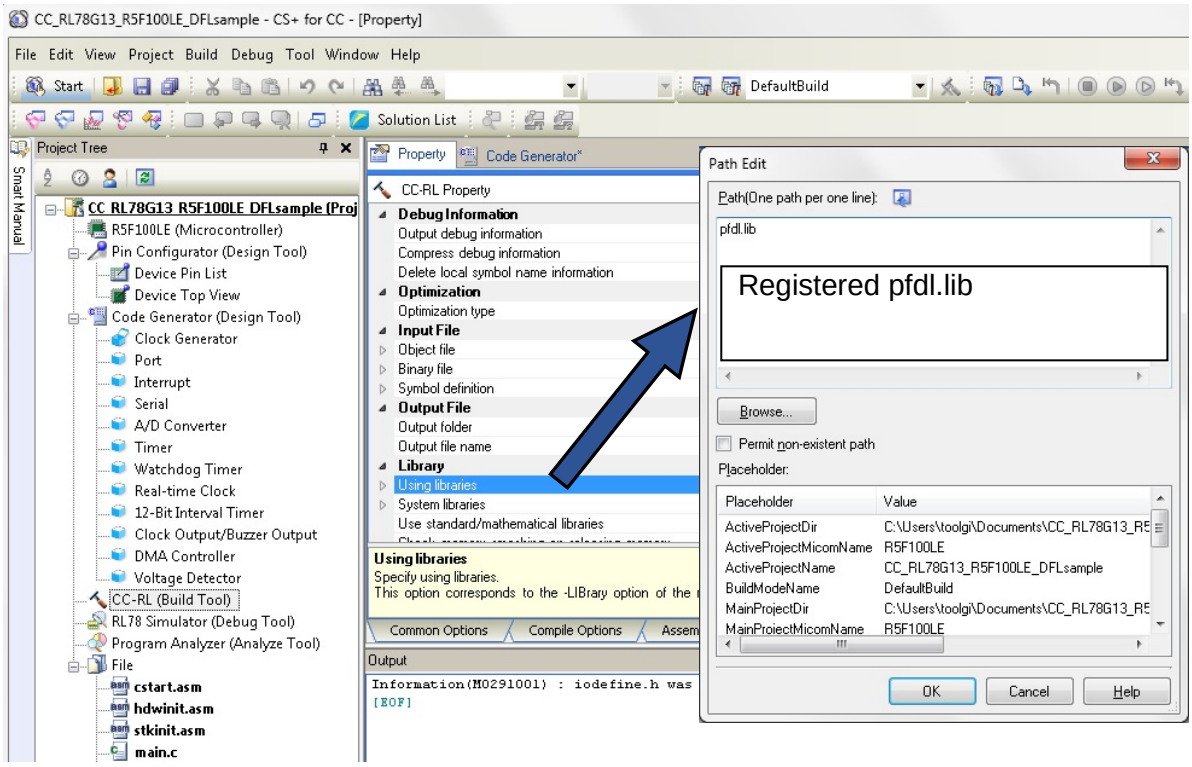
pfdl_status	reffer pfdl.inc (same R_FDL_Write)

8.2 Sample use(CC-RL)

8.2.1 Install of Data Flash Library



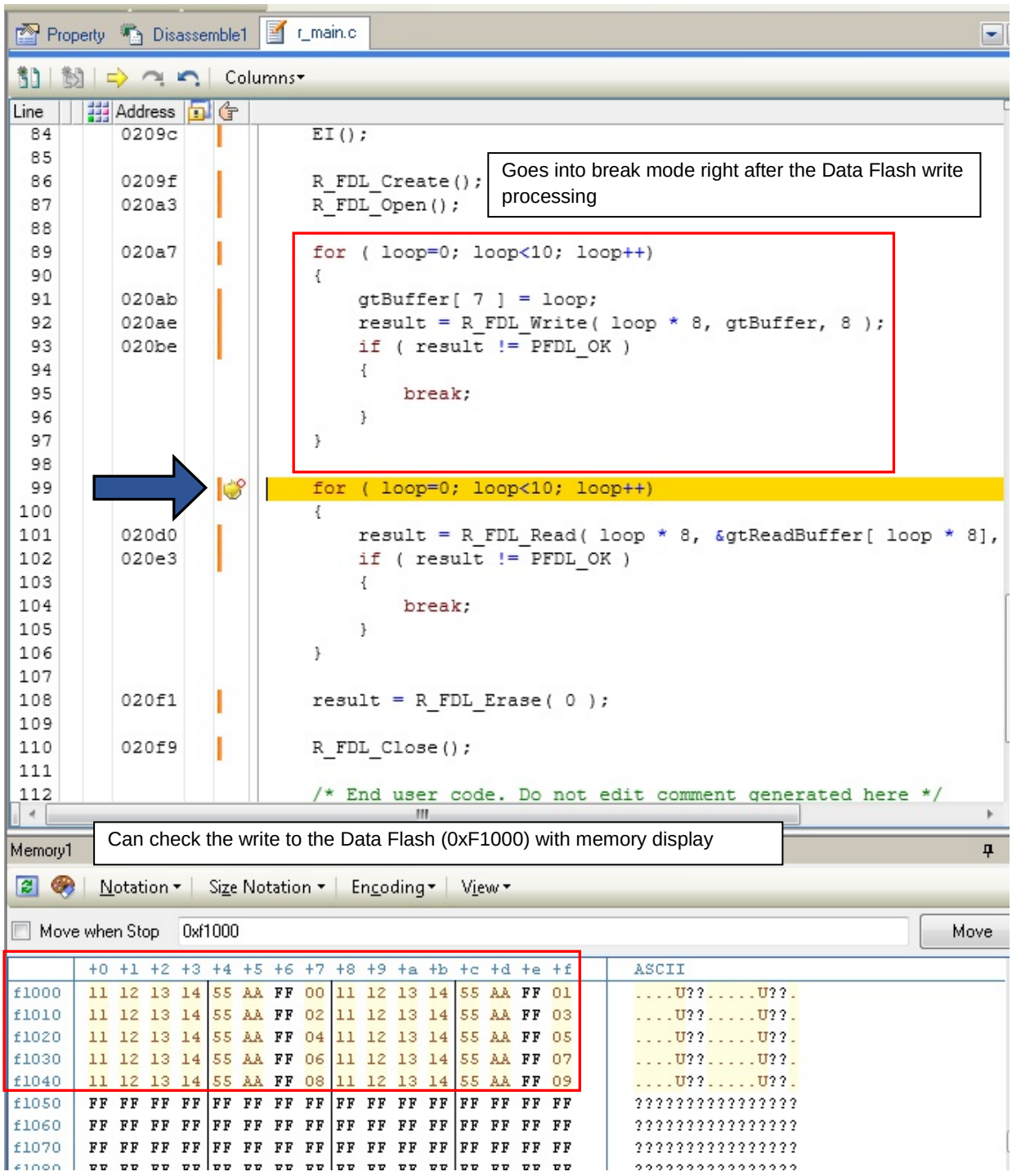
8.2.2 The Data Flash Library is registered with build tool



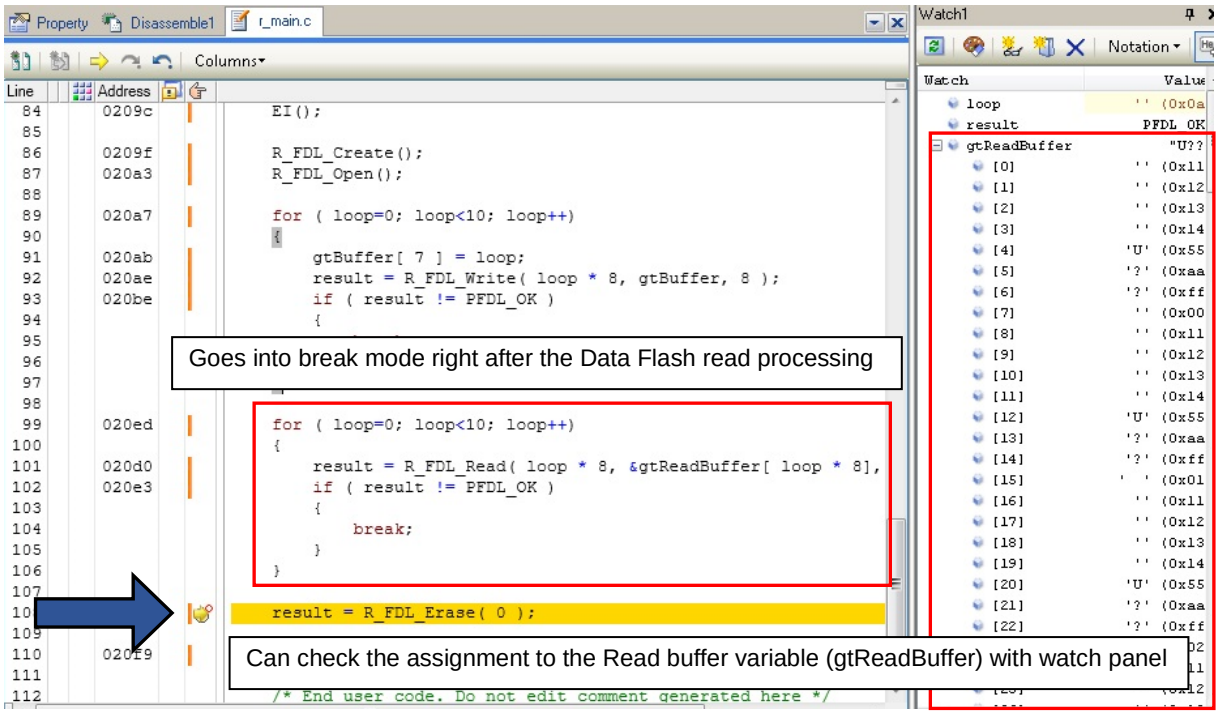
8.2.3 Edit r_main.c (Red is additional code)

```
/***********************************************************************************
Pragma directive
***********************************************************************************/
/* Start user code for pragma. Do not edit comment generated here */
pfdl_status_t result;
uint8_t loop;
static pfdl_u08 gtBuffer[] = { 0x11, 0x12, 0x13, 0x14, 0x55, 0xAA, 0xFF, 0x00 };
static pfdl_u08 gtReadBuffer[ 128 ];
/* End user code. Do not edit comment generated here */
      Abbreviation
void main(void)
      Abbreviation
/***********************************************************************************
* Function Name: R_MAIN_UserInit
* Description  : This function adds user code before implementing main function.
***********************************************************************************/
void R_MAIN_UserInit(void)
{
   /* Start user code. Do not edit comment generated here */
   EI();
   R_FDL_Create();
   R_FDL_Open();
   /* write Data Write */
   for ( loop=0; loop<10; loop++)
   {
      gtBuffer[ 7 ] = loop;
      result = R_FDL_Write( loop * 8, gtBuffer, 8 );
      if ( result != PFDL_OK )
      {
         break;
      }
   }
   /* read Data Flash */
     for ( loop=0; loop<10; loop++)
      {
            result = R_FDL_Read( loop * 8, &gtReadBuffer[ loop * 8], 8 );
            if ( result != PFDL_OK )
            {
               break;
            }
      }
   /* erase Data Flash */
      result = R_FDL_Erase( 0 );
      R_FDL_Close();
      /* End user code. Do not edit comment generated here */
}
```

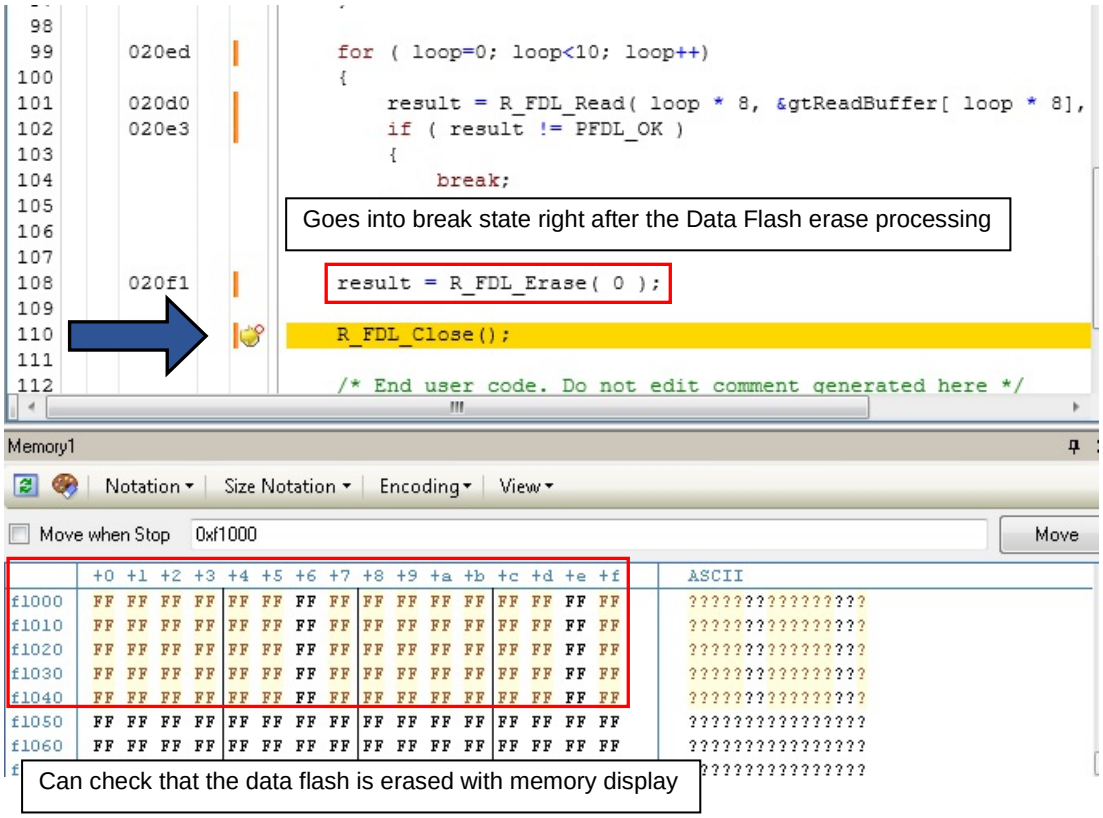
8.2.4 Function check on the QB-R5F100LE-TB (Write)



8.2.5 Function check on the QB-R5F100LE-TB (Read)



8.2.6 Function check on the QB-R5F100LE-TB (Erase)



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