CS+ Code Generator for RX V1.16.00

Release Note

R20UT4345EJ0201
Rev. 2.01
Jun. 28, 2019

Introduction

Thank you for using the AP4 for RX (the name has been changed from Application Leading Tool for RX).
This document describes the restrictions and points for caution regarding this product. Read this document before using the product.

Contents

Chapter 1. Introduction

The AP4 for RX is a software tool for generating control programs (device driver programs) for peripheral modules (timers, UARTs, A/D converters, etc.). It generates device driver code from user settings made through a GUI. Other than the code for initializing the peripheral modules, API (Application Programming Interface) functions for operating the peripheral modules are provided.

1.1 System Requirements

The operating environment is as listed below.

1.1.1 PC

- IBM PC/AT compatible (with Windows® 7, Windows® 8.1, or Windows® 10)
- Processor: At least 1 GHz (the product supports hyper-threading and multi-core CPUs)
- Memory capacity: 2 GB or more is recommended. At least 1 GB (or 2 GB for 64-bit versions of Windows®) is required.
- Hard disk capacity: At least 200 MB available
- Display resolution: 1024x768 or higher; at least 65536 colors
- Required elements of the software environment other than the Windows OS: .NET Framework 4.5 plus a language pack

1.1.2 Development tools

- Integrated development environment CS+ from Renesas, V6.01.00 or later
- CC-RX compiler from Renesas, V2.07.00 or later

Chapter 2. Supported Devices

2.1 Target Devices

The devices supported by the CS+ Code Generator for RX V1.16.00 are listed below.

Table 1-1 Supported devices

Group (HWM number)	Number of pins	Device name
RX110 group (R01UH0421EJ0100)	36 pins	R5F5110HAxLM, R5F5110JAxLM, R5F51101AxLM, R5F51103AxLM
	40 pins	R5F5110HAxNF, R5F5110JAxNF, R5F51101AxNF, R5F51103AxNF
	48 pins	R5F5110JAxFL, R5F5110JAxNE, R5F51101AxFL, R5F51101AxNE, R5F51103AxFL, R5F51103AxNE, R5F51104AxFL ,R5F51104AxNE, R5F51105AxFL ,R5F51105AxNE
	64 pins	R5F5110JAxFK, R5F5110JAxFM, R5F5110JAxLF, R5F51101AxFK, R5F51101AxFM, R5F51101AxLF, R5F51103AxFK, R5F51103AxFM, R5F51103AxLF, R5F51104AxFK, R5F51104AxFM, R5F51104AxLF, R5F51105AxFK, R5F51105AxFM, R5F51105AxLF
RX111 group (R01UH0365EJ0120)	36 pins	R5F51111AxLM, R5F51113AxLM, R5F5111JAxLM
	40 pins	R5F51111AxNF, R5F51113AxNF, R5F5111JAxNF
	48 pins	R5F5110JAxFLR5F51101AxNE, R5F51103AxNE, R5F51104AxNE, R5F51105AxNE, R5F5110JAxNE, R5F51101AxFL, R5F51101AxNE, R5F51103AxFL, R5F51103AxNE, R5F51104AxFL ,R5F51104AxNE, R5F51105AxFL ,R5F51105AxNE, R5F5110JAxFL
	64 pins	R5F5110JAxFK, R5F5110JAxFMR5F51101AxLF, R5F51103AxLF, R5F51104AxLF, R5F51105AxLF, R5F5110JAxLF, R5F51101AxFK, R5F51103AxFK, R5F51104AxFK, R5F51105AxFK, R5F5110JAxFK, R5F51101AxFM, R5F51101AxLF, R5F51103AxFK, R5F51103AxFM, R5F51103AxLF, R5F51104AxFK, R5F51104AxFM, R5F51104AxLF, R5F51105AxFK, R5F51105AxFM, R5F51105AxLFR5F5110JAxFM
RX113 group (R01UH0448EJ0100)	64 pins	R5F51135AxFM, R5F51136AxFM, R5F51137AxFM, R5F51138AxFM
	100 pins	R5F51135AxLJ, R5F51136AxLJ, R5F51137AxLJ, R5F51138AxLJ, R5F51135AxFP, R5F51136AxFP, R5F51137AxFP, R5F51138AxFP
RX130 group (R01UH0560EJ0100)	48 pins	R5F51303AxFL, R5F51305AxFL, R5F51303AxNE, R5F51305AxNE
	64 pins	R5F51303AxFM, R5F51305AxFM, R5F51303AxFK, R5F51305AxFK
	80 pins	R5F51303AxFN, R5F51305AxFN
RX230 group (R01UH0496EJ0110)	48 pins	R5F52305AxNE, R5F52306AxNE, R5F52305AxFL, R5F52306AxFL
	64 pins	R5F52305AxND, R5F52306AxND, R5F52305AxFM, R5F52306AxFM, R5F52305AxLF, R5F52306AxLF
	100 pins	R5F52305AxLA, R5F52306AxLA, R5F52305AxFP, R5F52306AxFP

Table 1-2 Supported Devices

Group (HWM number)	Number of pins	Device name
RX231 group (R01UH0496EJ0110)	48 pins	R5F52315AxNE, R5F52316AxNE, R5F52317AxNE, R5F52318AxNE, R5F52315CxNE, R5F52316CxNE, R5F52317BxNE, R5F52318BxNE, R5F52315AxFL, R5F52316AxFL, R5F52317AxFL, R5F52318AxFL, R5F52315CxFL, R5F52316CxFL, R5F52317BxFL, R5F52318BxFL
	64 pins	R5F52315AxND, R5F52316AxND, R5F52317AxND, R5F52318AxND, R5F52315CxND, R5F52316CxND, R5F52317BxND, 5F52318BxND, R5F52315AxFM, R5F52316AxFM, R5F52317AxFM, R5F52318AxFM, R5F52315CxFM, R5F52316CxFM, R5F52317BxFM, 5F52318BxFM, R5F52315CxLF, R5F52316CxLF
	100 pins	R5F52315AxLA, R5F52316AxLA, R5F52317AxLA, R5F52318AxLA, R5F52315CxLA, R5F52316CxLA, R5F52317BxLA, R5F52318BxLA, R5F52315AxFP, R5F52316AxFP, R5F52317AxFP, R5F52318AxFP, R5F52315CxFP, R5F52316CxFP, R5F52317BxFP, R5F52318BxFP
RX23T group (R01UH0520EJ0110)	48 pins	R5F523T3AxFL, R5F523T5AxFL
	52 pins	R5F523T3AxFD, R5F523T5AxFD
	64 pins	R5F523T3AxFM, R5F523T5AxFM
RX24T group (R01UH0576EJ0200)	64 pins	R5F524T8AxFM, R5F524TAAxFM
	80 pins	R5F524TAAxFF, R5F524T8AxFF, R5F524TAAxFN, R5F524T8AxFN
	100 pins	R5F524T8AxFP, R5F524TAAxFP, R5F524TBAxFP, R5F524TCAxFP, R5F524TEAxFP
RX24U group (R01UH0658EJ0100)	100 pins	R5F524UBAxFP, R5F524UCAxFP, R5F524UEAxFP
	144 pins	R5F524UBAxFB, R5F524UCAxFB, R5F524UEAxFB
RX64M group (R01UH0377EJ0100)	100 pins	R5F564MFCxLJ, R5F564MFDxLJ, R5F564MGCxLJ, 5F564MGDxLJ, R5F564MJCxLJ, R5F564MJDxLJ, R5F564MLCxLJ, R5F564MLDxLJ, R5F564MFCxFP, R5F564MFDxFP, R5F564MGCxFP, R5F564MGDxFP, R5F564MJCxFP, R5F564MJDxFP, R5F564MLCxFP, R5F564MLDxFP
	144/145 pins	R5F564MFCxFB, R5F564MFDxFB, R5F564MGCxFB, R5F564MGDxFB, R5F564MJCxFB, R5F564MJDxFB, R5F564MLCxFB, R5F564MLDxFB, R5F564MFCxLK, R5F564MFDxLK, R5F564MGCxLK, R5F564MGDxLK, R5F564MJCxLK, R5F564MJDxLK, R5F564MLCxLK, R5F564MLDxLK
	176/177 pins	R5F564MFCxFC, R5F564MFDxFC, R5F564MGCxFC, R5F564MGDxFC, R5F564MJCxFC, R5F564MJDxFC, R5F564MLCxFC, R5F564MLDxFC, R5F564MFCxLC, R5F564MFDxLC, R5F564MGCxLC, R5F564MGDxLC, R5F564MJCxLC, R5F564MJDxLC, R5F564MLCxLC, R5F564MLDxLC, R5F564MFCxBG, R5F564MFDxBG, R5F564MGCxBG, R5F564MGDxBG, R5F564MJCxBG, R5F564MJDxBG, R5F564MLCxBG, R5F564MLDxBG

Table 1-3 Supported devices

Group (HWM number)	Number of pins	Device name
RX65N group (R01UH0590EJ0100)	100 pins	R5F565N9AxLJ, R5F565N9BxLJ, R5F565N9ExLJ, R5F565N9FxLJ, R5F565N7AxLJ, R5F565N7BxLJ, R5F565N7ExLJ, R5F565N7FxLJ, R5F565N4AxLJ, R5F565N4BxLJ, R5F565N4ExLJ, R5F565N4FxLJ, R5F565N9AxFP, R5F565N9BxFP, R5F565N9ExFP, R5F565N9FxFP, R5F565N7AxFP, R5F565N7BxFP, R5F565N7ExFP, R5F565N7FxFP, R5F565N4AxFP, R5F565N4BxFP, R5F565N4ExFP, R5F565N4FxFP
	144/145 pins	R5F565N9AxFB, R5F565N9BxFB, R5F565N9ExFB, R5F565N9FxFB, R5F565N7AxFB, R5F565N7BxFB, R5F565N7ExFB, R5F565N7FxFB, R5F565N4AxFB, R5F565N4BxFB, R5F565N4ExFB, R5F565N4FxFB, R5F565N9AxLK, R5F565N9BxLK, R5F565N9ExLK, R5F565N9FxLK, R5F565N7AxLK, R5F565N7BxLK, R5F565N7ExLK, R5F565N7FxLK, R5F565N4AxLK, R5F565N4BxLK, R5F565N4ExLK, R5F565N4FxLK
RX651 group (R01UH0590EJ0100)	100 pins	R5F56519AxLJ, R5F56519BxLJ, R5F56519ExLJ, R5F56519FxLJ, R5F56517AxLJ, R5F56517BxLJ, R5F56517ExLJ, R5F56517FxLJ, R5F56514AxLJ, R5F56514BxLJ, R5F56514ExLJ, R5F56514FxLJ, R5F56519AxFP, R5F56519BxFP, R5F56519ExFP, R5F56519FxFP, R5F56517AxFP, R5F56517BxFP, R5F56517ExFP, R5F56517FxFP, R5F56514AxFP, R5F56514BxFP, R5F56514ExFP, R5F56514FxFP
	144/145 pins	R5F56519AxFB, R5F56519BxFB, R5F56519ExFB, R5F56519FxFB, R5F56517AxFB, R5F56517BxFB, R5F56517ExFB, R5F56517FxFB, R5F56514AxFB, R5F56514BxFB, R5F56514ExFB, R5F56514FxFB, R5F56519AxLK, R5F56519BxLK, R5F56519ExLK, R5F56519FxLK, R5F56517AxLK, R5F56517BxLK, R5F56517ExLK, R5F56517FxLK, R5F56514AxLK, R5F56514BxLK, R5F56514ExLK, R5F56514FxLK
RX71M group (R01UH0493EJ0100)	100 pins	R5F571MLCxFP, R5F571MLDxFP, R5F571MLGxFP, R5F571MLHxFP, R5F571MJCxFP, R5F571MJDxFP, R5F571MJGxFP, R5F571MJHxFP, R5F571MGCxFP, R5F571MGDxFP, R5F571MGGxFP, R5F571MGHxFP, R5F571MFCxFP, R5F571MFDxFP, R5F571MFGxFP, R5F571MFHxFP, R5F571MLCxLJ, R5F571MLDxLJ, R5F571MLGxLJ, R5F571MLHxLJ, R5F571MJCxLJ, R5F571MJDxLJ, R5F571MJGxLJ, R5F571MJHxLJ, R5F571MGCxLJ, R5F571MGDxLJ, R5F571MGGxLJ, R5F571MGHxLJ, R5F571MFCxLJ, R5F571MFDxLJ, R5F571MFGxLJ, R5F571MFHxLJ
	144/145 pins	R5F571MLCxLK, R5F571MLDxLK, R5F571MLGxLK, R5F571MLHxLJ, R5F571MJCxLK, R5F571MJDxLK, R5F571MJGxLK, R5F571MJHxLK, R5F571MGCxLK, R5F571MGDxLK, R5F571MGGxLK, R5F571MGHxLK, R5F571MFCxLK, R5F571MFDxLK, R5F571MFGxLK, R5F571MFHxLK, R5F571MLCxFB, R5F571MLDxFB, R5F571MLGxFB, R5F571MLHxFB, R5F571MJCxFB, R5F571MJDxFB, R5F571MJGxFB, R5F571MJHxFB, R5F571MGCxFB, R5F571MGDxFB, R5F571MGGxFB, R5F571MGHxFB, R5F571MFCxFB, R5F571MFDxFB, R5F571MFGxFB, R5F571MFHxFB
	176/177 pins	R5F571MLCxFC, R5F571MLDxFC, R5F571MLGxFC, R5F571MLHxFC, R5F571MJCxFC, R5F571MJDxFC, R5F571MJGxFC, R5F571MJHxFC, R5F571MGCxFC, R5F571MGDxFC, R5F571MGGxFC, R5F571MGHxFC, R5F571MFCxFC, R5F571MFDxFC, R5F571MFGxFC, R5F571MFHxFC, R5F571MLCxLC, R5F571MLDxLC, R5F571MLGxLC, R5F571MLHxLC, R5F571MJCxLC, R5F571MJDxLC, R5F571MJGxLC, R5F571MJHxLC, R5F571MGCxLC, R5F571MGDxLC, R5F571MGGxLC, R5F571MGHxLC, R5F571MFCxLC, R5F571MFDxLC, R5F571MFGxLC, R5F571MFHxLC, R5F571MLCxBG, R5F571MLDxBG, R5F571MLGxBG, R5F571MLHxBG, R5F571MJCxBG, R5F571MJDxBG, R5F571MJGxBG, R5F571MJHxBG, R5F571MGCxBG, R5F571MGDxBG, R5F571MGGxBG, R5F571MGHxBG, R5F571MFCxBG, R5F571MFDxBG, R5F571MFGxBG, R5F571MFHxBG

Chapter 3. User's Manuals

Please read me the following user's manuals together with this document.

Manual Name	Doument Number
Code Generator RX API Reference	R20UT4324
CS+ Code Generator Peripheral Function Operation	R20UT3104
CS+ Code Generator Pin View	R20UT3105
CS+ V7.00.00 Message	R20UT4309

Chapter 4. Uninstallation

There are two ways to ininstall this product.

- Use the integrated uninstaller from Renesas (uninstalls all CS+ components)
- Use the Windows uninstaller (only uninstalls this product only)

To use the Windows uninstaller, select "CS+ Code Generator for RX" from "Programs and Feature" of the control panel.

Chapter 5. Changes

This chapter describes changes to the CS+ Code Generator for RX V1.16.00.

5.1 List of Changes

No	Description	Version *1									
		RX110 V1.06.02.04	RX111 V1.06.02.04	RX113 V1.03.02.04	RX130 V1.01.02.04	RX230, RX231 V1.01.02.05	RX23T V1.01.02.03	RX24T, RX24U V1.03.02.04	RX64M V1.03.02.03	RX65N, RX651 V1.01.02.03	RX71M V1.01.02.03
1	Initialization of port direction register (PDR) of RX130	/	/	/	○	/	/	/	/	/	/

○: Applicable, /: Not applicable

*1: These version numbers are stated in the file headers of the source code which is generated by the code generator.

5.2 Details of the Changes

5.2.1 Initialization of port direction register (PDR) of RX130

The following points are no longer applicable.

To initialize the port direction register (PDR), the reserved bit needs to be set(Note) to "1" (output). However, even if it is set to "1", an initialization processing code is not generated.

For 64-pin package, PORTD initialization processing is not generated, and for 48-pin package, PORT0, PORT5, and PORTD initialization processing is not generated.

Note: The input-only P35 pin is set to “0” (input).

Refer to Tool News (R20TS0273) for the details.

Chapter 6. History of Corrections Announced in Renesas Tool News

This section is a summary of corrections announced in Renesas Tool News.

Issue Date	Document No.	Description	Device Concerned	Fixed Version
Mar. 01, 2015	150301/tn2	1. Multifunction Timer Pulse Unit 3	RX64M	V1.06.00
		2. Serial Communications Interface	RX111, RX113, RX64M, RX71M	
May 16, 2015	150516/tn1	1. Code Generated for the Clock Generation Circuit (PLL Circuit Operation)	RX111, RX113	V1.06.00
		2. Bus Settings	RX64M, RX71M	
		3. 16-bit Timer Pulse Unit (TPUa) and Multifunction Timer Pulse Unit 3 (MTU3a)	RX64M, RX71M	
		4. 12-bit A/D Converter (S12ADC)	RX64M, RX71M	V1.08.00
		5. 12-bit D/A Converter (R12DA)	RX64M, RX71M	
Jul. 16, 2015	150716/tn1	1. Bus Settings	RX64M, RX71M	V1.08.00
		2. Code Generated for the Clock Generation Circuit (HOCO Operation)	RX111, RX113	
Aug. 07, 2015	150807/tn3	Complementary PWM mode setting of the MTU	RX230, RX231	V1.08.00
Sep. 01, 2015	150901/tn2	Interrupts when the MTU is set for complementary PWM mode	RX110, RX111, RX113, RX23T, RX230, RX231	V1.08.00
Nov. 01, 2015	151101/tn4	1. Setting to permit or prohibit suspension of transfer in response to the reception of NACK over the I2C bus interface (RIIC)	RX110, RX111, RX113, RX23T, RX230, RX231, RX64M, RX71M	V1.09.00
		2. Settings for the output of RTCOUT from the real time clock (RTC)	RX110, RX111, RX113	
		3. Setting of the data transfer controller (DTC)	RX110, RX111, RX113, RX23T, RX230, RX231, RX64M, RX71M	V1.08.00
Dec. 01, 2015	151201/tn3	Using the Multi-Function Pin Controller (MPC) to Select Functions of the PAn Pins	RX113	V1.08.00
Feb. 16, 2016	160216/tn4	FIFO embedded Serial Communications Interface SCIFA10	RX64M, RX71M	V1.09.00
Jun. 16, 2016	R20TS0039	1. Serial Communications Interface SCI6	RX231, RX230	V1.10.00
Nov. 01, 2016	R20TS0087	1. Selection of the MTIOC3 pin for MTU3 in Multi-Function Timer Pulse Unit 3	RX64M, RX71M	V1.11.00
		2. Low-speed On-chip Oscillator (LOCO) when Low Power Consumption (LPC) is Specified	RX64M, RX65N, RX651, RX71M	V1.11.00
Mar. 01, 2017	R20TS0140	1. Port Direction Register (PDR) Settings	RX231, RX230	V1.12.00

Issue Date	Document No.	Description	Device Concerned	Fixed Version
Apr. 16, 2017	R20TS0161	1. Prohibition of Reading from and Writing to Registers Protected from Programming by Mistake in Multi-function Timer Pulse Unit 2 (MTU2) and 3 (MTU3)	RX110, RX111, RX113, RX23T, RX230, RX231, RX24T, RX24U, RX64M, RX71M	V1.14.00
		3. LCD Initialization Code	RX113	V1.13.00
Sep. 01, 2017	R20TS0197	1. When Using the I^2C Bus Interface in Slave Mode	All groups	V1.14.00
Feb. 16, 2018	R20TS0273	1. Initialization of Port Direction Register (PDR) of RX130	RX130	V1.15.00

Chapter 7. Points for Caution

This section describes points for caution regarding the CS+ Code Generator for RX V1.16.00. Refer to the documents for the individual modules for points for caution regarding the FIT modules.

7.1 List of Points for Caution

Table 4 List of Points for Caution

No	Description	Version *1									
		RX110 V1.06.02.04	RX111 V1.06.02.04	RX113 V1.03.02.04	RX130 V1.01.02.04	RX230, RX231 V1.01.02.05	RX23T V1.01.02.03	RX24T, RX24U V1.03.02.04	RX64M V1.03.02.03	RX65N, RX651 V1.01.02.03	RX71M V1.01.02.03
1	Online help	○	○	○	○	○	○	○	○	○	○
2	USB	/	○	○	/	○	/	/	○	○	○
3	Serial communications interface asynchronous mode	○	○	○	○	○	○	○	○	○	○
4	Processor mode	○	○	○	○	○	○	○	○	○	○
5	I^2C bus interface	/	/	○	○	○	○	○	○	○	○
6	Initial operation with low power consumption	○	○	○	/	/	/	/	/	/	/
7	Setting when the USB clock is not to be used	/	/	/	/	/	/	/	○	○	○
8	How to specify slave addresses of an SCI running in simple I^2C mode	○	○	○	○	○	○	○	○	○	○
9	Setting the system clock (ICLK) to a Frequency Higher than 32 MHz	/	/	/	/ *2	○ *2	○ *2	/	/	/	/
10	Dead-time compensation	/	○	○	○	○	○	○	○	/	○
11	Realtime clock	○	○	○	○	○	○	○	○	/	○
12	SPI clock synchronous mode	/	/	/	○	○	/	/	○	/	○
13	SCI/SCIF clock synchronous mode	/	/	/	/	/	/	/	○	○	○
14	All-module clock-stop function	/	/	/	/	/	/	/	○	○	○
15	Using the Voltage Detection Circuits	○	○	○	○	○	○	○	/	/	/
16	When the LCD Controller/Driver and I/O Ports, PB3 and PB5 are Set	/	/	○	/	/	/	/	/	/	/

○: Applicable, /: Not applicable

*1: The version numbers are stated in the file headers of the source code which is generated by the code generator.

*2: Refer to FAQ when using previous version smart configurator.

7.2 Details of Points for Caution

7.2.1 Online help

AP4 for RX does not support online help.

7.2.2 USB

AP4 for RX does not support the USB interface.

7.2.3 Serial communications interface asynchronous mode

AP4 for RX does not support the input of a transfer rate clock from the TMR or MTU in the asynchronous mode of the Serial Communications Interface.

7.2.4 Processor mode

RX CPUs have two processor modes: supervisor and user. The API driver functions may be assumed to operate with the CPU in supervisor mode.
More information on the processor modes can be found in the RX Family software manual.

7.2.5 I²C bus interface

The code generator does not support detecting the host address in slave mode or the multi-master operation of the I²C bus interface (RIIC).

7.2.6 Initial operation with low power consumption

“Middle-speed mode” can be selected for the initial operation with low power consumption even if the system clock (ICLK) is set to a frequency above 12 MHz. In practice, however, be sure to set the initial operation with low power consumption to “High-speed mode” when ICLK is set to a frequency above 12 MHz.

7.2.7 Setting when the USB clock is not to be used

When the USB clock is not to be used, set the USB clock (UCLK) selection bits to "0001" (x1/2) after the code has been generated.

7.2.8 How to specify slave addresses of an SCI running in simple I²C mode

When an SCI is running in simple I²C mode, specify the slave address in the seven higher-order bits of the argument adr, and set the lowest-order bit to "1" for master transmission or to "0" for master reception.

b7	b6	b5	b4	b3	b2	b1	b0
Slave address							R/W *1

*1: Readable =1, Writable = 0

Functions: R_SCIx_IIC_Master_Send, R_SCIx_IIC_Master_Receive

7.2.9 Setting the system clock (ICLK) to a Frequency Higher than 32 MHz

When the system clock (ICLK) is set to a frequency higher than 32 MHz, the AP4 for RX might not produce code for operating at the specified frequency, since the code does not correctly switch the operating power control mode or check the MEMWAIT register setting.

After the code has been generated, add processing to the initialization function to switch the operating power control mode and to check that the MEMWAIT register has been set.
Move the code in the **blue box** in [Before modification] to where the **red box** is in [After modification].
Modify the **blue code** in [Before modification] to the **red code** in [After modification]

Refer to Tool News (R20TS0426) when using previous version Smart Configurator.

Function: R_CGC_Create

Example of correction: for RX230/RX231

Before modificaion:

```
void R_CGC_Create(void)
{
    …
    /* Set memory wait cycle setting register */
    SYSTEM.MEMWAIT.BIT.MEMWAIT = 1U;
    memorywaitcycle = SYSTEM.MEMWAIT.BYTE;
    memorywaitcycle++;

    /* Set operating power control */
    SYSTEM.OPCCR.BIT.OPCM = _00_LPC_HIGH_SPEED_MODE;
    while (1U == SYSTEM.OPCCR.BIT.OPCMTSF);

    /* Set clock source */
    SYSTEM.SCKCR3.WORD = _0400_CGC_CLOCKSOURCE_PLL;
    …
}
```

After modificaion:

```
void R_CGC_Create(void)
{
    …
    /* Set operating power control */
    SYSTEM.OPCCR.BIT.OPCM = _00_LPC_HIGH_SPEED_MODE;
    while (1U == SYSTEM.OPCCR.BIT.OPCMTSF);

    /* Set memory wait cycle setting register */
    SYSTEM.MEMWAIT.BIT.MEMWAIT = 1U;
    while(SYSTEM.MEMWAIT.BIT.MEMWAIT != 1U);

    /* Set clock source */
    SYSTEM.SCKCR3.WORD = _0400_CGC_CLOCKSOURCE_PLL;
    …
}
```

Example of correction: for RX23T

Before modificaion:

```
void R_CGC_Create(void)
{
    …
    /* Set memory wait cycle setting register */
    SYSTEM.MEMWAIT.BIT.MEMWAIT = 1U;
    while(SYSTEM.MEMWAIT.BIT.MEMWAIT != 1U);

    /* Set operating power control */
    SYSTEM.OPCCR.BIT.OPCM = _00_LPC_HIGH_SPEED_MODE;
    while (1U == SYSTEM.OPCCR.BIT.OPCMTSF);

    /* Set clock source */
    SYSTEM.SCKCR3.WORD = _0400_CGC_CLOCKSOURCE_PLL;
    …
}
```

After modificaion:

```
void R_CGC_Create(void)
{
    …
    /* Set operating power control */
    SYSTEM.OPCCR.BIT.OPCM = _00_LPC_HIGH_SPEED_MODE;
    while (1U == SYSTEM.OPCCR.BIT.OPCMTSF);

    /* Set memory wait cycle setting register */
    SYSTEM.MEMWAIT.BIT.MEMWAIT = 1U;
    while(SYSTEM.MEMWAIT.BIT.MEMWAIT != 1U);

    /* Set clock source */
    SYSTEM.SCKCR3.WORD = _0400_CGC_CLOCKSOURCE_PLL;
    …
}
```

7.2.10 Dead-time compensation

External pulse width measurement is not available as a general register feature when the dead-time compensation of the multi-function timer pulse unit is to be used.

Add processing for initialization for the measurement of external pulse widths in the user-defined initialization processing for the multi-function timer pulse unit.

Functions: R_MTU2_Create_UserInit, R_MTU3_Create_UserInit

Example of correction: When capture for measurement of the high pulse width of an external input signal is to proceed at crests and troughs in complementary PWM mode

```
void R_MTU3_Create_UserInit(void)
{
    /* Start user code. Do not edit comment generated here */
    MTU5.TIORU.BYTE = 0x1FU;
    MTU5.TIORV.BYTE = 0x1FU;
    MTU5.TIORW.BYTE = 0x1FU;
    /* End user code. Do not edit comment generated here */…
}
```

7.2.11 Realtime clock

When the realtime clock is to be used, the AP4 for RX might not set up correct operation, since there is no processing to wait for the circuit to become stable after setting the clock source.

After code has been generated, add processing to the initialization function to wait for six clock cycles of the clock source for the realtime clock to allow stabilization of the circuit.

Function: R_RTC_Create

Example of correction: When the sub-clock is to be used as the source of the realtime clock and the system clock (ICLK) is running at 16 MHz

```
void R_RTC_Create(void)
{
    uint32_t w_count;
    …
    /* Set sub-clock oscillator */
    while (RTC.RCR3.BIT.RTCEN != 1U)
    {
        RTC.RCR3.BIT.RTCEN = 1U;
    }

    /* Wait for supply 6 clocks of count source */
    for (w_count = 0U; w_count < 267; w_count++)
    {
        nop()
    }
    …
}
```

7.2.12 SPI clock synchronous mode

When an SPI's clock synchronous mode is to be used, the AP4 for RX might not set up communications correctly, since there is no processing to read the SPCR register for checking the completion of the register setting.

Add processing to read the SPCR register in the user-defined initialization function.

Function: R_RSPIx_Create_UserInit

Example of correction: When RSPI0 is to be used

```
void R_RSPI0_Create_UserInit(void)
{
    /* Start user code. Do not edit comment generated here */
    uint8_t w_dummy;

    w_dummy = RSPI0.SPCR.BYTE;
    /* End user code. Do not edit comment generated here */
}
```

7.2.13 SCI/SCIF clock synchronous mode

When the FIFO buffer is to be used in SCI or SCIF clock synchronous mode, unnecessary clock cycles might be output after transmission of data is completed if the bit rate is to be high (3 MHz or above).

Set the FIFO buffer to the maximum number of stages (15) when the bit rate is to be high.

7.2.14 All-module clock-stop function

When the all-module clock-stop function is to be used, the code produced by the AP4 for RX does not allow the initiation of return from the module-stop state even if an interrupt occurs, since the clock supply to the RAM module is also stopped.

After code has been generated, correct the setting value of module stop control register C (MSTPCRC) in the API function to the value after a reset which is stated in the hardware manual.

Function: R_LPC_AllModuleClockStop

Example of correction: RX64M

```
MD_STATUS R_LPC_AllModuleClockStop(void)
{
    …
    /* Set module stop for RAM and CAC. */
    SYSTEM.MSTPCRC.LONG = 0xFFFF0000U;
    …
}
```

7.2.15 Using the Voltage Detection Circuits

When using the voltage detection circuits (LVDAa and LVDAb), “wait time” for the voltage monitoring 1 interrupt and the voltage monitoring 2 interrupt after code is not generated.

Refer to Tool News (R20TS0314) for the details.

Function: R_LPC_AllModuleClockStop

7.2.16 When the LCD Controller/Driver and I/O Ports, PB3 and PB5 are Set

Conflict checking is wrong when the LCD controller/driver and I/O Ports, PB3 and PB5 are set the same time. When the LCD controller/driver is used and SEG13, which is the shared pin of I/O port PB5, is configured, I/O port PB3, which avoid pin conflict, cannot be configured.

Refer to Tool News (R20TS0245) for the details.

Revision History

Rev	Date	Description	
1.00	Apr. 22, 2019	-	New release
2.00	Jun. 13, 2019	The whole document	Restructured.
		5	Device number corrected.
		8	Changes corrected.
		10	History of correction announced corrected.
		11 to 16	Points for caution corrected and added.
2.01	June 28, 2019	1	Contents corrected.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.4.0-1 November 2017)

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