

## RZ/T2H Group

### Encoder I/F BiSS-C sample program

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#### Summary

This document describes the RZ/T2H Encoder I/F BiSS sample program package.

For BiSS Interface communication protocol specifications and encoder specifications, contact manufacturer of each encoder to obtain it.

#### Functionality Checked Device

RZ/T2H Evaluation Board (RTK9RZT2Hxxxxxxxx)

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## 1. Package Contents

This package contains the following contents.

The BiSS-C encoder interface of the RZ/T2H supports up to 16 axes, but the sample program uses only 1 axis of them. If you use with 2 axes or more simultaneously, modify the sample program to support required axes.

### 1.1 Software

- Source code

No.	Name	Version
1	RZ/T2H BiSS-C sample program (CR52 ver. *)	2.0
2	RZ/T2H BiSS-C sample program (CA55 ver. *)	2.0

Note: This sample program has a CR52 version that runs on the CPU core Cortex-R52 and a CA55 version that runs on the CPU core Cortex-A55. CR52 ver. and CA55 ver. are descriptions of the respective version.

### 1.2 Document

No.	Document name	Version	File name
1	RZ/T2H Group Encoder I/F BiSS-C sample program Release Note	2.01	(j) r11an0790jj0201-rzt2h.pdf (e) r11an0790ej0201-rzt2h.pdf (this document)
2	RZ/T2H Group BiSS-C sample program Application Note	2.00	(j) r11an0789jj0200-rzt2h-biss.pdf (e) r11an0789ej0200-rzt2h-biss.pdf

## 2. File Structure

The file structure and contents of this package are detailed below.

Top

```

├── r11an0790jj0201-rzt2h.pdf
├── r11an0790ej0201-rzt2h.pdf
├── workspace
│   ├── Software
│   │   ├── iccarm
│   │   │   ├── RZ_T2H_biss.zip           : RZ/T2H BiSS sample program set
│   │   │   │                               CR52 ver. (IAR)
│   │   │   └── RZ_T2H_CA55_biss.zip
│   │   │       ├── RZ_T2H_CA55_0_biss    : RZ/T2H BiSS sample program set
│   │   │       │                               CA55 ver. (IAR)
│   │   │       └── RZ_T2H_CR52_0_primary : CPU_CTRL register setting program (IAR)
│   │   └── gcc
│   │       ├── RZ_T2H_biss.zip           : RZ/T2H BiSS sample program set
│   │       │                               CR52 ver. (e2 studio)
│   │       └── RZ_T2H_CA55_biss.zip
│   │           ├── RZ_T2H_CA55_0_biss    : RZ/T2H BiSS sample program set
│   │           │                               CA55 ver. (e2 studio)
│   │           └── RZ_T2H_CR52_0_primary : CPU_CTRL register setting program (e2 studio)
│   └── Documents
│       ├── r11an0789jj0200-rzt2h-biss.pdf
│       └── r11an0789ej0200-rzt2h-biss.pdf

```

The file structure of the RZ\_T2H\_CR52\_biss.zip and RZ\_T2H\_CA55\_0\_biss folder are shown below.

Top folder

```

├── configuration.xml           : FSP Configuration data
├── ( Build Tool Dependency Environment File )
├── src
│   ├── hal_entry.c           : BiSS-C sample program
│   ├── biss_main.c           : BiSS-C sample program
│   ├── siochar.c             : SCI_UART sample program
│   ├── siorw.c               : SCI_UART sample program
│   ├── sio_char.h            : SCI_UART sample program
│   └── drv
│       ├── biss
│       │   ├── iodefne_biss.h : BiSS register definition file
│       │   ├── r_biss_rzt2.c   : BiSS driver file
│       │   ├── r_biss_rzt2_config.h : BiSS driver file
│       │   ├── r_biss_rzt2_dat.h : BiSS driver file
│       │   ├── r_biss_rzt2_if.h : BiSS driver file
│       │   ├── r_biss_rzt2_private.h : BiSS driver file
│       │   └── bissc
│       │       ├── r_bissc_rzt2.c : BiSS-C driver file
│       │       ├── r_bissc_rzt2_config.h : BiSS-C driver file
│       │       ├── r_bissc_rzt2_if.h : BiSS-C driver file
│       │       └── r_bissc_rzt2_private.h : BiSS-C driver file

```

The file structure of the RZ\_T2H\_CR52\_0\_primary folder is shown below.

Top folder

```
|— configuration.xml           : FSP Configuration data
|— ( Environment File Depending on Build Tool )
|— src
   |— hal_entry.c             : CA55 start-up program
```

### 3. About BiSS Sample Program

This section contains information necessary to use the complete set of BiSS sample program.

#### 3.1 Software Information

##### 3.1.1 Base OS

This sample program is OS-independent.

##### 3.1.2 Memory Size

Memory size used by this sample program and BiSS, BiSS-C driver is shown in following table. This table does not include the memory size used by Flexible Software Package or C language libraries of the compiler.

###### (1) CR52 ver.

Items		Memory Size	
		EWARM [kBytes]	e <sup>2</sup> studio [kBytes]
BiSS, BiSS-C driver	Code	3.7	3.5
	Data (with initial value)	0.0	0.0
	Data (without initial value)	0.9	0.9
	Constant Data	0.3	0.3
Sample program	Code	3.1	3.4
	Data (with initial value)	0.0	0.0
	Data (without initial value)	0.6	0.6
	Constant Data	1.5	1.6

###### (2) CA55 ver.

Items		Memory Size	
		EWARM [kBytes]	e <sup>2</sup> studio [kBytes]
BiSS, BiSS-C driver	Code	5.8	4.9
	Data (with initial value)	0.0	0.0
	Data (without initial value)	1.1	1.1
	Constant Data	0.4	0.5
Sample program	Code	4.9	6.1
	Data (with initial value)	0.0	0.0
	Data (without initial value)	0.7	0.7
	Constant Data	1.7	1.7

## 3.2 Hardware Information

### 3.2.1 Device

RZ/T2H

### 3.2.2 Target Board

#### (1) Board Name

RZ/T2H Evaluation Board (RTK9RZT2Hxxxxxxxx)

#### (2) Setting of the Target Board

SW1-4: ON

SW1-6: OFF

SW2-1: ON, SW2-2: OFF

SW2-7: OFF

SW2-8: OFF

SW14-1: ON, SW14-2: OFF, SW14-3: ON, SW14-6: OFF (Set to xSPI1 boot mode)

CN39: Short between 2-3pin (Set VDD1833\_2 to 3.3V)

CN40: Short between 2-3pin (Set VDD1833\_3 to 3.3V)

CN78: Short between 1-2 pins, Open between 3-4 pins, and between 5-6 pins (Set VDD1833\_6 to 3.3V)

Note: To use target board RTK9RZT2H0CW1000BJ with connecting RS-485 board, power on/off by plugging and unplugging to the power-supply connector CN47 with keeping the slide switch SW16 on.

## (3) Used pin for Target Board

The correspondence between the pin used as the encoder I/F and the pin header of the target board is as follows.

Channel	Port Name	Pin Header	Input/Output	Voltage Domain	Description
BiSS0	ENCIFDI0 (SL0)	CN2 #9	Input	VDD33	Sensor / Control data
	ENCIFCK0 (MA0)	CN2 #3	Output	VDD33	Clock / Control data
BiSS1	ENCIFDI1 (SL1)	CN2 #8	Input	VDD1833_3	Sensor / Control data
	ENCIFCK1 (MA1)	CN2 #2	Output	VDD1833_3	Clock / Control data
BiSS2	ENCIFDI2 (SL2)	CN2 #17	Input	VDD33	Sensor / Control data
	ENCIFCK2 (MA2)	CN2 #11	Output	VDD33	Clock / Control data
BiSS3	ENCIFDI3 (SL3)	CN2 #18	Input	VDD33	Sensor / Control data
	ENCIFCK3 (MA3)	CN2 #12	Output	VDD33	Clock / Control data
BiSS4	ENCIFDI4 (SL4)	CN2 #27	Input	VDD1833_5	Sensor / Control data
	ENCIFCK4 (MA4)	CN2 #21	Output	VDD33	Clock / Control data
BiSS5	ENCIFDI5 (SL5)	CN2 #26	Input	VDD1833_6	Sensor / Control data
	ENCIFCK5 (MA5)	CN2 #20	Output	VDD1833_6	Clock / Control data
BiSS6	ENCIFDI6 (SL6)	CN3 #9	Input	VDD1833_3	Sensor / Control data
	ENCIFCK6 (MA6)	CN3 #3	Output	VDD1833_3	Clock / Control data
BiSS7	ENCIFDI7 (SL7)	CN3 #8	Input	VDD1833_3	Sensor / Control data
	ENCIFCK7 (MA7)	CN3 #2	Output	VDD1833_3	Clock / Control data
BiSS8	ENCIFDI8 (SL8)	CN3 #17	Input	VDD33	Sensor / Control data
	ENCIFCK8 (MA8)	CN3 #11	Output	VDD33	Clock / Control data
BiSS9	ENCIFDI9 (SL9)	CN3 #18	Input	VDD1833_2	Sensor / Control data
	ENCIFCK9 (MA9)	CN3 #12	Output	VDD1833_2	Clock / Control data
BiSS10	ENCIFDI10 (SL10)	CN3 #27	Input	VDD1833_2	Sensor / Control data
	ENCIFCK10 (MA10)	CN3 #21	Output	VDD1833_2	Clock / Control data
BiSS11	ENCIFDI11 (SL11)	CN3 #26	Input	VDD1833_2	Sensor / Control data
	ENCIFCK11 (MA11)	CN3 #20	Output	VDD1833_2	Clock / Control data
BiSS12	ENCIFDI12 (SL12)	CN10 #9	Input	VDD1833_6	Sensor / Control data
	ENCIFCK12 (MA12)	CN10 #3	Output	VDD1833_6	Clock / Control data
BiSS13	ENCIFDI13 (SL13)	CN10 #8	Input	VDD1833_6	Sensor / Control data
	ENCIFCK13 (MA13)	CN10 #2	Output	VDD1833_6	Clock / Control data
BiSS14	ENCIFDI14 (SL14)	CN10 #17	Input	VDD33	Sensor / Control data
	ENCIFCK14 (MA14)	CN10 #11	Output	VDD33	Clock / Control data
BiSS15	ENCIFDI15 (SL15)	CN10 #18	Input	VDD33	Sensor / Control data
	ENCIFCK15 (MA15)	CN10 #12	Output	VDD33	Clock / Control data

### 3.3 Procedures on Development Environments: CR52 ver.

#### 3.3.1 Preparation before Executing the Sample Program

This sample program communicates with a PC. The USB connection terminal on the target board is CN34. Select higher-numbered port from COM ports that appear at connecting the board with the host PC.

The terminal software of the host PC is set as shown in the following table.

Function	Setting
Communication method	Asynchronous serial transmission/reception
Sending / receiving order	LSB first
Transfer rate	19200 bps
Character length	8 bits
Stop bit length	1 bit
Parity function	None
Hardware flow control	None

#### 3.3.2 EWARM: IAR Systems

##### (1) Build Environment

IAR Embedded Workbench for ARM (EWARM)

Version 9.60.2 + patch (EWARM\_Patch\_for\_RZT2H\_N2H\_rev1.0)

RENESAS FSP Smart Configurator (FSP SC) 2024-10

RENESAS Flexible Software Package (FSP) for RZ/T2 v2.2.0

##### (2) Execution Environment ICE

IAR I-jet

##### (3) Build Procedure for Sample Programs

The build procedure for the sample program is as follows.

- 1 Extract RZ\_T2H\_CR52\_biss.zip and copy the extracted source files to the desired location.
- 2 Activate EWARM.
- 3 Select [File] menu -> [Open Workspace].
- 4 Open the extracted source file RZ\_T2H\_biss.eww.
- 5 Start the FSP Smart Configurator from the [Tools] menu of the EWARM IDE. \*

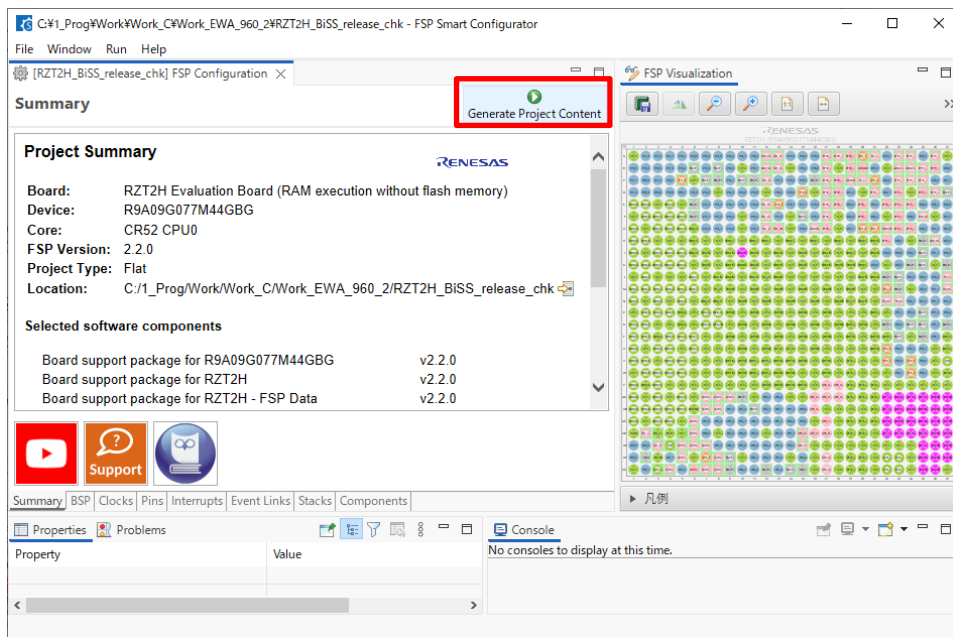
Note: The following procedure adds the activation of the FSP Smart Configurator to the [Tools] menu of the EWARM IDE. Select [Tools] menu -> [Tool Configuration] in the EWARM IDE. Select the [New] button, specify a table string in each field, and press [OK].

Field	String
Menu text	FSP Smart Configurator
Command	\$RASC_EXE_PATH\$
Argument	--compiler IAR configuration.xml
Initial directory	\$PROJ_DIR\$

String for the command is variable holding the path of the Smart Configurator execution file, rasc.exe. You can also start the FSP Smart Configurator directly from the command prompt by specifying the folder where it is installed.



- 6 In the FSP Configuration pane of the Smart Configurator, click Generate Project Content. The rzt, rzt\_cfg, rzt\_gen, script and .setting folders will be generated.



- 7 When project generation is complete, close the Smart Configurator.  
 8 Select [Rebuild ALL] from the [Project] menu of EWARM.  
 The file Debug\Exe\RZ\_T2H\_biss.out is generated.

#### (4) Sample Program Execution Procedure

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

- 1 Select [Project] menu -> [Download and Debug].
- 2 Select [Debug] menu -> [Execute].

#### (5) Execution Result of the Sample Program

Run the sample program and enter commands in the terminal software window. For commands, see 4.11.7 console commands in the RZ/T2H Group BiSS-C Sample Program Application Note.

```

COM18 - Tera Term VT
File Edit Setup Control Window Help
BiSS sample program start
biss>pos
get position
result
multi turn data: 2807
single turn data: 139396
alarm err: 0
warning err: 0
biss>
  
```

### 3.3.3 e<sup>2</sup> studio: RENESAS

#### (1) Build Environment

RENESAS e<sup>2</sup> studio 2024-10

Toolchain version: GNU ARM Embedded 12.2.1.arm-12-24

RENESAS Flexible Software Package (FSP) for RZ/T2 v2.2.0

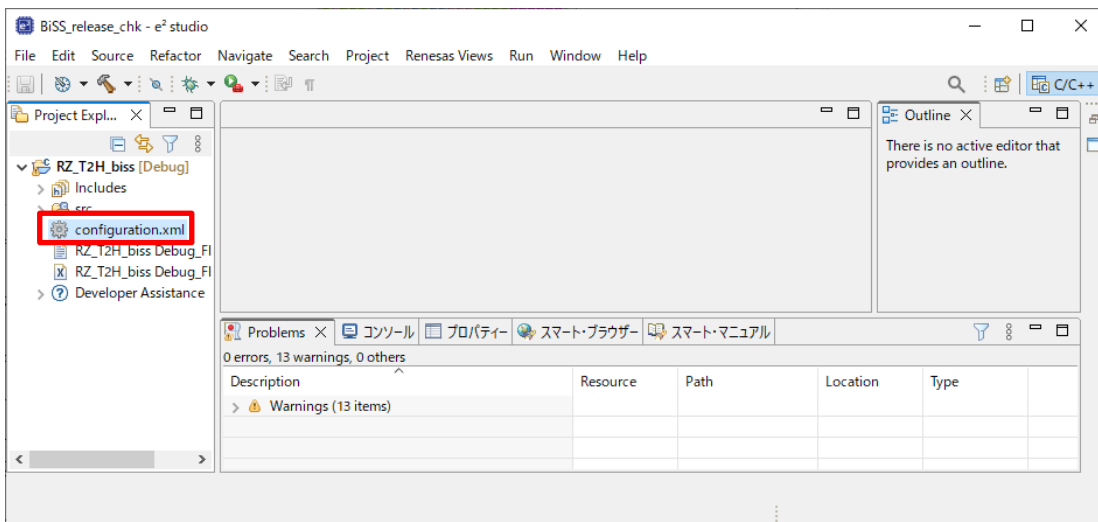
#### (2) Execution Environment ICE

SEGGER J-Link v7.98c

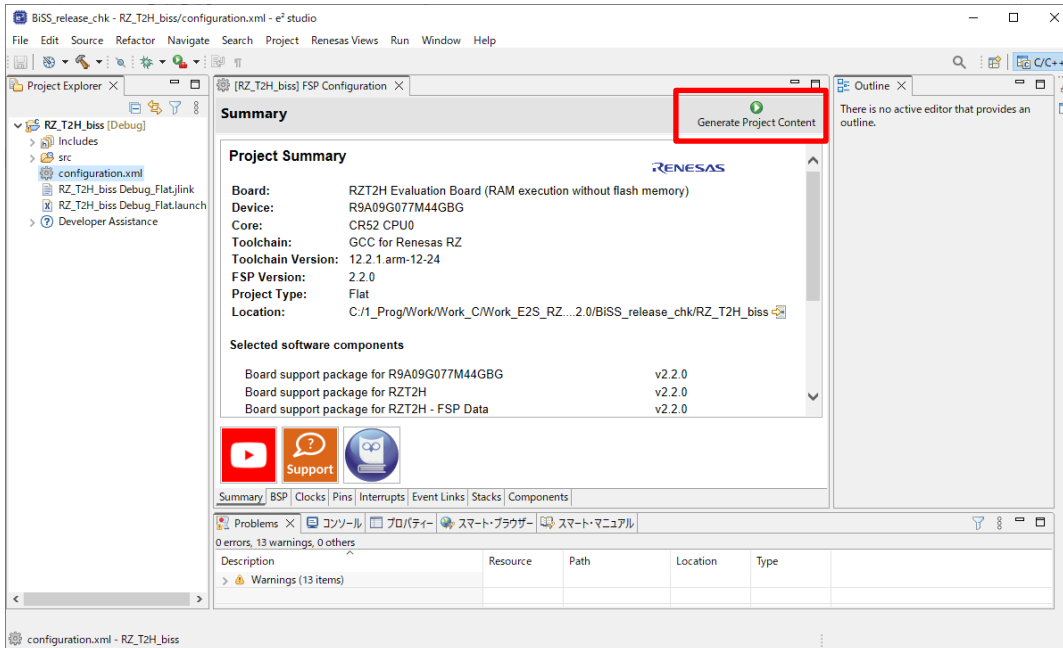
#### (3) Build Procedure of the Sample Program

The procedure for building the sample program is as follows.

- 1 Extract RZ\_T2H\_CR52\_biss.zip and copy the expanded source file to any location.
- 2 After launching e<sup>2</sup> studio and moving to the workspace, click the [File] menu -> [Import] and select Existing project to workspace and click [Next].
- 3 On the project import screen, select the folder where the sample program was expanded as the root directory.
- 4 Select a project, check Copy Project to Workspace, and click [Finish].
- 5 Double-click the configuration.xml in the Project Explorer pane of e<sup>2</sup> studio to open it.



- 6 Click Generate Project Content in the FSP Configuration pane of e<sup>2</sup> studio.  
The rzt, rzt\_cfg, rzt\_gen, script and .settings folders are generated.



- 7 Select [Project] menu -> [Build All]  
The Debug¥RZ\_T2H\_biss.elf file is generated.

#### (4) Execution Procedure of the Sample Program

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

- 1 Select [Run] menu -> [Debug As] -> [Renesas GDB Hardware Debugging].
- 2 Click [Debug] to start downloading to internal RAM.
- 3 Click [Run] menu -> [Resume] to run the sample program

#### (5) Execution Result of the Sample Program

Run the sample program and enter commands in the terminal software window. For commands, see 4.11.7 console commands in the RZ/T2H Group BiSS-C Sample Program Application Note.

```

COM18 - Tera Term VT
File Edit Setup Control Window Help
BiSS sample program start
biSS>pos
get position
result
multi turn data: 2807
single turn data: 139396
alarm err: 0
warning err: 0
biSS>

```

### 3.4 Procedures on Development Environments: CA55 ver.

#### 3.4.1 Preparation before Executing the Sample Program

This sample program communicates with a PC. The USB connection terminal on the target board is CN34. Select lower-numbered port from COM ports that appear at connecting the board with the host PC.

The terminal software of the host PC is set as shown in the following table.

Function	Setting
Communication method	Asynchronous serial transmission/reception
Sending / receiving order	LSB first
Transfer rate	19200 bps
Character length	8 bits
Stop bit length	1 bit
Parity function	None
Hardware flow control	None

#### 3.4.2 EWARM: IAR Systems

##### (1) Build Environment

IAR Embedded Workbench for ARM (EWARM)

Version 9.60.2 + patch (EWARM\_Patch\_for\_RZT2H\_N2H\_rev1.0)

RENESAS FSP Smart Configurator (FSP SC) 2024-10

RENESAS Flexible Software Package (FSP) for RZ/T2 v2.2.0

##### (2) Execution Environment ICE

IAR I-jet

##### (3) Build Procedure for Sample Programs

The build procedure for the sample program is as follows.

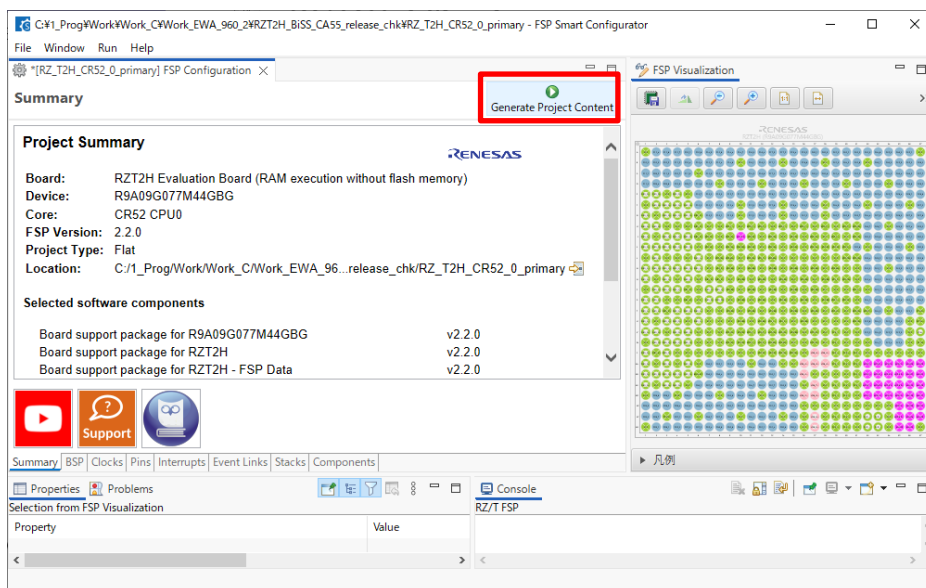
- 1 Extract RZ\_T2H\_CA55\_biss.zip and copy the extracted source files to the desired location.
- 2 Activate EWARM.
- 3 Select [File] menu -> [Open Workspace].
- 4 Open the extracted source file RZ\_T2H\_CR52\_0\_primary -> RZ\_T2H\_CR52\_0\_primary.eww.
- 5 Start the FSP Smart Configurator from the [Tools] menu of the EWARM IDE. \*

Note: The following procedure adds the activation of the FSP Smart Configurator to the [Tools] menu of the EWARM IDE. Select [Tools] menu -> [Tool Configuration] in the EWARM IDE. Select the [New] button, specify a table string in each field, and press [OK].

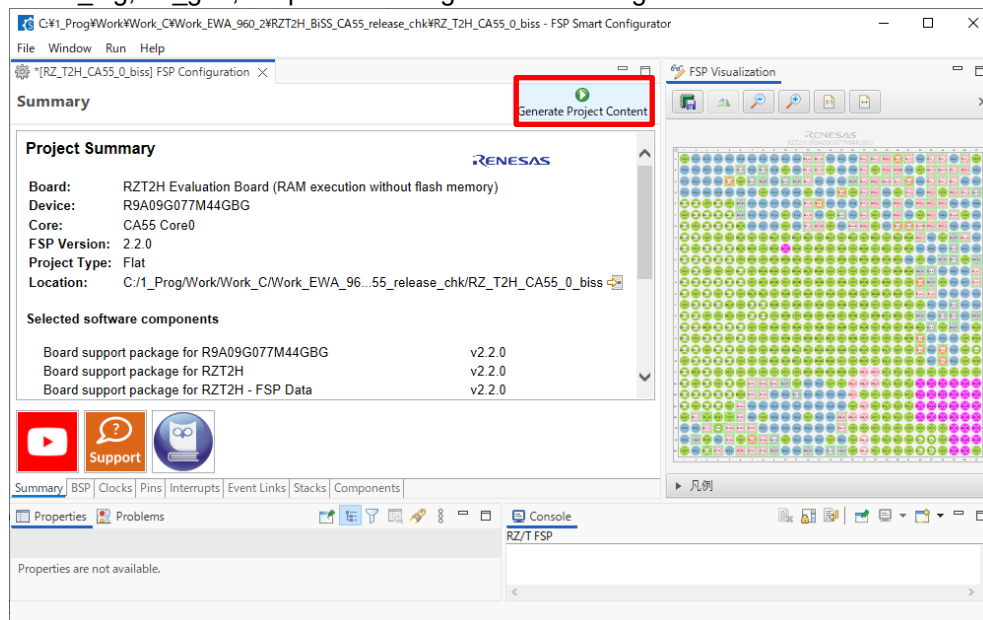
Field	String
Menu text	FSP Smart Configurator
Command	\$RASC_EXE_PATH\$
Argument	--compiler IAR configuration.xml
Initial directory	\$PROJ_DIR\$

String for the command is variable holding the path of the Smart Configurator execution file, rasc.exe. You can also start the FSP Smart Configurator directly from the command prompt by specifying the folder where it is installed.

- 6 In the FSP Configuration pane of the Smart Configurator, click Generate Project Content. The rzt, rzt\_cfg, rzt\_gen, script and .setting folders will be generated.



- 7 When project generation is complete, close the Smart Configurator.  
 8 Select [Rebuild ALL] from the [Project] menu of EWARM.  
 The file Debug\Exe\RZ\_T2H\_CR52\_0\_primary.sbd is generated.  
 9 Select [File] menu -> [Open Workspace].  
 10 Open the extracted source file RZ\_T2H\_CA55\_0\_biss -> RZ\_T2H\_CA55\_0\_primary.eww.  
 (RZ\_T2H\_CR52\_0\_primary.sbd of the primary project is referenced to open this workspace file.  
 Please build the primary project in advance.)  
 11 Start the FSP Smart Configurator from the [Tools] menu of the EWARM IDE.  
 12 In the FSP Configuration pane of the Smart Configurator, click Generate Project Content. The rzt, rzt\_cfg, rzt\_gen, script and .setting folders will be generated.



- 13 When project generation is complete, close the Smart Configurator.  
 14 Select [Rebuild ALL] from the [Project] menu of EWARM.  
 The file Debug\Exe\RZ\_T2H\_CA55\_0\_biss.out is generated.

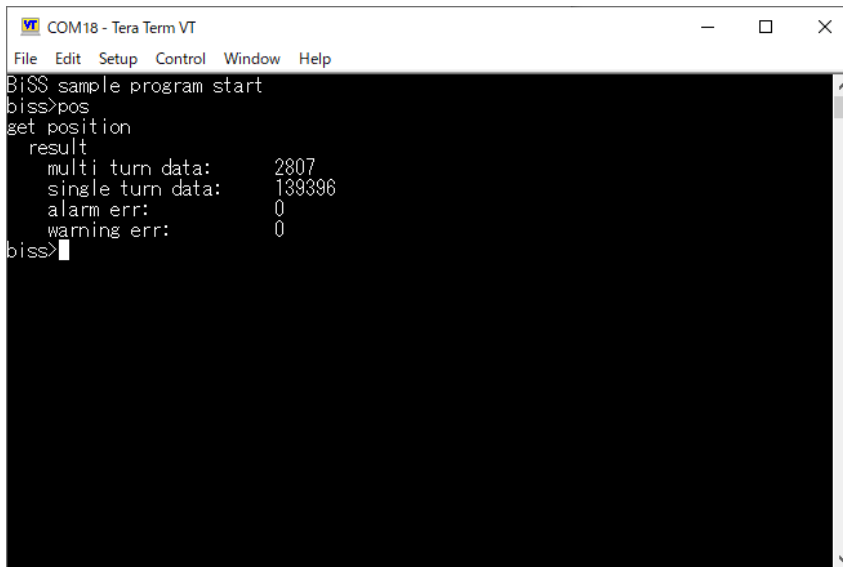
#### (4) Sample Program Execution Procedure

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

- 1 In the workspace of RZ\_T2H\_CR52\_0\_primary, select [Project] menu -> [Download and Debug]. RZ\_T2H\_CA55\_0\_biss project is launched.
- 2 In the workspace of RZ\_T2H\_CR52\_0\_primary, select [Debug] menu -> [Execute]. CA55 start-up program is executed.
- 3 In the workspace of RZ\_T2H\_CA55\_0\_biss, select [Debug] menu -> [Execute]. Sample program is executed.

#### (5) Execution Result of the Sample Program

Run the sample program and enter commands in the terminal software window. For commands, see 4.11.7 console commands in the RZ/T2H Group BiSS-C Sample Program Application Note.



```
COM18 - Tera Term VT
File Edit Setup Control Window Help
BiSS sample program start
biss>pos
get position
result
multi turn data: 2807
single turn data: 139396
alarm err: 0
warning err: 0
biss>
```

### 3.4.3 e<sup>2</sup> studio: RENESAS

#### (1) Build Environment

RENESAS e<sup>2</sup> studio 2024-10

Toolchain version:

GNU ARM Embedded 12.2.1.arm-12-24 (Used by RZ\_T2H\_CR52\_0\_primary.)

GCC ARM A-Profile (Aarch64 bare-metal) 10.3.1.20210621 (Used by RZ\_T2H\_CA55\_0\_biss.)

RENESAS Flexible Software Package (FSP) for RZ/T2 v2.2.0

#### (2) Execution Environment ICE

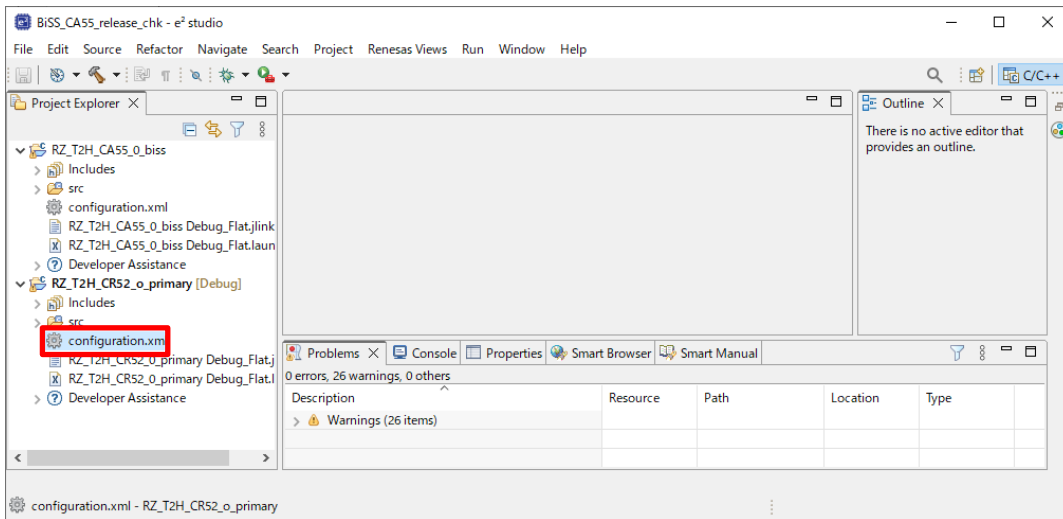
SEGGER J-Link v7.98c

#### (3) Build Procedure of the Sample Program

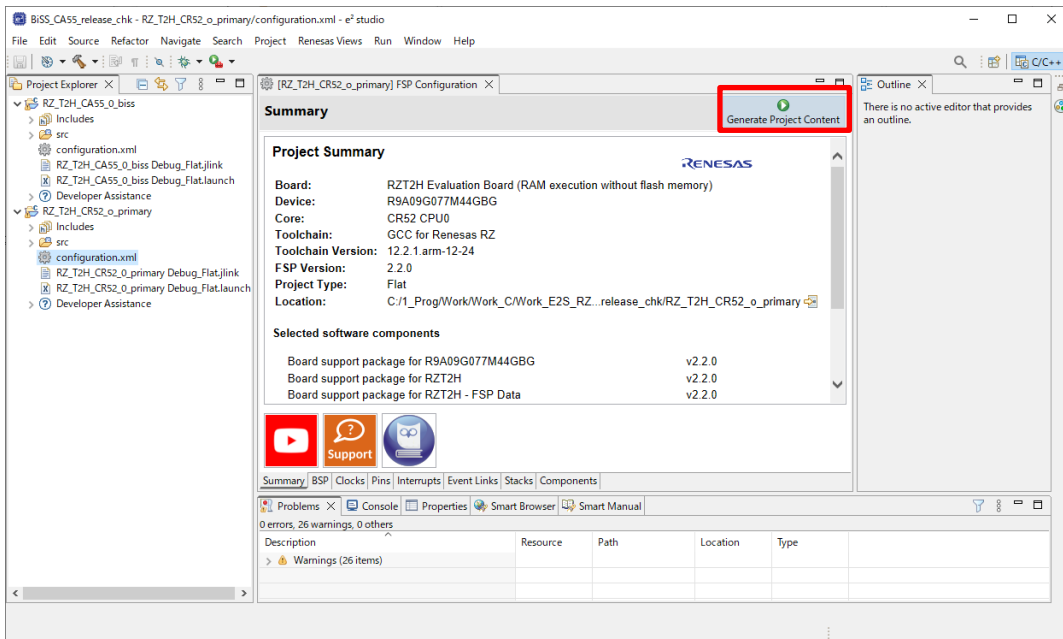
The procedure for building the sample program is as follows.

- 1 Extract RZ\_T2H\_CA55\_biss.zip and copy the expanded source file to any location.
- 2 After launching e<sup>2</sup> studio and moving to the workspace, click the [File] menu -> [Import] and select Existing project to workspace and click [Next].

- 3 On the project import screen, select the folder where the sample program was expanded as the root directory.
- 4 Select a project, check Copy Project to Workspace, and click [Finish].
- 5 Double-click the configuration.xml of the RZ\_T2H\_CR52\_0\_primary project in the Project Explorer pane of e<sup>2</sup> studio to open it.

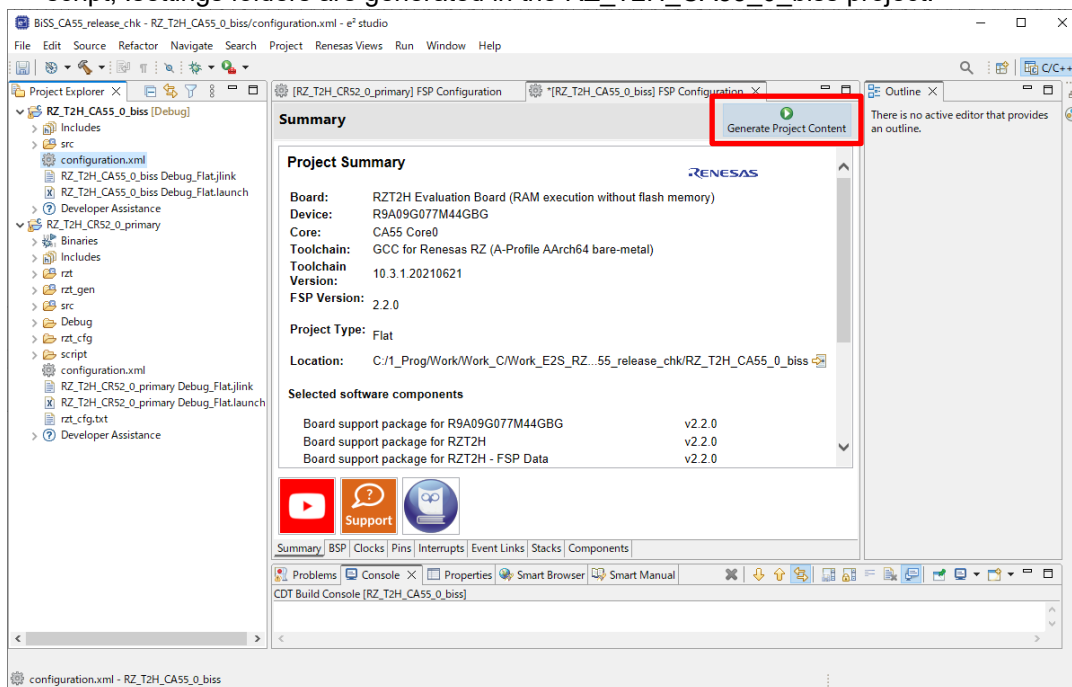


- 6 Click Generate Project Content in the FSP Configuration pane of e<sup>2</sup> studio. The rzt, rzt\_cfg, rzt\_gen, script and .settings folders are generated in the RZ\_T2H\_CR52\_0\_primary project.



- 7 Select RZ\_T2H\_CR52\_primary project in the Project Explorer pane and execute [Run] menu -> [Build Project].  
The file Debug\RZ\_T2H\_CR52\_0\_primary.sbd is generated.
- 8 Double-click the configuration.xml of the RZ\_T2H\_CA55\_0\_biss project in the Project Explorer pane of e<sup>2</sup> studio to open it. (RZ\_T2H\_CR52\_0\_primary.sbd of the primary project is referenced to open this configuration file. Please build the primary project in advance.)

9 Click Generate Project Content in the FSP Configuration pane of e<sup>2</sup> studio. The rzt, rzt\_cfg, rzt\_gen, script, .settings folders are generated in the RZ\_T2H\_CA55\_0\_biss project.

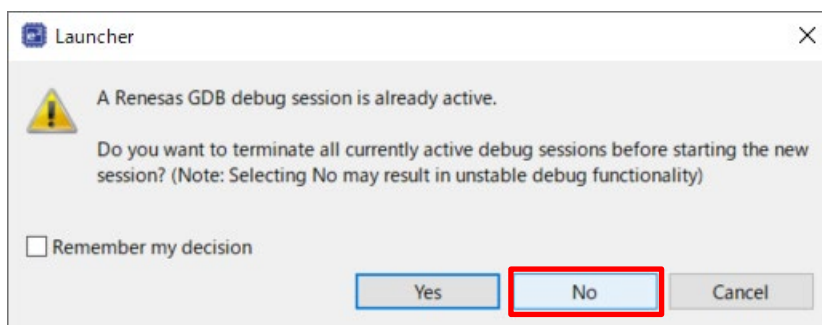


10 Select [Project] menu -> [Build All]  
Files Debug\RZ\_T2H\_CA55\_0\_biss.elf is generated.

(4) Execution Procedure of the Sample Program

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

- 1 Select [Run] menu -> [Debug As] -> [Renesas GDB Hardware Debugging] for the RZ\_T2H\_CR52\_0\_primary project.  
Click [Debug] to start downloading to internal RAM.
- 2 Click [Run] menu -> [Resume] to run the CA55 start-up program.
- 3 Select [Run] menu -> [Debug As] -> [Renesas GDB Hardware Debugging] for the RZ\_T2H\_CA55\_0\_biss project.
- 4 Select 'No' when the dialog box inquiring about termination of the active debug session is displayed.

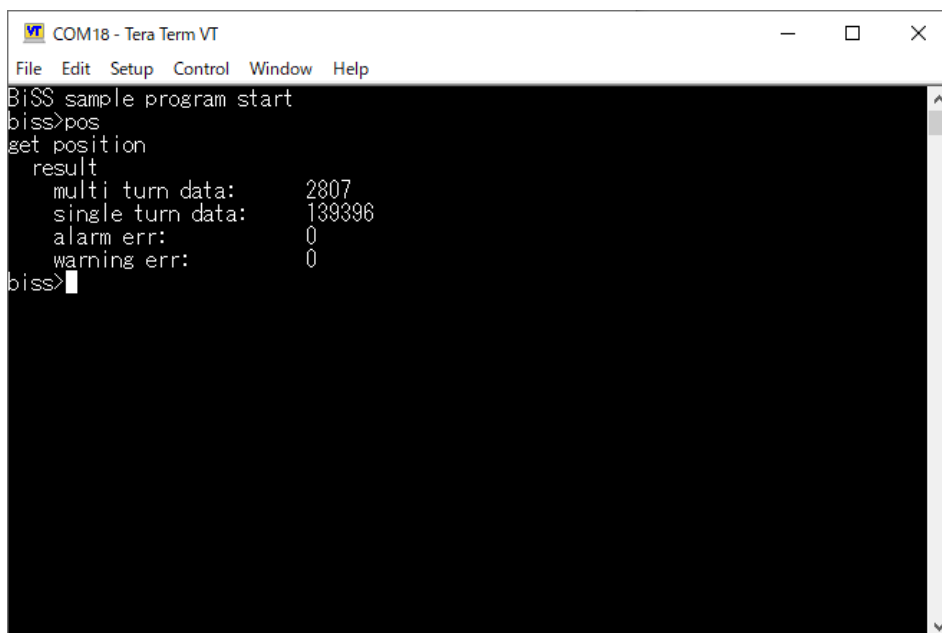


- 5 If 'Proceed with launch' is displayed, select 'Yes'.
- 6 Click [Debug] to start downloading to internal RAM.
- 7 Click [Run] menu -> [Resume] to run the sample program.



## (5) Execution Result of the Sample Program

Run the sample program and enter commands in the terminal software window. For commands, see 4.11.7 console commands in the RZ/T2H Group BiSS-C Sample Program Application Note.



```
COM18 - Tera Term VT
File Edit Setup Control Window Help
BiSS sample program start
biss>pos
get position
result
multi turn data: 2807
single turn data: 139396
alarm err: 0
warning err: 0
biss>
```

## Revision History

Rev.	Date	Description	
		Page	Summary
0.50	Sep 29.23		First Edition issued.
0.60	Apr 19.24	1 - 4	Update the application note and release note version number.
			Update sample program version to 0.6 (Support FSP v1.3.0)
		5	Update file structure. Add structure of CA55 version.
			Update memory size information. Add information of CA55 ver.
		1, 6	Update description of the board name.
		8 - 11	Update build environment and figures for CR52 ver.
		12 - 16	Add development procedures for CA55 ver.
2.00	Nov 21.24	2 - 4	Update revisions of the application note and the release note.
			Update sample program version to 2.0. (Supported FSP v2.2.0.)
		5	Update the file structure.
			Update memory size information.
		6	Add xSPI1 boot mode in setting of the target board.
		8 - 17	Update build environment for FSP v2.2.0. Figures are replaced.
2.01	Dec 13.24	2, 3	Update revision of the release note. Correct path name of the FSP SC in the sample program environment files to use default installation path.

## General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

### 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

### 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

### 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

### 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

### 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

### 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

### 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

### 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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