

## RZ/T2H Group

### Encoder I/F A-format sample program

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#### Summary

This document describes the RZ/T2H Encoder I/F A-format® sample program package.

For A-format® Ver.2.0 communication protocol specifications and encoder specifications (RES-61QAP06), contact Nikon Corporation.

#### Functionality Checked Device

RZ/T2H Evaluation Board (RTK9RZT2Hxxxxxxxx)

#### Contents

1. Package Contents .....	2
1.1 Software .....	2
1.2 Documents .....	2
2. File Structure .....	3
3. About A-format Sample Program .....	5
3.1 Software Information .....	5
3.1.1 Base OS .....	5
3.1.2 Memory Size.....	5
3.2 Hardware Information .....	6
3.2.1 Device.....	6
3.2.2 Target Board.....	6
3.3 Procedures on Development Environments: CR52 ver. ....	8
3.3.1 Preparation before Executing the Sample Program.....	8
3.3.2 EWARM from IAR Systems.....	8
3.3.3 e <sup>2</sup> studio from RENESAS .....	10
3.4 Procedures on Development Environments: CA55 ver.....	12
3.4.1 Preparation before Executing the Sample Program.....	12
3.4.2 EWARM from IAR Systems.....	12
3.4.3 e <sup>2</sup> studio from RENESAS .....	14
Revision History .....	18

A-format is a registered trademark of Nikon Corporation.

## 1. Package Contents

This package contains the following contents.

The RZ/T2H encoder interface supports up to 16 axes, but the sample program uses only 1 axis of them. If you use with 2 axes or more simultaneously, modify the sample program to support required axes.

This sample program operation was checked with one-to-one connection A-format Ver.2.0 encoder.

Operation with bus connection encoder is not checked. Operation with A-format Ver.1.0 encoder is not supported.

### 1.1 Software

- Source code

No.	Name	Version number
1	RZ/T2H A-format sample program (CR52 ver.*)	2.0
2	RZ/T2H A-format sample program (CA55 ver.*)	2.0

Note This sample program has a CR52 version that runs on the CPU core Cortex-R52 and a CA55 version that runs on the CPU core Cortex-A55. CR52 ver. and CA55 ver. are descriptions of the respective version.

### 1.2 Documents

No.	Document name	Version	File name
1	RZ/T2H Group Encoder I/F A-format sample program Release Note	2.01	(j) r11an0779jj0201-rzt2h.pdf (e) r11an0779ej0201-rzt2h.pdf (this document)
2	RZ/T2H Group A-format sample program Application Note	2.00	(j) r11an0778jj0200-rzt2h-a-format.pdf (e) r11an0778ej0200-rzt2h-a-format.pdf

## 2. File Structure

The file structure and contents of this package are detailed below.

Top

```
|— r11an0779jj0201-rzt2h.pdf
|— r11an0779ej0201-rzt2h.pdf
└─ workspace
    └─ Software
        └─ iccarm
            └─ RZ_T2H_CR52_a_as.zip : RZ/T2H A-format sample program set
                                   CR52 ver. (IAR)
            └─ RZ_T2H_CA55_a_as.zip
                └─ RZ_T2H_CA55_0_a_as : RZ/T2H A-format sample program set
                                           CA55 ver. (IAR)
                └─ RZ_T2H_CR52_0_primary : CPU CTRL register setting program (IAR)
        └─ gcc
            └─ RZ_T2H_CR52_a_as.zip : RZ/T2H A-format sample program set
                                   CR52 ver. (e2 studio)
            └─ RZ_T2H_CA55_a_as.zip
                └─ RZ_T2H_CA55_0_a_as : RZ/T2H A-format sample program set
                                           CA55 ver. (e2 studio)
                └─ RZ_T2H_CR52_0_primary : CPU_CTRL register setting program (e2 studio)
    └─ Documents
        └─ r11an0778jj0200-rzt2h-a-format.pdf
        └─ r11an0778ej0200-rzt2h-a-format.pdf
```

The file structure of the RZ\_T2H\_CR52\_a\_as.zip and RZ\_T2H\_CA55\_0\_a\_as folder is shown below.

Top folder

```

├── configuration.xml           : FSP Configuration data
├── ( Build Tool Dependent Environment File )
├── src
│   ├── hal_entry.c           : A-format sample program
│   ├── a_as_main.c           : A-format sample program
│   ├── siochar.c             : SCI_UART sample program
│   ├── siorw.c               : SCI_UART sample program
│   ├── sio_char.h            : SCI_UART sample program
│   └── drv
│       └── a_as
│           ├── iodefine_a_as.h : A_AS register definition file
│           ├── r_a_as_rzt2.c    : A_AS driver file
│           ├── r_a_as_rzt2_config.h : A_AS driver file
│           ├── r_a_as_rzt2_dat.h : A_AS driver file
│           ├── r_a_as_rzt2_if.h : A_AS driver file
│           ├── r_a_as_rzt2_private.h : A_AS driver file
│           └── a_format
│               ├── r_a_format_rzt2.c : A-format driver file
│               ├── r_a_format_rzt2_config.h : A-format driver file
│               └── r_a_format_rzt2_private.h : A-format driver file

```

The file structure of the RZ\_T2H\_CR52\_0\_primary is shown below.

Top folder

```

├── configuration.xml           : FSP Configuration data
├── ( Build Tool Dependent Environment File )
├── src
│   └── hal_entry.c           : CA55 start-up program

```

### 3. About A-format Sample Program

This section contains information necessary to use the complete set of A-format sample program.

#### 3.1 Software Information

##### 3.1.1 Base OS

This sample program is OS-independent.

##### 3.1.2 Memory Size

Memory size used by this sample program and A-format driver is shown in following table. This table does not include memory size used by Flexible Software Package or C language libraries of the compiler.

###### (1) CR52 ver.

Items		Memory Size	
		EWARM [kBytes]	e <sup>2</sup> studio [kBytes]
A-format driver	Code	4.2	3.5
	Data (with initial value)	0.0	0.0
	Data (without initial value)	6.1	6.1
	Constant Data	0.2	0.2
Sample program	Code	4.2	4.8
	Data (with initial value)	0.1	0.0
	Data (without initial value)	0.8	0.8
	Constant Data	1.8	1.9

###### (2) CA55 ver.

Items		Memory Size	
		EWARM [kBytes]	e <sup>2</sup> studio [kBytes]
A-format driver	Code	6.1	5.9
	Data (with initial value)	0.0	0.0
	Data (without initial value)	6.7	6.8
	Constant Data	0.3	0.3
Sample program	Code	6.5	8.5
	Data (with initial value)	0.2	0.0
	Data (without initial value)	0.8	0.9
	Constant Data	1.9	2.1

## 3.2 Hardware Information

### 3.2.1 Device

RZ/T2H

### 3.2.2 Target Board

#### (1) Board Name

RZ/T2H Evaluation Board (RTK9RZT2Hxxxxxxxx)

#### (2) Setting of Target Board

The target board configuration is as follows.

SW1-6: OFF

SW2-1: ON, SW2-2: OFF

SW2-7: OFF

SW2-8: OFF

SW14-1: ON, SW14-2: OFF, SW14-3: ON, SW14-6: OFF (Set xSPI1 boot mode)

CN39: Short between 2-3 pins (Set VDD1833\_2 to 3.3 V)

CN40: Short between 2-3 pins (Set VDD1833\_3 to 3.3 V)

CN78: Short between 1-2 pins, Open between 3-4 pins, and between 5-6 pins (Set VDD1833\_6 to 3.3 V)

Note: To use Target board RTK9RZT2H0CW1000BJ with connecting RS-485 board, power on/off by plugging and unplugging to the power-supply connector CN47 with keeping the slide switch SW16 on.

#### (3) Used Pin for Target Board

The correspondence between the pin used as the encoder I/F and the pin header of the target board is as follows.

Channel	Port Name	Pin Header	Input/Output	Voltage Domain	Description
AFMT0	ENCIFDI00 (SDAT)	CN2 #9	Input	VDD33	Data input
	ENCIFDO00 (REQ)	CN2 #7	Output	VDD33	Data output
	ENCIFOE00 (D/R)	CN2 #5	Output	VDD33	Drive/receive control
AFMT1	ENCIFDI01 (SDAT)	CN2 #8	Input	VDD1833_3	Data input
	ENCIFDO01 (REQ)	CN2 #6	Output	VDD1833_3	Data output
	ENCIFOE01 (D/R)	CN2 #4	Output	VDD1833_3	Drive/receive control
AFMT2	ENCIFDI02 (SDAT)	CN2 #17	Input	VDD33	Data input
	ENCIFDO02 (REQ)	CN2 #15	Output	VDD33	Data output
	ENCIFOE02 (D/R)	CN2 #13	Output	VDD33	Drive/receive control
AFMT3	ENCIFDI03 (SDAT)	CN2 #18	Input	VDD33	Data input
	ENCIFDO03 (REQ)	CN2 #16	Output	VDD33	Data output
	ENCIFOE03 (D/R)	CN2 #14	Output	VDD33	Drive/receive control
AFMT4	ENCIFDI04 (SDAT)	CN2 #27	Input	VDD1833_5	Data input
	ENCIFDO04 (REQ)	CN2 #25	Output	VDD1833_5	Data output
	ENCIFOE04 (D/R)	CN2 #23	Output	VDD33	Drive/receive control
AFMT5	ENCIFDI05 (SDAT)	CN2 #26	Input	VDD1833_6	Data input
	ENCIFDO05 (REQ)	CN2 #24	Output	VDD1833_6	Data output
	ENCIFOE05 (D/R)	CN2 #22	Output	VDD1833_6	Drive/receive control
AFMT6	ENCIFDI06 (SDAT)	CN3 #9	Input	VDD1833_3	Data input
	ENCIFDO06 (REQ)	CN3 #7	Output	VDD1833_3	Data output
	ENCIFOE06 (D/R)	CN3 #5	Output	VDD1833_3	Drive/receive control

Channel	Port Name	Pin Header	Input/Output	Voltage Domain	Description
AFMT7	ENCIFDI07 (SDAT)	CN3 #8	Input	VDD1833_3	Data input
	ENCIFDO07 (REQ)	CN3 #6	Output	VDD1833_3	Data output
	ENCIFOE07 (D/R)	CN3 #4	Output	VDD1833_3	Drive/receive control
AFMT8	ENCIFDI08 (SDAT)	CN3 #17	Input	VDD33	Data input
	ENCIFDO08 (REQ)	CN3 #15	Output	VDD33	Data output
	ENCIFOE08 (D/R)	CN3 #13	Output	VDD33	Drive/receive control
AFMT9	ENCIFDI09 (SDAT)	CN3 #18	Input	VDD1833_2	Data input
	ENCIFDO09 (REQ)	CN3 #16	Output	VDD1833_2	Data output
	ENCIFOE09 (D/R)	CN3 #14	Output	VDD1833_2	Drive/receive control
AFMT10	ENCIFDI10 (SDAT)	CN3 #27	Input	VDD1833_2	Data input
	ENCIFDO10 (REQ)	CN3 #25	Output	VDD1833_2	Data output
	ENCIFOE10 (D/R)	CN3 #23	Output	VDD1833_2	Drive/receive control
AFMT11	ENCIFDI11 (SDAT)	CN3 #26	Input	VDD1833_2	Data input
	ENCIFDO11 (REQ)	CN3 #24	Output	VDD1833_2	Data output
	ENCIFOE11 (D/R)	CN3 #22	Output	VDD1833_2	Drive/receive control
AFMT12	ENCIFDI12 (SDAT)	CN10 #9	Input	VDD1833_6	Data input
	ENCIFDO12 (REQ)	CN10 #7	Output	VDD1833_6	Data output
	ENCIFOE12 (D/R)	CN10 #5	Output	VDD1833_6	Drive/receive control
AFMT13	ENCIFDI13 (SDAT)	CN10 #8	Input	VDD1833_6	Data input
	ENCIFDO13 (REQ)	CN10 #6	Output	VDD1833_6	Data output
	ENCIFOE13 (D/R)	CN10 #4	Output	VDD1833_6	Drive/receive control
AFMT14	ENCIFDI14 (SDAT)	CN10 #17	Input	VDD33	Data input
	ENCIFDO14 (REQ)	CN10 #15	Output	VDD33	Data output
	ENCIFOE14 (D/R)	CN10 #13	Output	VDD33	Drive/receive control
AFMT15	ENCIFDI15 (SDAT)	CN10 #18	Input	VDD33	Data input
	ENCIFDO15 (REQ)	CN10 #16	Output	VDD33	Data output
	ENCIFOE15 (D/R)	CN10 #14	Output	VDD33	Drive/receive control

### 3.3 Procedures on Development Environments: CR52 ver.

#### 3.3.1 Preparation before Executing the Sample Program

This sample program communicates with a PC. The USB connection terminal on the target board is CN34. Select higher-numbered port from COM ports that appear at connecting the board with the host PC.

The terminal software of the host PC is set as shown in the following table.

Function	Setting
Communication method	Asynchronous serial transmission/reception
Order of transmission / reception	LSB first
Transfer rate	19200 bps
Character length	8 bits
Stop bit length	1 bit
Parity function	None
Hardware flow control	None

#### 3.3.2 EWARM from IAR Systems

##### (1) Build Environment

IAR Embedded Workbench for ARM (EWARM)

Version 9.60.2 + patch (EWARM\_Patch\_for\_RZT2H\_N2H\_rev1.0)

RENESAS FSP Smart Configurator (FSP SC) 2024-10

RENESAS Flexible Software Package (FSP) for RZ/T2 v2.2.0

##### (2) Execution Environment ICE

IAR I-jet

##### (3) Build Procedure for Sample Programs

The build procedure for the sample program is as follows.

- 1 Extract RZ\_T2H\_CR52\_a\_as.zip and copy the extracted source files to the desired location.
- 2 Activate EWARM.
- 3 Select [File] menu -> [Open Workspace].
- 4 Open the extracted source file RZ\_T2H\_a\_as.eww.
- 5 Start the FSP Smart Configurator from the [Tools] menu of the EWARM IDE. \*

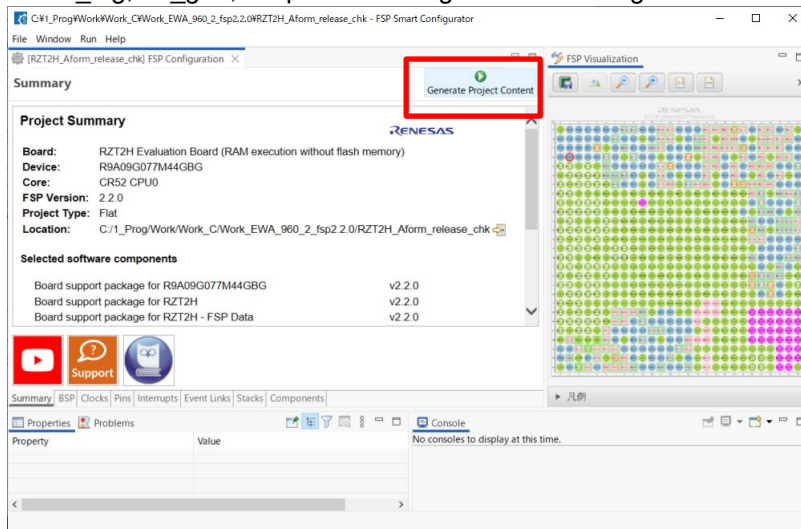
Note: The following procedure adds the activation of the FSP Smart Configurator to the [Tools] menu of the EWARM IDE. Select [Tools] menu -> [Tool Configuration] in the EWARM IDE. Select the [New] button, specify a table string in each field, and press [OK].

Field	String
Menu text	FSP Smart Configurator
Command	\$RASC_EXE_PATH\$
Argument	--compiler IAR configuration.xml
Initial directory	\$PROJ_DIR\$

String for the command is variable holding the path of the Smart Configurator execution file, rasc.exe. You can also start the FSP Smart Configurator directly from the command prompt by specifying the folder where it is installed.



- 6 In the FSP Configuration pane of the Smart Configurator, click Generate Project Content. The rzt, rzt\_cfg, rzt\_gen, script and .setting folders will be generated.



- 7 When project generation is complete, close the Smart Configurator.  
 8 Select [Rebuild ALL] from the [Project] menu of EWARM.  
 The file Debug\Exe\RZ\_T2H\_a\_as.out is generated.

#### (4) Sample Program Execution Procedure

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

- 1 Select [Project] menu -> [Download and Debug].
- 2 Select [Debug] menu -> [Execute].

#### (5) Execution Result of the Sample Program

Run the sample program and enter commands in the terminal software window. For commands, see 4.11.8 console commands in the RZ/T2H Group A-format Sample Program Application Note.

```

COM10 - Tera Term VT
ファイル(F) 編集(E) 設定(S) コントロール(O) ウィンドウ(W) ヘルプ(H)
A-format sample program start
R_A_AS_GetVersion = 2.0

a_as >req 1 0DF0
req command
-----
ENC1
R_A_AS_REQ_SUCCESS
EA : 0
ES : 0
CC : 0
ABS 40bit [39:32] : 0x00000000
ABS 40bit [31:0] : 0x00454E73

a_as >
  
```

### 3.3.3 e<sup>2</sup> studio from RENESAS

#### (1) Build Environment

RENESAS e<sup>2</sup> studio 2024-10

Toolchain version: GNU ARM Embedded 12.2.1.arm-12-24

RENESAS Flexible Software Package (FSP) for RZ/T2 v2.2.0

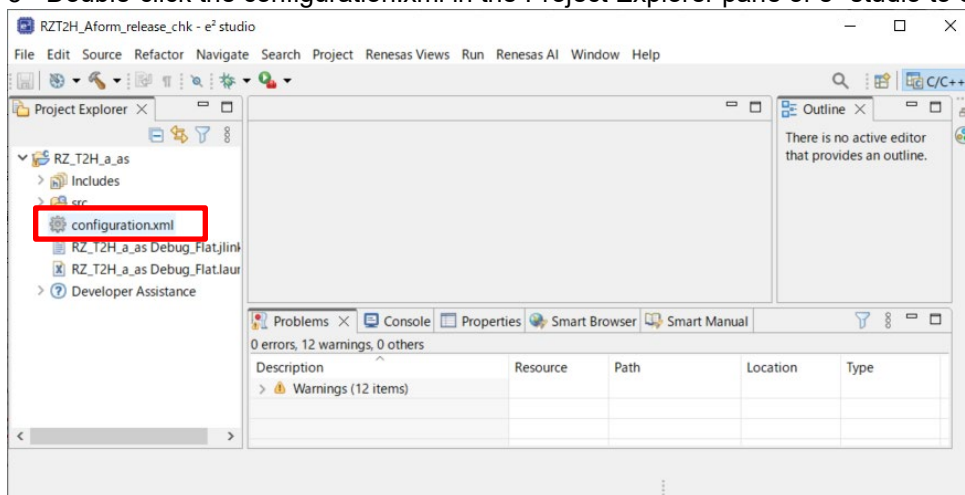
#### (2) Execution Environment ICE

SEGGER J-Link v7.98c

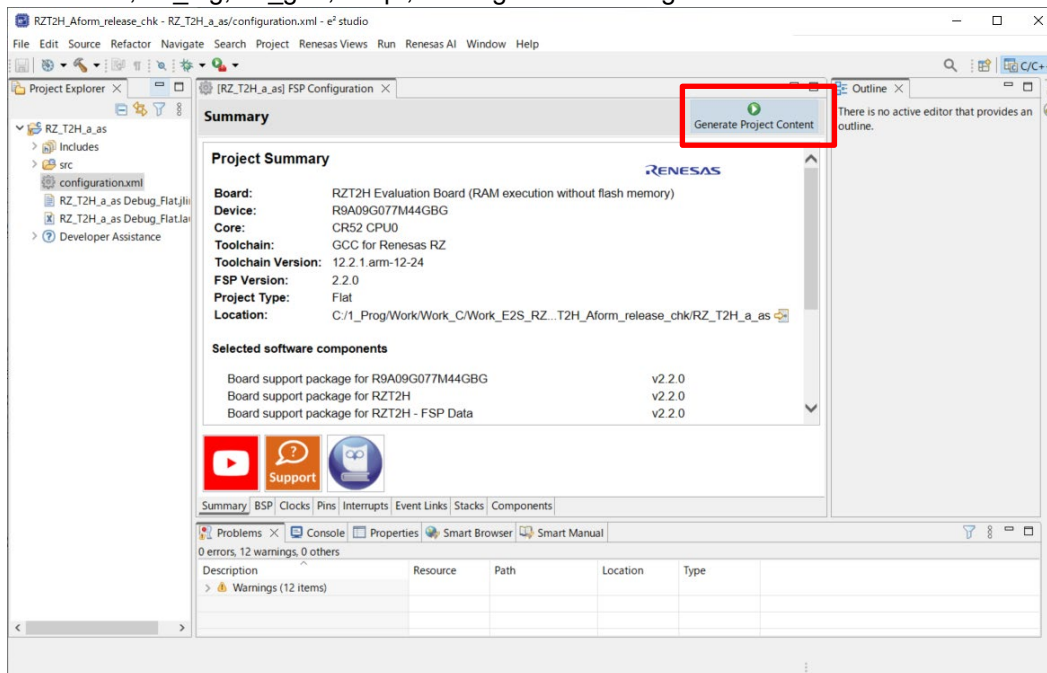
#### (3) Build Procedure of the Sample Program

The procedure for building the sample program is as follows.

- 1 Extract RZ\_T2H\_CR52\_a\_as.zip and copy the extracted source files to the desired location.
- 2 After launching e<sup>2</sup> studio and moving to the workspace, click the [File] menu -> [Import] and select Existing project to workspace and click [Next].
- 3 On the project import screen, select the folder where the sample program was expanded as the root directory.
- 4 Select a project, check Copy Project to Workspace, and click [Finish].
- 5 Double-click the configuration.xml in the Project Explorer pane of e<sup>2</sup> studio to open it.



- 6 Click Generate Project Content in the FSP Configuration pane of e<sup>2</sup> studio.  
The rzt, rzt\_cfg, rzt\_gen, script, .settings folders are generated.



- 7 Select [Project] menu -> [Build All]  
The Debug\RZ\_T2H\_a\_as.elf file is generated.

#### (4) Execution Procedure of the Sample Program

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

- 1 Select [Run] menu -> [Debug As] -> [Renesas GDB Hardware Debugging].
- 2 Click [Debug] to start downloading to internal RAM.
- 3 Click [Run] menu -> [Resume] to run the sample program.

#### (5) Execution Result of the Sample Program

Run the sample program and enter commands in the terminal software window. For commands, see 4.11.8 console commands in the RZ/T2H Group A-format Sample Program Application Note.

```

COM10 - Tera Term VT
ファイル(F) 編集(E) 設定(S) コントロール(O) ウィンドウ(W) ヘルプ(H)
A-format sample program start
R_A_AS_GetVersion = 2.0

a_as >req 1 00F0
req command
-----
ENC1
R_A_AS_REQ_SUCCESS
EA : 0
ES : 0
OC : 0
ABS 40bit [39:32] : 0x00000000
ABS 40bit [31:0] : 0x00454E73

a_as >

```

### 3.4 Procedures on Development Environments: CA55 ver.

#### 3.4.1 Preparation before Executing the Sample Program

This sample program communicates with a PC. The USB connection terminal on the target board is CN34. Select lower-numbered port from COM ports that appear at connecting the board with the host PC.

The terminal software of the host PC is set as shown in the following table.

Function	Setting
Communication method	Asynchronous serial transmission/reception
Order of transmission / reception	LSB first
Transfer rate	19200 bps
Character length	8 bits
Stop bit length	1 bit
Parity function	None
Hardware flow control	None

#### 3.4.2 EWARM from IAR Systems

##### (1) Build Environment

IAR Embedded Workbench for ARM (EWARM)

Version 9.60.2 + patch (EWARM\_Patch\_for\_RZT2H\_N2H\_rev1.0)

RENESAS FSP Smart Configurator (FSP SC) 2024-10

RENESAS Flexible Software Package (FSP) for RZ/T2 v2.2.0

##### (2) Execution Environment ICE

IAR I-jet

##### (3) Build Procedure for Sample Programs

The build procedure for the sample program is as follows.

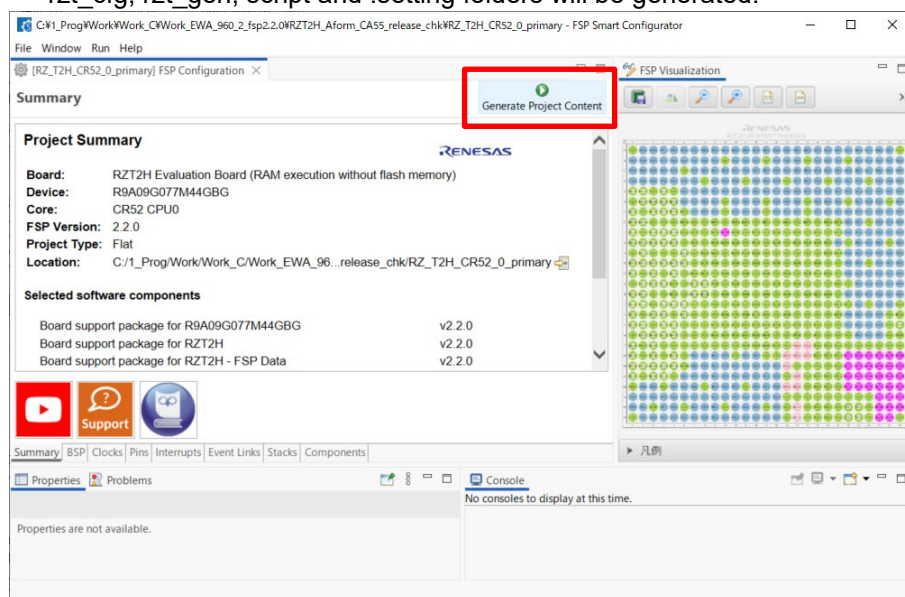
- 1 Extract RZ\_T2H\_CA55\_a\_as.zip and copy the extracted source files to the desired location.
- 2 Activate EWARM.
- 3 Select [File] menu -> [Open Workspace].
- 4 Open the extracted source file RZ\_T2H\_CR52\_0\_primary -> RZ\_T2H\_CR52\_0\_primary.eww.
- 5 Start the FSP Smart Configurator from the [Tools] menu of the EWARM IDE. \*

Note: The following procedure adds the activation of the FSP Smart Configurator to the [Tools] menu of the EWARM IDE. Select [Tools] menu -> [Tool Configuration] in the EWARM IDE. Select the [New] button, specify a table string in each field, and press [OK].

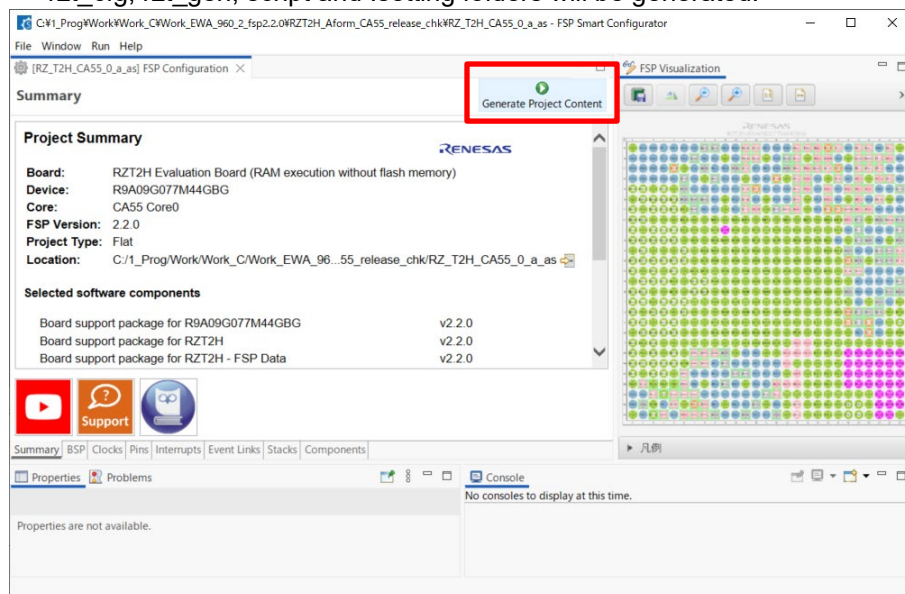
Field	String
Menu text	FSP Smart Configurator
Command	\$RASC_EXE_PATH\$
Argument	--compiler IAR configuration.xml
Initial directory	\$PROJ_DIR\$

String for the command is variable holding the path of the Smart Configurator execution file, rasc.exe. You can also start the FSP Smart Configurator directly from the command prompt by specifying the folder where it is installed.

- 6 In the FSP Configuration pane of the Smart Configurator, click Generate Project Content. The rzt, rzt\_cfg, rzt\_gen, script and .setting folders will be generated.



- 7 When project generation is complete, close the Smart Configurator.  
 8 Select [Rebuild ALL] from the [Project] menu of EWARM.  
 The file Debug\Exe\RZ\_T2H\_CR52\_0\_primary.sbd is generated.  
 9 Select [File] menu -> [Open Workspace].  
 10 Open the extracted source file RZ\_T2H\_CA55\_0\_a\_as → RZ\_T2H\_CA55\_0\_a\_as.eww.  
 (RZ\_T2H\_CR52\_0\_primary.sbd of the primary project is referenced to open this workspace file.  
 Please build the primary project in advance.)  
 11 Start the FSP Smart Configurator from the [Tools] menu of the EWARM IDE.  
 12 In the FSP Configuration pane of the Smart Configurator, click Generate Project Content. The rzt, rzt\_cfg, rzt\_gen, script and .setting folders will be generated.



- 13 When project generation is complete, close the Smart Configurator.  
 14 Select [Rebuild ALL] from the [Project] menu of EWARM.  
 The file Debug\Exe\RZ\_T2H\_CA55\_0\_a\_as.out is generated.

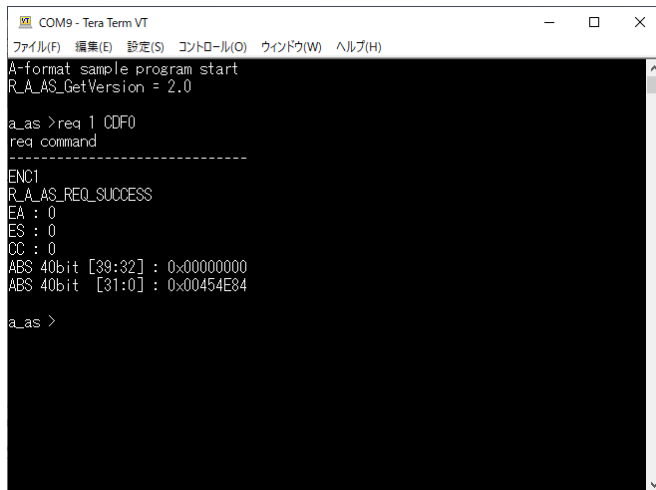
#### (4) Sample Program Execution Procedure

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

- 1 In the workspace of RZ\_T2H\_CR52\_0\_primary, select [Project] menu -> [Download and Debug]. RZ\_T2H\_CA55\_0\_a\_as project is launched.
- 2 In the workspace of RZ\_T2H\_CR52\_0\_primary, select [Debug] menu -> [Execute]. CA55 start-up program is executed.
- 3 In the workspace of RZ\_T2H\_CA55\_0\_a\_as, select [Debug] menu -> [Execute]. Sample program is executed.

#### (5) Execution Result of the Sample Program

Run the sample program and enter commands in the terminal software window. For commands, see 4.11.8 console commands in the RZ/T2H Group A-format Sample Program Application Note.



```

COM9 - Tera Term VT
ファイル(F) 編集(E) 設定(S) コントロール(O) ウィンドウ(W) ヘルプ(H)
A-format sample program start
R_A_AS_GetVersion = 2.0

a_as >req 1 CDF0
req command
-----
ENC1
R_A_AS_REQ_SUCCESS
EA : 0
ES : 0
CC : 0
ABS 40bit [39:32] : 0x00000000
ABS 40bit [31:0] : 0x00454E84

a_as >

```

### 3.4.3 e<sup>2</sup> studio from RENESAS

#### (1) Build Environment

RENESAS e<sup>2</sup> studio 2024-10

Toolchain version:

GNU ARM Embedded 12.2.1.arm-12-24 (Used by RZ\_T2H\_CR52\_0\_primary.)

GCC ARM A-Profile (Aarch64 bare-metal) 10.3.1.20210621 (Used by RZ\_T2H\_CA55\_0\_a\_as.)

RENESAS Flexible Software Package (FSP) for RZ/T2 v2.2.0

#### (2) Execution Environment ICE

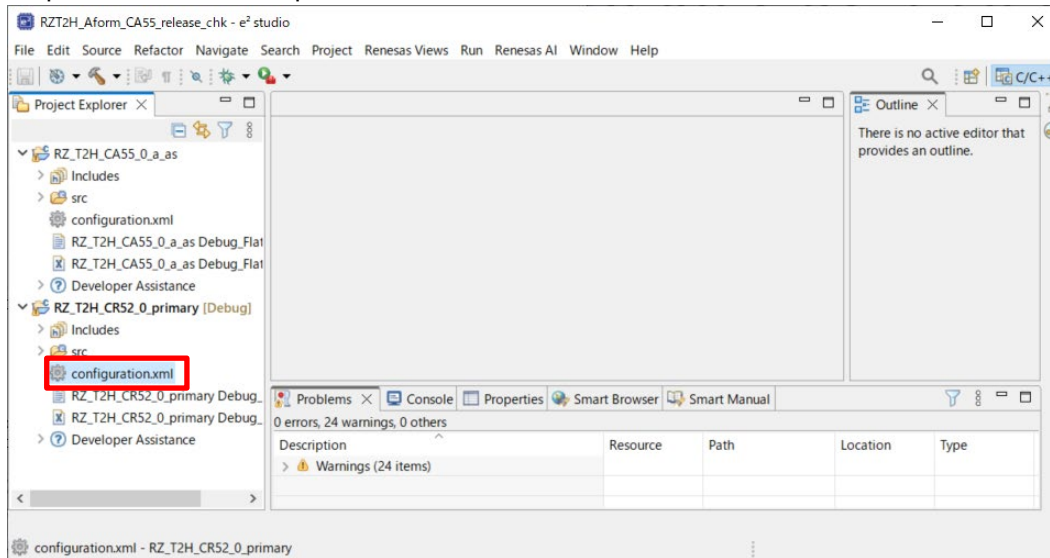
SEGGER J-Link v7.98c

#### (3) Build Procedure of the Sample Program

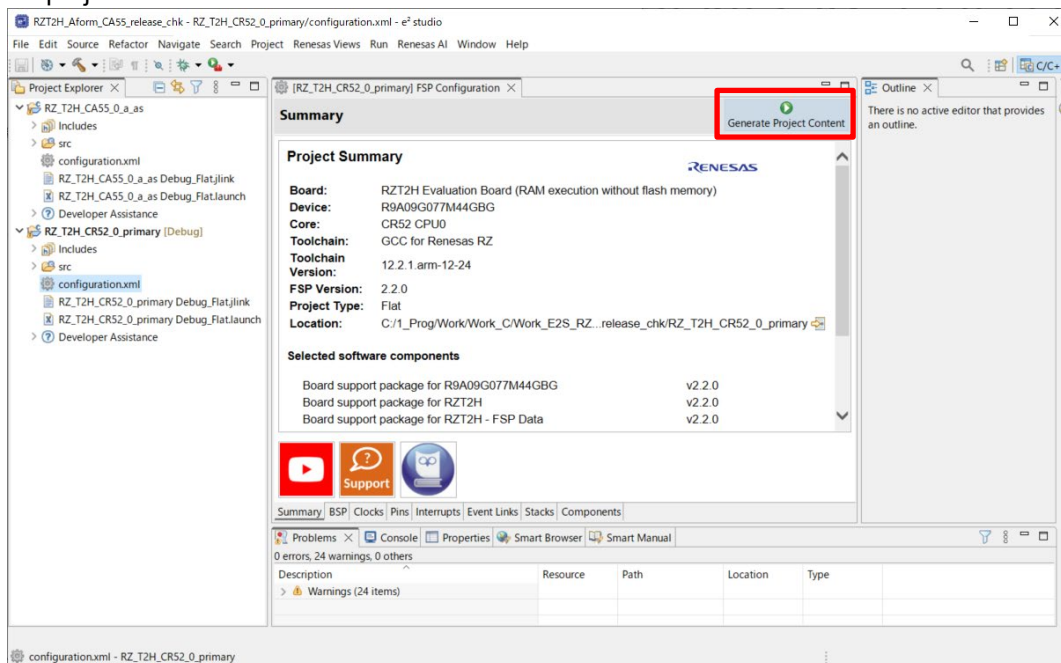
The procedure for building the sample program is as follows.

- 1 Extract RZ\_T2H\_CA55\_a\_as.zip and copy the extracted source files to the desired location.
- 2 After launching e<sup>2</sup> studio and moving to the workspace, click the [File] menu -> [Import] and select Existing project to workspace and click [Next].

- 3 On the project import screen, select the folder where the sample program was expanded as the root directory.
- 4 Select a project, check Copy Project to Workspace, and click [Finish].
- 5 Double-click the configuration.xml of the RZ\_T2H\_CR52\_0\_primary project in the Project Explorer pane of e<sup>2</sup> studio to open it.



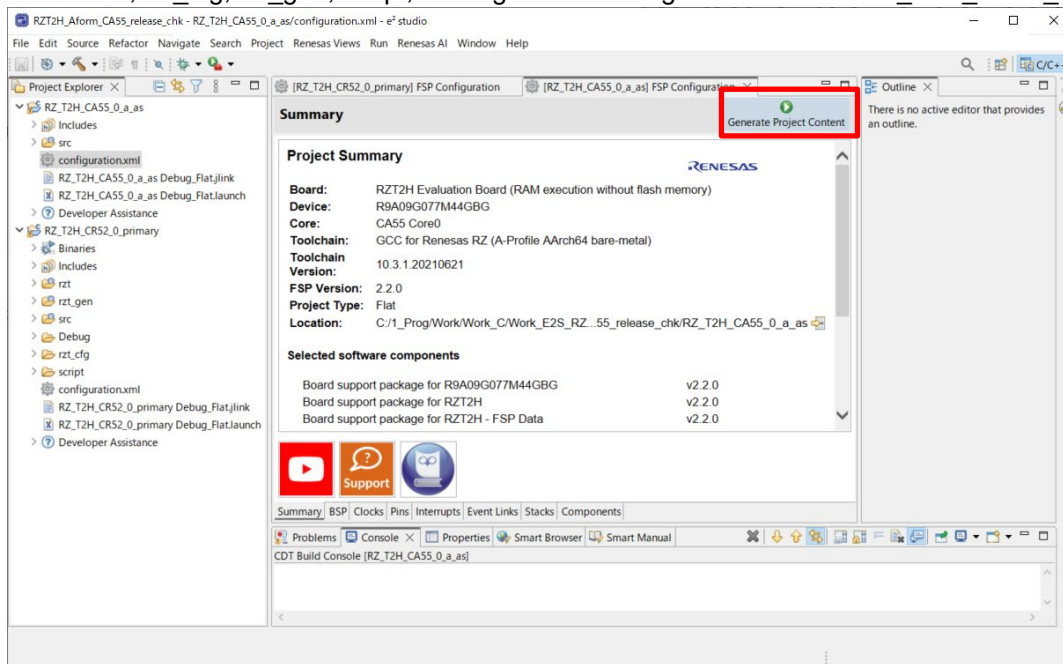
- 6 Click Generate Project Content in the FSP Configuration pane of e<sup>2</sup> studio.  
The rzt, rzt\_cfg, rzt\_gen, script, .settings folders are generated in the RZ\_T2H\_CR52\_0\_primary project.



- 7 Select RZ\_T2H\_CR52\_primary project in the Project Explorer pane and execute [Run] menu -> [Build Project].  
The file Debug\RZ\_T2H\_CR52\_0\_primary.sbd is generated.
- 8 Double-click the configuration.xml of the RZ\_T2H\_CA55\_0\_a\_as project in the Project Explorer pane of e<sup>2</sup> studio to open it. (RZ\_T2H\_CR52\_0\_primary.sbd of the primary project is referenced to open this configuration file. Please build the primary project in advance.)

### 9 Click Generate Project Content in the FSP Configuration pane of e<sup>2</sup> studio.

The rzt, rzt\_cfg, rzt\_gen, script, .settings folders are generated in the RZ\_T2H\_CA55\_0\_a\_as project.



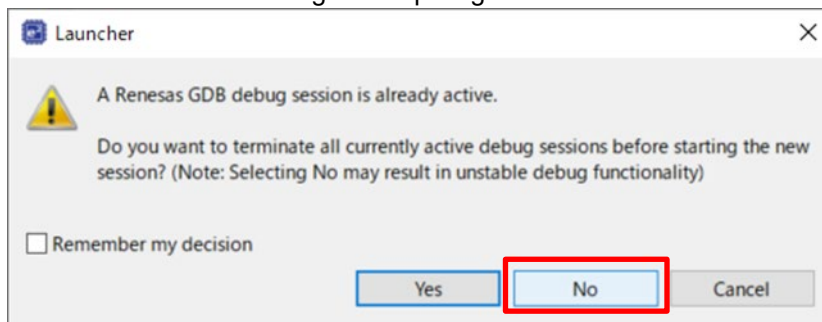
### 10 Select [Project] menu -> [Build All]

The Debug\RZ\_T2H\_CA55\_0\_a\_as.elf file is generated.

### (4) Execution Procedure of the Sample Program

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

- 1 Select [Run] menu -> [Debug As] -> [Renesas GDB Hardware Debugging] for the RZ\_T2H\_CR52\_0\_primary project.  
Click [Debug] to start downloading to internal RAM.
- 2 Click [Run] menu -> [Resume] to run the CA55 start-up program.
- 3 Select [Run] menu -> [Debug As] -> [Renesas GDB Hardware Debugging] for the RZ\_T2H\_CA55\_0\_a\_as project.
- 4 Select 'No' when the dialog box inquiring about termination of the active debug session is displayed.

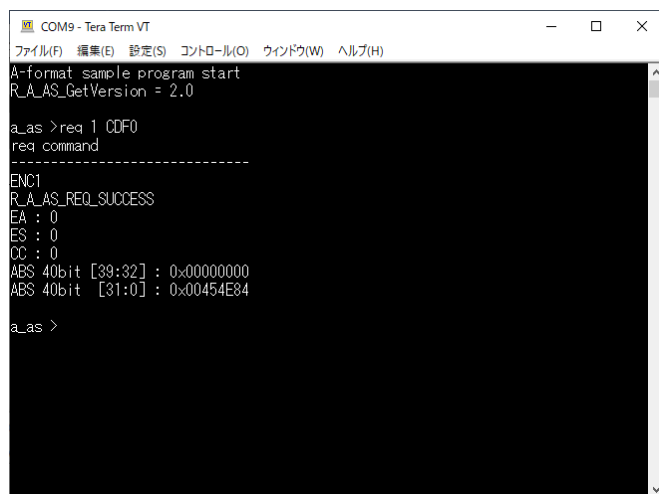


- 5 If 'Proceed with launch' is displayed, select 'Yes'.
- 6 Click [Debug] to start downloading to internal RAM.
- 7 Click [Run] menu -> [Resume] to run the sample program.



## (5) Execution Result of the Sample Program

Run the sample program and enter commands in the terminal software window. For commands, see 4.11.8 console commands in the RZ/T2H Group A-format Sample Program Application Note.



```
COM9 - Tera Term VT
ファイル(F) 編集(E) 設定(S) コントロール(O) ウィンドウ(W) ヘルプ(H)
A-format sample program start
R_A_AS_GetVersion = 2.0

a_as >req 1 CDF0
req command
-----
ENC1
R_A_AS_REQ_SUCCESS
EA : 0
ES : 0
CC : 0
ABS 40bit [39:32] : 0x00000000
ABS 40bit [31:0] : 0x00454E84
a_as >
```

## Revision History

Rev.	Date	Description	
		Page	Summary
0.50	Aug.31.23	-	First Edition issued.
0.60	Oct 13.23	2, 3	Updated the source code and the release note version number. Source code is corrected for preventing command parameter mismatch.
		4	Updated memory size information.
0.70	Mar 29.24	2-3,	Updated the source code and the release note version number. Update file structure.
		4,	Added explanation of CA55 ver. Updated memory size information.
		8-11, 11-17	Update build environment. Added explanation of CA55 ver. Update build and execution procedure. Execution Procedure
2.00	Nov 21.24	2-4	Updated revisions of the application note and the release note. Updated sample program version to 2.0. (Supported FSP v2.2.0.)
		5	Updated the file structure. Updated memory size information.
		6	Add SW14-6 in setting of target board.
		8-17	Updated build environment for FSP v2.2.0. Figures are replaced.
2.01	Dec 13.24	2, 3	Update revision of the release note. Correct path name of the FSP SC in the sample program environment files to use default installation path.

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

## 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

## 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

## 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

## 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

## 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

## 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

## 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

## 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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