Smart Configurator for RL78 Plug-in in e² studio 2025-01
Smart Configurator for RL78 V1.12.0
Release Note

Introduction
Thank you for using the Smart Configurator for RL78.
This document describes the restrictions and points for caution. Read this document before using the product.

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1. Introduction

Smart Configurator is a utility for combining software to meet your needs. It supports the following three functions related to the embedding of Renesas drivers in your systems: importing middleware, generating driver code, and setting pins.
Smart Configurator for RL78 V1.12.0 is equivalent to Smart Configurator for RL78 Plug-in in e2 studio 2025-01.

1.1 System Requirements

The operating environment is as follows.

1.1.1 Windows PC

- System: x64/x86 based processor
  Windows® 11
  Windows® 10 (64-bit version)
- Memory capacity: We recommend 4 GB or more.
- Capacity of hard disk: At least 300 MB of free space.
- Display: Graphics resolution should be at least 1024 x 768, and the mode should display at least 65,536 colors.
- Processor: 1 GHz or higher (must support hyper-threading, multi-core CPUs)

1.1.2 Linux PC

Smart Configurator for RL78 plug-in in e2 studio 2023-01 or later is supported on Linux OS.

- System: x64 based processor, 2 GHz or faster (with multicore CPUs)

  Ubuntu 22.04 LTS Desktop (64-bit version)
  Ubuntu 20.04 LTS Desktop (64-bit version)
- Memory capacity: We recommend 2 GB or more.
- Capacity of hard disk: At least 2 GB of free space.

1.1.3 Mac OS

Smart Configurator for RL78 plug-in in e2 studio 2024-04 or later is supported on Mac OS.

- System: 1.8 GHz or faster 64-bit processor. Dual-core or better recommended. Apple Silicon (arm64) processors are only supported.

  MacOS 13 (Ventura)
- Memory capacity: 4 GB of RAM; 8 GB of RAM recommended.
- Capacity of hard disk: At least 2 GB of free space.
- A screen resolution of 1280 x 800 or higher.

Note: Only LLVM is available for Mac OS.

1.1.4 Development Environments

- Renesas Electronics Compiler for RL78 [CC-RL] V1.14 or later (Windows PC)
- LLVM for Renesas RL78 17.0.1.202409 or later (Windows PC, Linux PC, Mac OS)
- IAR Embedded Workbench for Renesas RL78 V5.10.3 or later (Windows PC)
- SMS Assembler V1.00.00 or later (Windows PC)
- FAA Assembler V1.04.02 or later (Windows PC)
- CS+ for CC V8.13.00 Note1 or later (Windows PC)

Note:

1.Smart Configurator for RL78 V1.12.0 has been evaluated in the CS+ for CC V8.13.00 environment. When using Smart Configurator for RL78 V1.11.0 or lower, please refer to Release Note (R20UT5533EC0100) about the target version of CS+ for CC.

2. Support List

2.1 Support Devices List

Below is a list of devices supported by the Smart Configurator for RL78 V1.12.0.

Table 2-1 Support Devices (1/2)

Group (HW Manual number)	PIN	Device name
RL78/G23 Group (R01UH0896EJ0120)	30pin	R7F100GAFxSP, R7F100GAGxSP, R7F100GAHxSP, R7F100GAJxSP
	32pin	R7F100GBFxNP, R7F100GBGxNP, R7F100GBHxNP, R7F100GBJxNP, R7F100GBFxFP, R7F100GBGxFP, R7F100GBHxFP, R7F100GBJxFP
	36pin	R7F100GCFxLA, R7F100GCGxLA, R7F100GCHxLA, R7F100GCJxLA
	40pin	R7F100GEFxNP, R7F100GEGxNP, R7F100GEHxNP, R7F100GEJxNP
	44pin	R7F100GFFxFP, R7F100GFGxFP, R7F100GFHxFP, R7F100GFJxFP, R7F100GFKxFP, R7F100GFLxFP, R7F100GFNxFP
	48pin	R7F100GGFxFB, R7F100GGGxFB, R7F100GGHxFB, R7F100GGJxFB, R7F100GGKxFB, R7F100GGLxFB, R7F100GGNxFB, R7F100GGFxNP, R7F100GGGxNP, R7F100GGHxNP, R7F100GGJxNP, R7F100GGKxNP, R7F100GGLxNP, R7F100GGNxNP
	52pin	R7F100GJFxFA, R7F100GJGxFA, R7F100GJHxFA, R7F100GJJxFA, R7F100GJKxFA, R7F100GJLxFA, R7F100GJNxFA
	64pin	R7F100GLFxFA, R7F100GLGxFA, R7F100GLHxFA, R7F100GLJxFA, R7F100GLKxFA, R7F100GLLxFA, R7F100GLNxFA, R7F100GLFxFB, R7F100GLGxFB, R7F100GLHxFB, R7F100GLJxFB, R7F100GLKxFB, R7F100GLLxFB, R7F100GLNxFB, R7F100GLFxLA, R7F100GLGxLA, R7F100GLHxLA, R7F100GLJxLA, R7F100GLKxLA, R7F100GLLxLA, R7F100GLNxLA
	80pin	R7F100GMGxFA, R7F100GMHxFA, R7F100GMJxFA, R7F100GMKxFA, R7F100GMLxFA, R7F100GMNxFA, R7F100GMGxFB, R7F100GMHxFB, R7F100GMJxFB, R7F100GMKxFB, R7F100GMLxFB, R7F100GMNxFB
	100pin	R7F100GPGxFB, R7F100GPHxFB, R7F100GPJxFB, R7F100GPKxFB, R7F100GPLxFB, R7F100GPNxFB, R7F100GPGxFA, R7F100GPHxFA, R7F100GPJxFA, R7F100GPKxFA, R7F100GPLxFA, R7F100GPNxFA
	128pin	R7F100GSJxFB, R7F100GSKxFB, R7F100GSLxFB, R7F100GSNxFB
RL78/F24 Group (R01UH0944EJ0100)	32pin	R7F124FBJ3xNP, R7F124FBJ4xNP, R7F124FBJ5xNP
	48pin	R7F124FGJ3xFB, R7F124FGJ4xFB, R7F124FGJ5xFB
	64pin	R7F124FLJ3xFB, R7F124FLJ4xFB, R7F124FLJ5xFB
	80pin	R7F124FMJ3xFB, R7F124FMJ4xFB, R7F124FMJ5xFB
	100pin	R7F124FPJ3xFB, R7F124FPJ4xFB, R7F124FPJ5xFB
RL78/G15 Group (R01UH0959EJ0100)	8pin	R5F12008xNS, R5F12007xNS, R5F12008xSN
	10pin	R5F12018xSP, R5F12017xSP
	16pin	R5F12048xNA, R5F12047xNA, R5F12048xSP, R5F12047xSP
	20pin	R5F12068xSP, R5F12067xSP
RL78/F23 Group (R01UH0944EJ0100)	32pin	R7F123FBG3xNP, R7F123FBG4xNP, R7F123FBG5xNP
	48pin	R7F123FGG3xFB, R7F123FGG4xFB, R7F123FGG5xFB
	64pin	R7F123FLG3xFB, R7F123FLG4xFB, R7F123FLG5xFB
	80pin	R7F123FMG3xFB, R7F123FMG4xFB, R7F123FMG5xFB
RL78/G22 Group (R01UH0978EJ0100)	16pin	R7F102G4ExNP, R7F102G4CxNP
	20pin	R7F102G6ExSP, R7F102G6CxSP
	24pin	R7F102G7ExNP, R7F102G7CxNP
	25pin	R7F102G8ExLA, R7F102G8CxLA
	30pin	R7F102GAExSP, R7F102GACxSP
	32pin	R7F102GBExNP, R7F102GBCxNP, R7F102GBExFP, R7F102GBCxFP
	36pin	R7F102GCExLA, R7F102GCCxLA
	40pin	R7F102GEExNP, R7F102GECxNP
	44pin	R7F102GFExFP, R7F102GFCxFP
	48pin	R7F102GGExFB, R7F102GGExNP, R7F102GGCxFB, R7F102GGCxNP

Table 2-2 Support Devices (2/2)

Group (HW Manual number)	PIN	Device name
RL78/G24 Group (R01UH0961EJ0100)	20pin	R7F101G6GxSP, R7F101G6ExSP
	24pin	R7F101G7GxNP, R7F101G7ExNP
	25pin	R7F101G8GxLA, R7F101G8ExLA
	30pin	R7F101GAGxSP, R7F101GAExSP
	32pin	R7F101GBGxNP, R7F101GBExNP, R7F101GBGxFP, R7F101GBExFP
	40pin	R7F101GEGxNP, R7F101GEExNP
	44pin	R7F101GFGxFP, R7F101GFExFP
	48pin	R7F101GGGxFB, R7F101GGExFB, R7F101GGGxNP, R7F101GGExNP
	52pin	R7F101GJGxFA, R7F101GJExFA
	64pin	R7F101GLGxFA, R7F101GLGxFB, R7F101GLExFA, R7F101GLExFB
RL78/G16 Group (R01UH0980EJ0100)	10pin	R5F1211AxSP, R5F1211CxSP
	16pin	R5F1214AxNA, R5F1214AxSP, R5F1214CxNA, R5F1214CxSP
	20pin	R5F1216AxSP, R5F1216CxSP
	24pin	R5F1217AxNA, R5F1217CxNA
	32pin	R5F121BAxFP, R5F121BAxNA, R5F121BCxFP, R5F121BCxNA
RL78/F25 Group (R01UH1061EJ0050)	48pin	R7F125FGL3xFB, R7F125FGL4xFB
	64pin	R7F125FLL3xFB, R7F125FLL4xFB
	80pin	R7F125FML3xFB, R7F125FML4xFB
	100pin	R7F125FPL3xFB, R7F125FPL4xFB
RL78/F22 Group (R01UH1061EJ0050)	24pin	R7F122F7G3xNP, R7F122F7G4xNP
	32pin	R7F122FBG3xNP, R7F122FBG4xNP
	48pin	R7F122FGG3xFB, R7F122FGG4xFB

2.2 Support Components List

Below is a list of Components supported by the Smart Configurator for RL78 V1.12.0.

Table 2-3 Support Components (1/2) ✓: Support, -: Non-support

No	Components	Mode	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	RL78/F25	Remarks
1	12 Bit A/D Single Scan	-	-	✓	-	✓	-	-	-	✓	
2	12 Bit A/D Continuous Scan	-	-	✓	-	✓	-	-	-	✓	
3	12 Bit A/D Group Scan	-	-	✓	-	✓	-	-	-	✓	
4	A/D Converter	Normal mode	✓	-	✓	-	✓	✓	✓	-	Only RL78/G24 A/D converter has mode selection GUI. For other devices, the default mode is "Normal mode" and no GUI is provided for mode selection.
		Advanced mode	-	-	-	-	-	-	✓	-	
5	Clock Output/Buzzer Output Controller	-	✓	✓	✓	✓	✓	✓	✓	✓	
6	Comparator	-	✓	✓	✓	-	-	✓	✓	✓	
7	D/A Converter	-	✓	✓	-	-	-	-	✓	✓	
8	Data Transfer Controller	-	✓	✓	-	✓	✓	-	✓	✓	
9	Delay Counter	-	✓	✓	✓	✓	✓	✓	✓	✓	
10	Divider Function	-	✓	✓	✓	✓	✓	✓	✓	✓	
11	Event Link Controller	-	–	✓	–	-	✓	–	✓	✓	
12	External Event Counter	-	✓	✓	✓	✓	✓	✓	✓	✓	
13	IIC Communication (Master mode)	-	✓	✓	✓	✓	✓	✓	✓	✓	
14	IIC Communication (Slave mode)	-	✓	✓	✓	✓	✓	✓	✓	✓	
15	Input Capture Function	-	–	✓	–	✓	–	–	✓	✓	
16	Input Pulse Interval/Period Measurement	-	✓	✓	✓	✓	✓	✓	✓	✓	
17	Input Signal High-/Low-Level Width Measurement	-	✓	✓	✓	✓	✓	✓	✓	✓	
18	Interrupt Controller	-	✓	✓	✓	✓	✓	✓	✓	✓	
19	Interval Timer	8 bit count mode	✓	✓	✓	✓	✓	✓	✓	✓	
		12 bit count mode	–	–	✓	–	–	✓	–	–	
		16 bit count mode	✓	✓	✓	✓	✓	✓	✓	✓	
		16 bit capture mode	✓	-	-	-	✓	-	✓	–	
		32 bit count mode	✓	-	-	-	✓	-	✓	–	
20	Key Interrupt	-	✓	✓	-	✓	✓	-	✓	✓	
21	One-Shot Pulse Output	One-Shot Pulse Output	✓	✓	✓	✓	✓	✓	✓	✓	
		Two-Channel Input with One-Shot Pulse Output	–	–	✓	–	–	✓	-	-	
22	Output Compare Function	-	–	✓	–	✓	–	–	✓	✓	
23	Ports	-	✓	✓	✓	✓	✓	✓	✓	✓	
24	PWM Option Unit A	-	–	✓	–	✓	–	-	✓	✓	
25	DALI Communication (Control devices)	-	–	–	–	–	–	–	✓	–	
26	DALI Communication (Control gear)	-	–	–	–	–	–	–	✓	–	
27	Real-Time Clock	-	✓	✓	–	✓	✓	✓	✓	✓	

Table 2-4 Support Components (2/2) ✓: Support, -: Non-support

No	Components	Mode	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	RL78/F25	Remarks
28	PWM Output	PWM Mode	✓	✓	✓	✓	✓	✓	✓	✓	
		PWM3 Mode	–	✓	–	✓	–	–	✓	✓	
		Extended PWM Mode	–	✓	–	✓	–	-	✓	✓	
		PWM2 Mode	–	–	–	–	–	–	✓	-	
		Timer KB3 PWM Output Gate Mode	–	–	–	–	–	–	✓	-	
		Standalone Mode (Period controlled by the TKBCRn0 register)	–	–	–	–	–	–	✓	-	
		Standalone Mode (Period controlled by external trigger input)	–	–	–	–	–	–	✓	-	
		Simultaneous Start/Stop Mode (Period controlled by the TKBCRn0 register)	–	–	–	–	–	–	✓	-	
		Simultaneous Start/Stop Mode (Period controlled by external trigger input)	–	–	–	–	–	–	✓	-	
		Simultaneous Start/Clear Mode (Period controlled by master)	–	–	–	–	–	–	✓	-	
		Interleaved PFC Output Mode	–	–	–	–	–	–	✓	-	
29	Remote Control Signal Receiver	-	✓	–	–	–	–	–	–	-	
30	SNOOZE Mode Sequencer	-	✓	–	–	–	✓	–	–	-	
31	SPI (CSI) Communication	Transmission	✓	✓	✓	✓	✓	✓	✓	✓	
		Reception	✓	✓	✓	✓	✓	✓	✓	✓	
		Transmission/reception	✓	✓	✓	✓	✓	✓	✓	✓	
32	Square Wave Output	-	✓	✓	✓	✓	✓	✓	✓	✓	
33	Three-phase PWM Output	Reset Synchronous PWM Mode	–	✓	–	✓	–	✓	✓	✓	
		Complementary PWM Mode	–	✓	–	✓	–	✓	✓	✓	
		Extended Complementary PWM Mode	–	✓	–	✓	–	✓	✓	✓	
34	UART Communication	Transmission	✓	✓	✓	✓	✓	✓	✓	✓	
		Reception	✓	✓	✓	✓	✓	✓	✓	✓	
		Transmission/reception	✓	✓	✓	✓	✓	✓	✓	✓	
35	Voltage Detector	-	✓	✓	–	✓	✓	–	✓	✓	
36	Watchdog Timer	-	✓	✓	✓	✓	✓	✓	✓	✓	
37	Logic & Event Link Controller	-	✓	–	–	–	–	–	–	-	To use ELCL modules of fixed function, need download in Smart Configurator RL78.
38	Phase Counting Mode	-	–	–	–	–	–	–	✓	-	
39	Programmable Gain Amplifier	-	–	–	–	–	–	–	✓	-	
40	Flexible Application Accelerator	-	–	–	–	–	–	–	✓	-	

Table 2-5 Support Components (1/2) ✓: Support, -: Non-support

No	Components	Mode	RL78/F22	Remarks
1	12 Bit A/D Single Scan	-	✓	
2	12 Bit A/D Continuous Scan	-	✓	
3	12 Bit A/D Group Scan	-	✓	
4	A/D Converter	Normal mode	-	Only RL78/G24 A/D converter has mode selection GUI. For other devices, the default mode is "Normal mode" and no GUI is provided for mode selection.
		Advanced mode	-	
5	Clock Output/Buzzer Output Controller	-	✓	
6	Comparator	-	-	
7	D/A Converter	-	-	
8	Data Transfer Controller	-	✓	
9	Delay Counter	-	✓	
10	Divider Function	-	✓	
11	Event Link Controller	-	-	
12	External Event Counter	-	✓	
13	IIC Communication (Master mode)	-	✓	
14	IIC Communication (Slave mode)	-	✓	
15	Input Capture Function	-	✓	
16	Input Pulse Interval/Period Measurement	-	✓	
17	Input Signal High-/Low-Level Width Measurement	-	✓	
18	Interrupt Controller	-	✓	
19	Interval Timer	8 bit count mode	✓	
		12 bit count mode	–	
		16 bit count mode	✓	
		16 bit capture mode	–	
		32 bit count mode	–	
20	Key Interrupt	-	✓	
21	One-Shot Pulse Output	One-Shot Pulse Output	✓	
		Two-Channel Input with One-Shot Pulse Output	-	
22	Output Compare Function	-	✓	
23	Ports	-	✓	
24	PWM Option Unit A	-	✓	
25	DALI Communication (Control devices)	-	–	
26	DALI Communication (Control gear)	-	–	
27	Real-Time Clock	-	✓	

Table 2-6 Support Components (2/2) ✓: Support, -: Non-support

No	Components	Mode	RL78/F22	Remarks
28	PWM Output	PWM Mode	✓	
		PWM3 Mode	✓	
		Extended PWM Mode	✓	
		PWM2 Mode	-	
		Timer KB3 PWM Output Gate Mode	-	
		Standalone Mode (Period controlled by the TKBCRn0 register)	-	
		Standalone Mode (Period controlled by external trigger input)	-	
		Simultaneous Start/Stop Mode (Period controlled by the TKBCRn0 register)	-	
		Simultaneous Start/Stop Mode (Period controlled by external trigger input)	-	
		Simultaneous Start/Clear Mode (Period controlled by master)	-	
		Interleaved PFC Output Mode	-	
29	Remote Control Signal Receiver	-	-	
30	SNOOZE Mode Sequencer	-	-	
31	SPI (CSI) Communication	Transmission	✓	
		Reception	✓	
		Transmission/reception	✓	
32	Square Wave Output	-	✓	
33	Three-phase PWM Output	Reset Synchronous PWM Mode	✓	
		Complementary PWM Mode	✓	
		Extended Complementary PWM Mode	✓	
34	UART Communication	Transmission	✓	
		Reception	✓	
		Transmission/reception	✓	
35	Voltage Detector	-	✓	
36	Watchdog Timer	-	✓	
37	Logic & Event Link Controller	-	-	To use ELCL modules of fixed function, need download in Smart Configurator RL78.
38	Phase Counting Mode	-	-	
39	Programmable Gain Amplifier	-	-	
40	Flexible Application Accelerator	-	-	

2.3 New support

2.3.1 BSP (Board Support Package) revision update

BSP rev1.80 is supported and will be added as default BSP when creating Smart Configurator project.

2.3.2 Support RL78/F22 devices

See 2.1 Support Devices List for details on supported packages.

2.3.3 Support CMake generation for Smart Configurator with Visual Studio Code

From Smart Configurator for RL78 V1.12.0, when using Visual Studio Code (VS Code) with Renesas Debug extension v25.3.0 or later to create RL78 project by choosing “Renesas: Create RL78 project with Smart Configurator”, CMake project is generated for easier build the driver code generated by Smart Configurator for RL78 on Visual Studio Code. Both CCRL toolchain and LLVM toolchain are supported for CMake generation. For detailed how to use the CMake generation for Smart Configurator, please refer to Renesas VS Code Extensions User Guide.

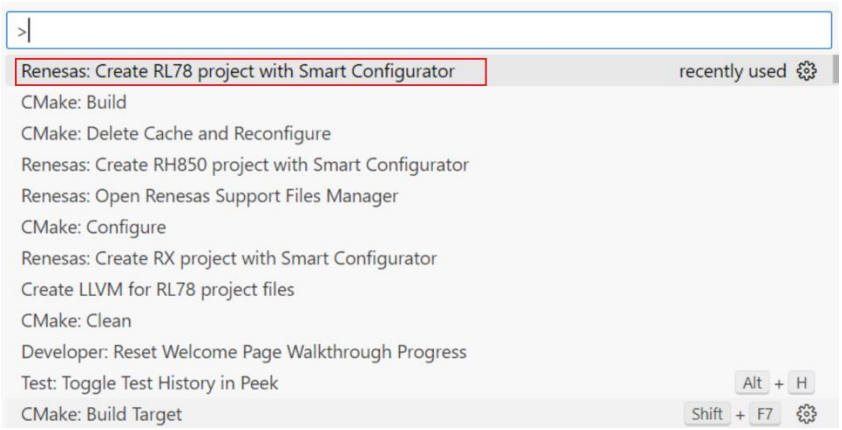


Figure 2-1 Select “Renesas: Create RL78 project with Smart Configurator” in VS Code

Figure 2-2 CMake CCRL project created for VS Code

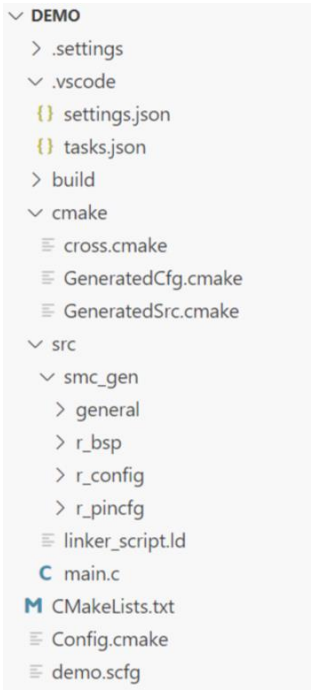


Figure 2-3 CMake LLVM project created for VS Code

Note: Smart Configurator doesn't support Flexible Application Accelerator (FAA) component and SNOOZE Mode Sequencer (SMS) component in CMake project.

2.3.4 Show Smart Configurator version at Overview tab

From Smart Configurator for RL78 V1.12.0, Smart Configurator version is displayed at Overview page.

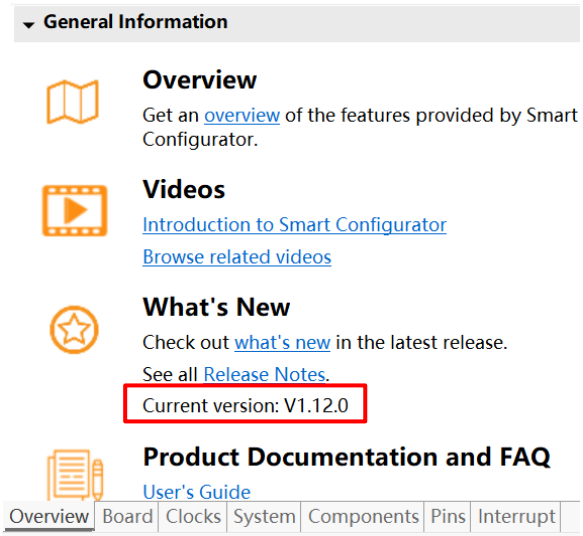


Figure 2-4 Smart Configurator version at Overview page

2.3.5 Support new ELCL feature

From Smart Configurator for RL78 V1.12.0, new ELCL feature was supported which can let user to implement flexible circuit creation in GUI by drag & drop and configure the ELCL elements.

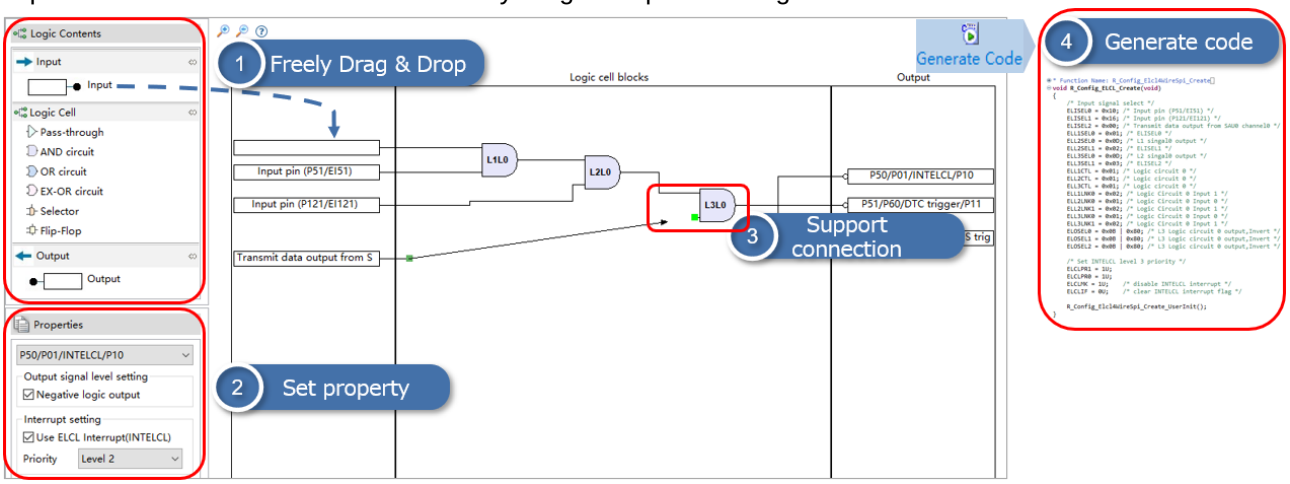


Figure 2-5 New ELCL feature

3. Changes

This chapter describes changes to the Smart Configurator for RL78 V1.12.0.

3.1 Correction of issues/limitations

Table 3-1 List of Correction of issues/limitations (1/2) ✓: Applicable, -: Not Applicable

No	Description	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	RL78/F25	Remarks
1	Fixed the issue of the setting of subsystem clock pin operation is wrong when fCLK is from fMP and fSL is from fIL	–	✓	–	✓	–	–	–	✓	
2	Fixed the issue of 16 bit capture mode with channel 0 and 1 can't be used together with 16 bit count mode with channel 2 and 3	✓	–	–	–	✓	–	✓	–	

Table 3-2 List of Correction of issues/limitations (2/2) ✓: Applicable, -: Not Applicable

No	Description	RL78/F22	Remarks
1	Fixed the issue of the setting of subsystem clock pin operation is wrong when fCLK is from fMP and fSL is from fIL	✓	
2	Fixed the issue of 16 bit capture mode with channel 0 and 1 can't be used together with 16 bit count mode with channel 2 and 3	–	

3.1.1 Fixed the issue of the setting of subsystem clock pin operation is wrong when fCLK is from fMP and fSL is from fIL

When fCLK is from fMP and fSL is from fIL, the generated code about CMC.[EXCLKS, OSCSELS] is wrong in r_bsp_config.h. From Smart Configurator for RL78 V1.12.0, this issue is fixed.

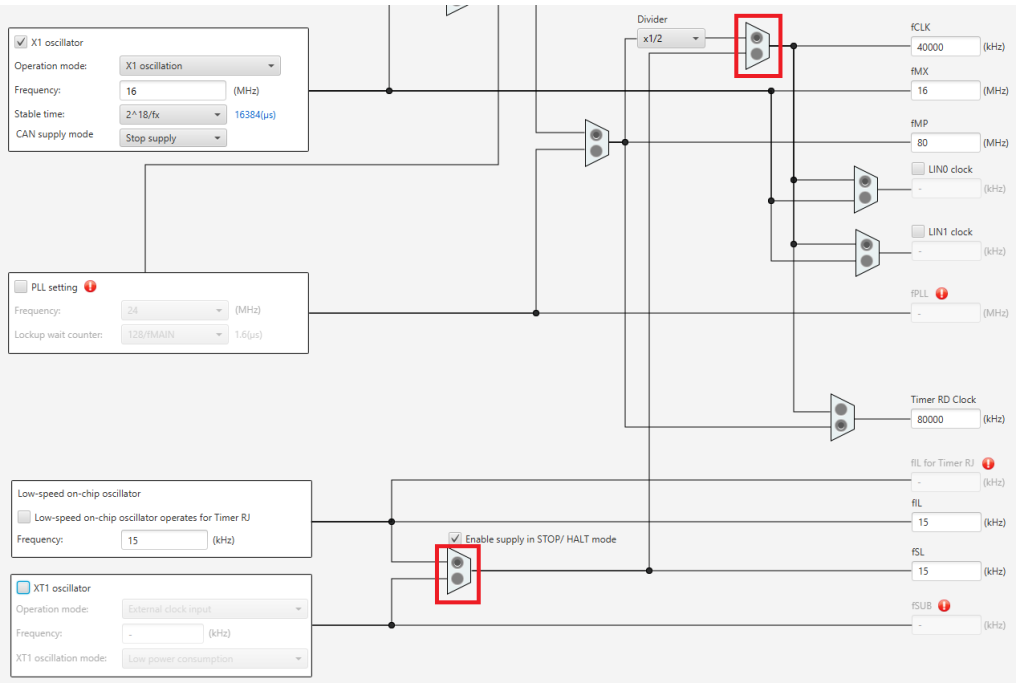


Figure 3-1 fCLK is from fMP and fSL is from fIL in [Clocks] page

3.1.2 Fixed the issue of 16 bit capture mode with channel 0 and 1 can't be used together with 16 bit count mode with channel 2 and 3

If the user wants to use 16 bit count mode with channel 2 and 3 when the user selects 16 bit capture mode and doesn't set "ITLCMP01 compare match interrupt" as "Capture trigger", the user can check "Use 16-bit counter (ITL012 + ITL013)" and sets "Operation clock (fITL1)" and "Interval value".

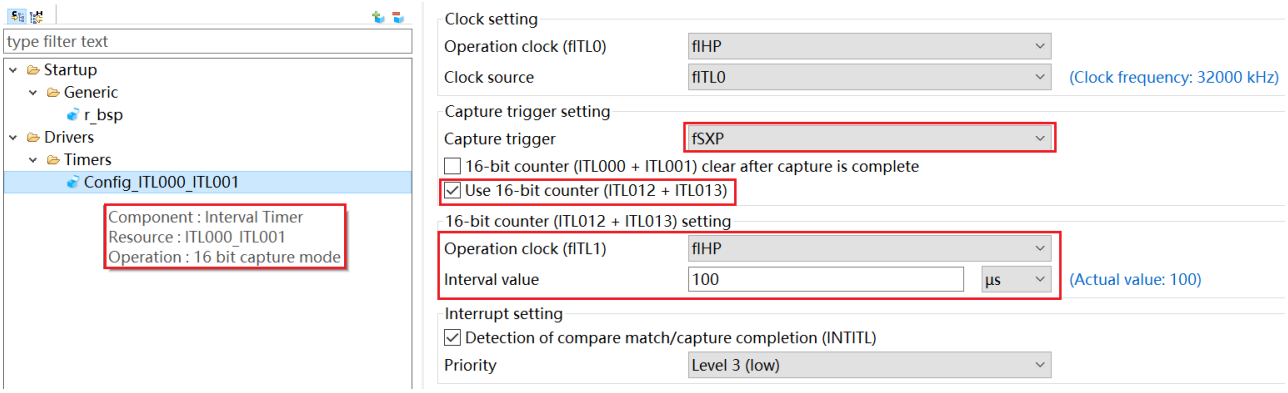


Figure 3-2 Use 16 bit count mode with channel 2 and 3 in 16 bit capture mode

3.2 Specification changes

Table 3-3 List of Specification changes (1/2) ✓: Applicable, -: Not Applicable

No	Description	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	RL78/F25	Remarks
1	Improvement for changing "debug monitor" specification	–	–	✓	–	–	✓	–	–	
2	Improvement for changing CCRL link options about trace RAM and hot plug-in RAM	✓	✓	–	✓	–	–	✓	✓	
3	Improvement for delete RL78/F23 LLVM support in Smart Configurator	–	–	–	✓	–	–	–	–	
4	Improvement for displaying an error icon when VDD and fCLK are not meeting the conditions for I2S communication function	–	–	–	–	–	–	–	✓	
5	Improvement for updating the specification when using Low current conversion mode in A/D Converter	–	–	–	–	–	–	–	✓	
6	Improvement for updating the name of Event Link Controller (ELC) in component tree	–	✓	–	–	✓	–	✓	✓	
7	Improve the specification of input source and output pin in SAU	✓	–	–	–	–	–	–	–	
8	Improve the specification of output pin in UARTA	✓	–	–	–	–	–	–	–	
9	Improve the specification of output pin in TAU	✓	–	–	–	–	–	–	–	
10	Improve the specification of input source in PORT	✓	–	–	–	–	–	–	–	

Table 3-4 List of Specification changes (2/2) ✓: Applicable, -: Not Applicable

No	Description	RL78/F22	Remarks
1	Improvement for changing "debug monitor" specification	–	
2	Improvement for changing CCRL link options about trace RAM and hot plug-in RAM	✓	
3	Improvement for delete RL78/F23 LLVM support in Smart Configurator	–	
4	Improvement for displaying an error icon when VDD and fCLK are not meeting the conditions for I2S communication function	✓	
5	Improvement for updating the specification when using Low current conversion mode in A/D Converter	✓	
6	Improvement for updating the name of Event Link Controller (ELC) in component tree	–	
7	Improve the specification of input source and output pin in SAU	–	
8	Improve the specification of output pin in UARTA	–	
9	Improve the specification of output pin in TAU	–	
10	Improve the specification of input source in PORT	–	

3.2.1 Improvement for changing "debug monitor" specification

Smart Configurator will set "debug monitor" when setting "On-chip debug operation setting" to "Use emulator" or "COM Port".

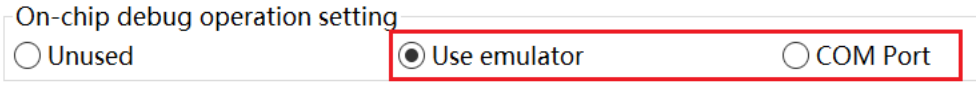


Figure 3-3 Using "On-chip debug operation setting" in [System] page

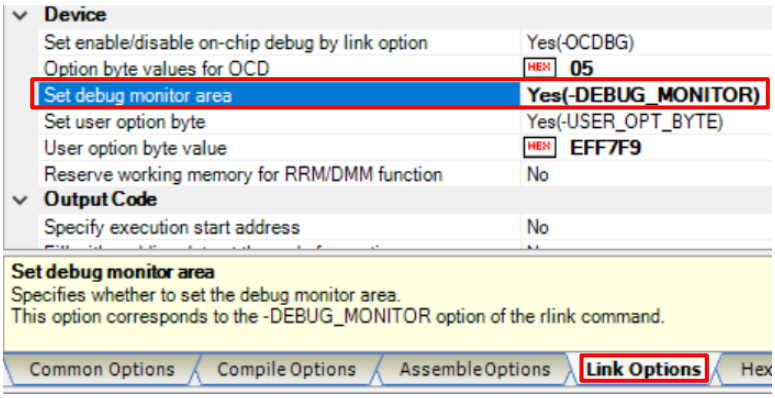


Figure 3-4 Set compiler property "debug monitor" in CS+

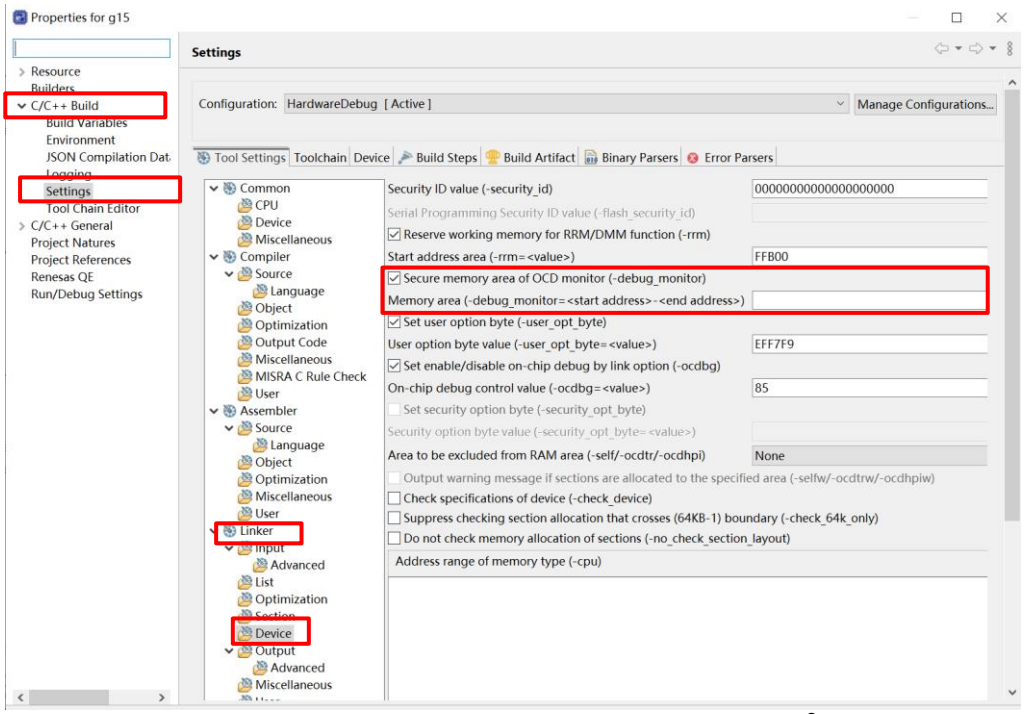


Figure 3-5 Set compiler property "debug monitor" in e2 studio

Note: The supported compilers only include CCRL.

3.2.2 Improvement for changing CCRL link options about trace RAM and hot plug-in RAM

When "On-chip debug operation setting" is set to "Use emulator" or "COM Port" and "Trace function setting" is set to “Used”, the compiler property will be changed after generating code.

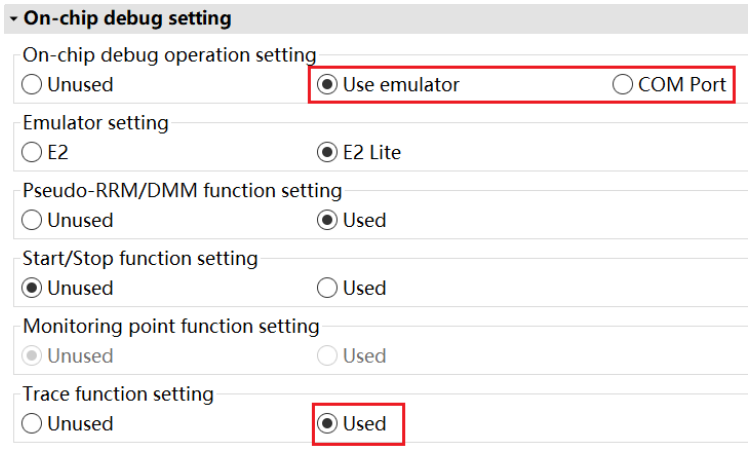


Figure 3-6 Use trace function in [System] page

Smart Configurator will set [Control allocation to trace RAM area] property to [Yes(Exclude trace RAM area)(-STRIDE_OCDTR_AREA)] in CS+.

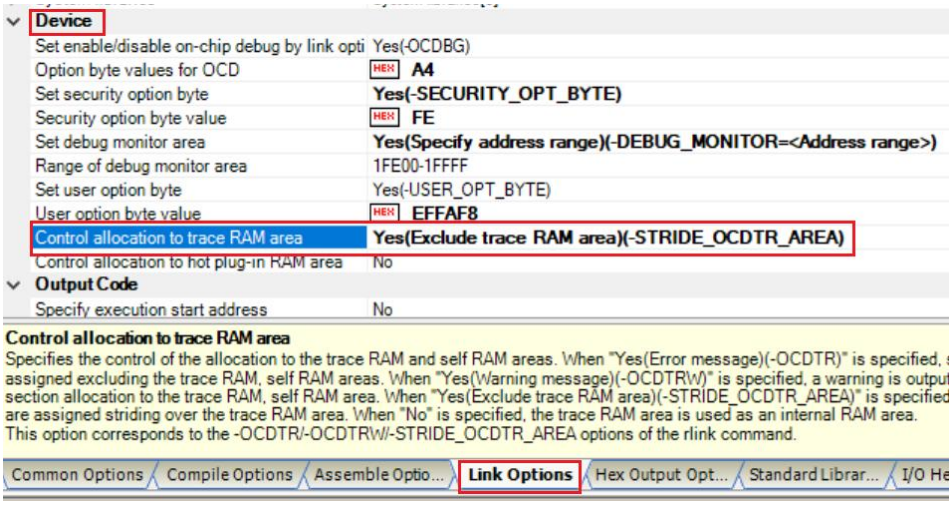


Figure 3-7 [Control allocation to trace RAM area] property in CS+

Smart Configurator will check [Exclude trace RAM area from RAM area (-stride_ocdtr_area)] property in e² studio with CCRL v1.15.

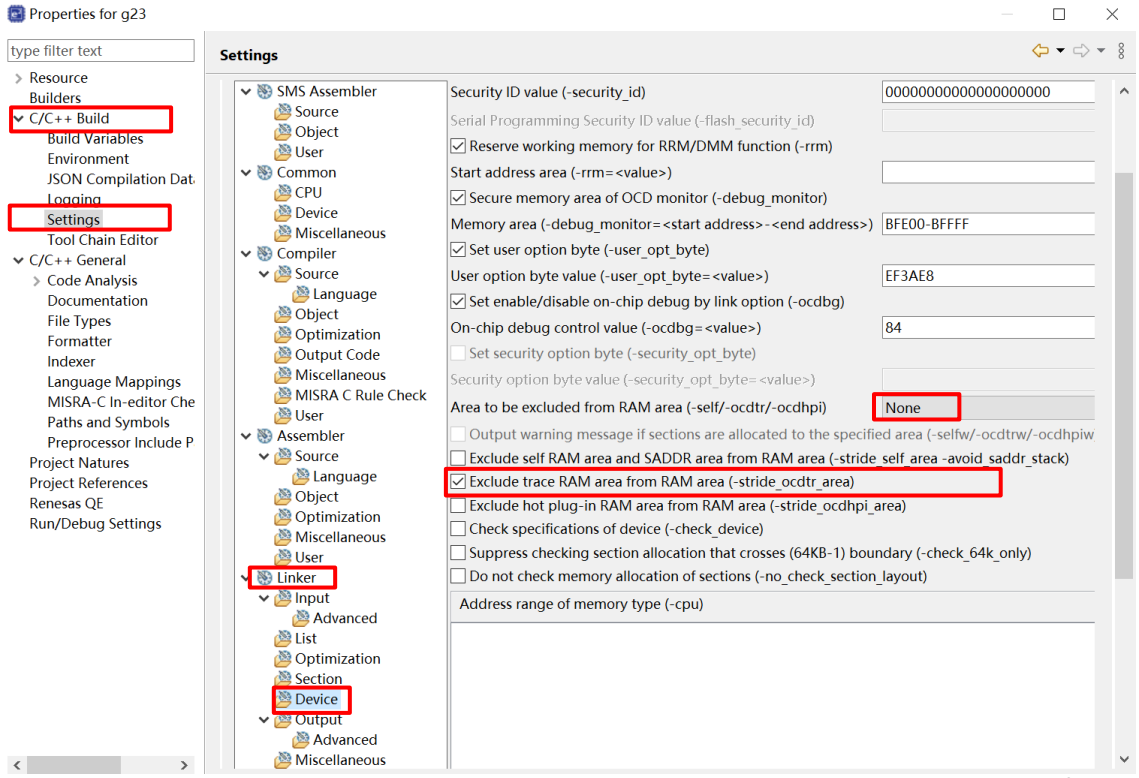


Figure 3-8 [Exclude trace RAM area from RAM area (-stride_ocdtr_area)] property in e² studio

When "On-chip debug operation setting" is set to "Use emulator" or "COM Port" and "Hot plug-in function setting" is set to “Used”, the compiler property will be changed after generating code.

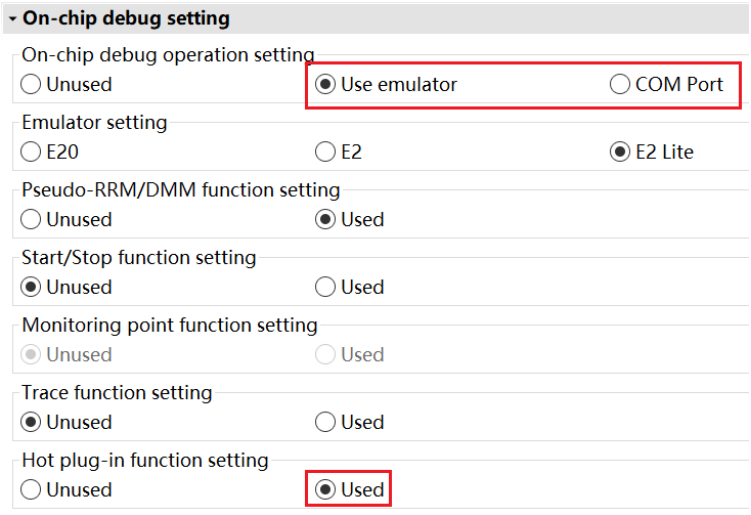


Figure 3-9 Use hot plug-in function in [System] page

Smart Configurator will set [Control allocation to hot plug-in RAM area] property to [Yes(Exclude hot plug-in RAM area)(-STRIDE_OCDHPI_AREA)] in CS+.

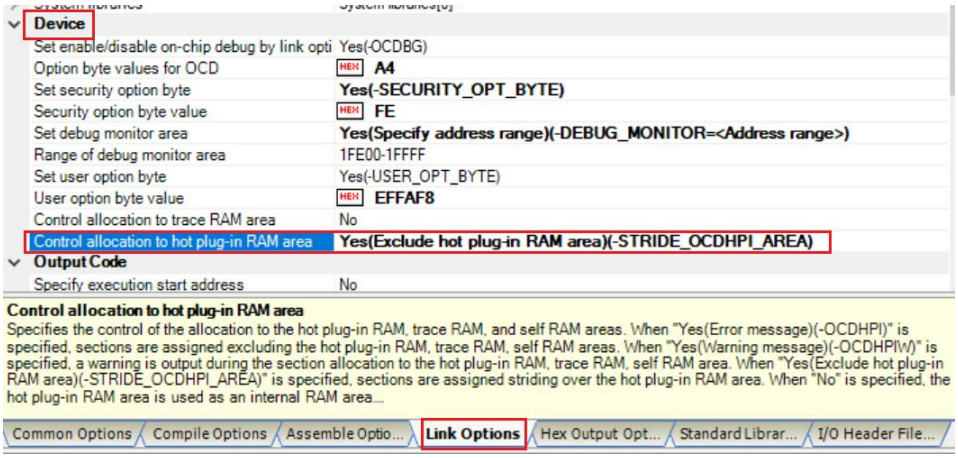


Figure 3-10 [Control allocation to hot plug-in RAM area] property in CS+

Smart Configurator will check [Exclude hot plug-in RAM area from RAM area (-stride_ocdhpi_area)] property in e2 studio with CCRL v1.15.

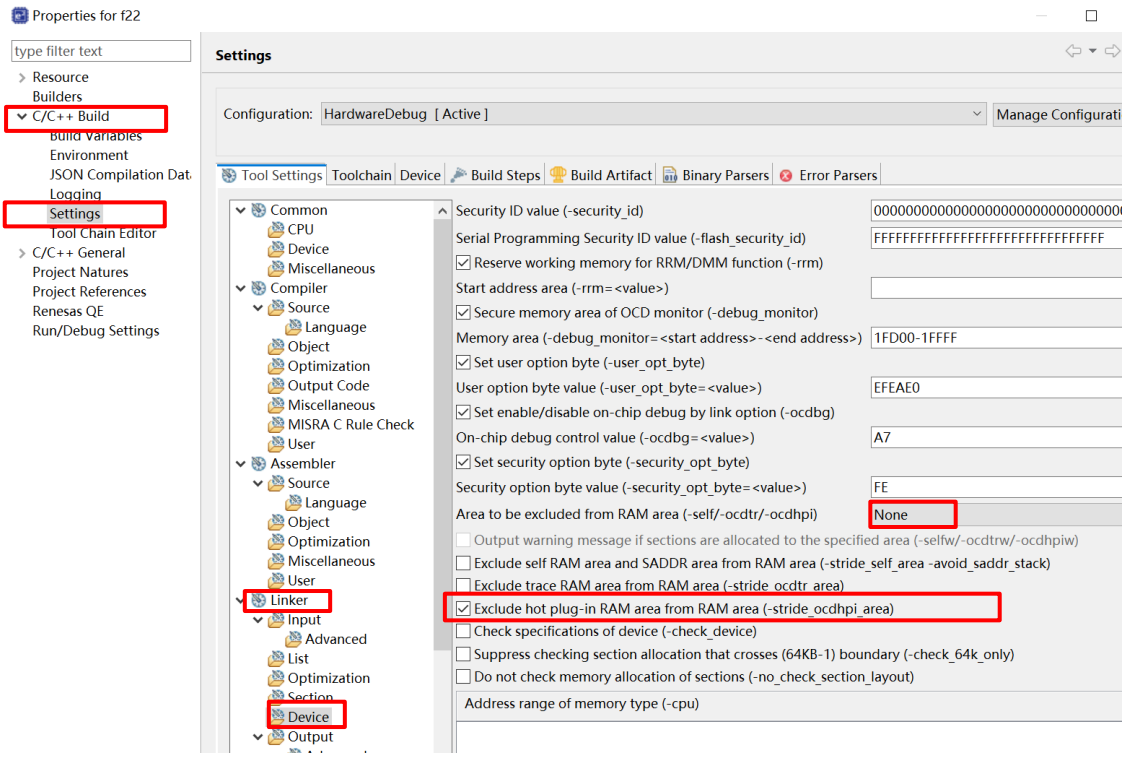


Figure 3-11 [Exclude hot plug-in RAM area from RAM area (-stride_ocdhpi_area)] property in e2 studio

Note: The specification is keeped in e2 studio with CCRL v1.14 or before.

3.2.3 Improvement for delete RL78/F23 LLVM support in Smart Configurator

Smart Configurator doesn't support RL78/F23 LLVM from Smart Configurator for RL78 V1.12.0.

3.2.4 Improvement for displaying an error icon when VDD and fCLK are not meeting the conditions for I2S communication function

The User's Manual (R01UH1061EJ0050) has an error about I2S communication function. If the user wants to use I2S communication function, it should meet the conditions: 2.7 V ⩽ VDD ⩽ 5.5 V and 8 MHz ⩽ fCLK ⩽ 40 MHz. Smart Configurator for RL78 V1.12.0 adds the judgment about VDD and fCLK. If the conditions are not meeted, an error icon will display after checkbox "Enable" in I2S communication function. The User's Manual (R01UH1061EJ0100) will fix this error.

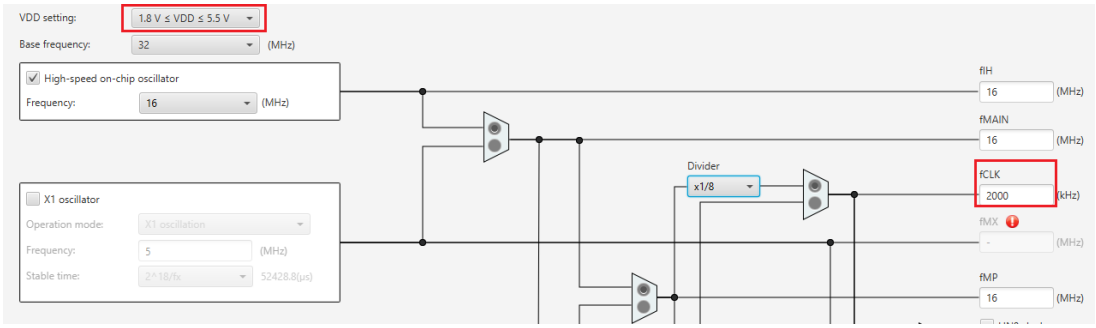


Figure 3-12 VDD and fCLK setting in [Clocks] page

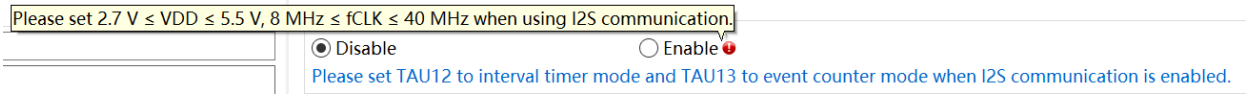


Figure 3-13 The error icon in I2S communication function

3.2.5 Improvement for updating the specification when using Low current conversion mode in A/D Converter

The User's Manual (R01UH1061EJ0050) lacks some Notes when using Low current conversion mode in A/D Converter. Smart Configurator updated A/D Converter GUI and code specification. The User's Manual (R01UH1061EJ0100) will fix these errors.

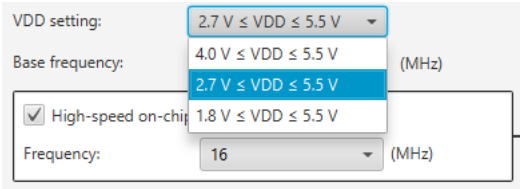


Figure 3-14 VDD setting in [Clocks] page

- GUI specification: Change the sampling time range of ANIn and the conversion time in groupbox “Input sampling time setting”. (n = 0 - 29)

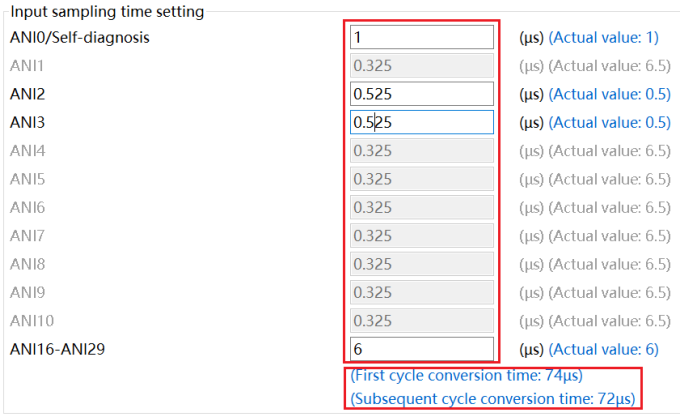


Figure 3-15 Input sampling time setting

When selecting VDD as “4.0 V ⩽ VDD ⩽ 5.5 V” or “2.7 V ⩽ VDD ⩽ 5.5 V”, the min sampling time of ANI0 - ANI15 is 0.337 µs and the min sampling time of ANI16 - ANI29 is 1.012 µs.

When selecting VDD as “1.8 V ⩽ VDD ⩽ 5.5 V”, the min sampling time of ANI0 - ANI15 is 1.688 µs and the min sampling time of ANI16 - ANI29 is 2.563 µs.

When selecting VDD as “1.8 V ⩽ VDD ⩽ 5.5 V”, the time for conversion by successive approximation changes to 40.5 × ADCLK. Smart Configurator updates the messages about conversion time values for “First cycle conversion time” and “Subsequent cycle conversion time”.

- GUI specification: When selecting VDD as “1.8 V ⩽ VDD ⩽ 5.5 V”, Smart Configurator adds an error icon after ANI1 and ANI2.

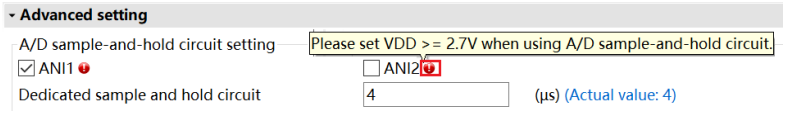


Figure 3-16 The message after ANI1 and ANI2 when VDD is “1.8 V ⩽ VDD ⩽ 5.5 V”

- GUI specification: When selecting VDD as “1.8 V ⩽ VDD ⩽ 5.5 V”, Smart Configurator adds an error icon when Clock source is greater than 8MHz.

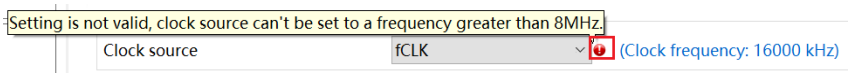


Figure 3-17 The message when “Clock source” is greater than 8MHz

- Code specification: When selecting VDD as “4.0 V ⩽ VDD ⩽ 5.5 V” or “2.7 V ⩽ VDD < 5.5 V”, ADCSR.ADHSC will be set to 0 in API R_Config_S12AD0_Create().

Old driver code

```
/* Set INTAD low priority */
ADPR1 = 1U;
ADPR0 = 1U;
/* Set transition analog block to operation mode */
ADWINR = _08_AD_ADGSPCR_ADHVREFCNT_RW_ENABLE;
```

Current driver code

```
/* Set INTAD low priority */
ADPR1 = 1U;
ADPR0 = 1U;
ADCSR &= (~_0400_AD_LOW_CURRENT_CONVERSION_ENABLE);
/* Set transition analog block to operation mode */
ADWINR = _08_AD_ADGSPCR_ADHVREFCNT_RW_ENABLE;
```

Figure 3-18 Set ADCSR.ADHSC in API R_Config_S12AD0_Create()

3.2.6 Improvement for updating the name of Event Link Controller (ELC) in component tree

Smart Configurator updates the name of Event Link Controller (ELC) in component tree.

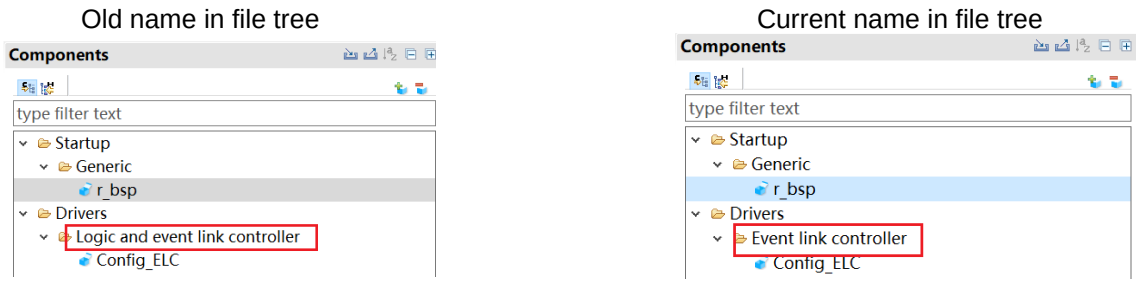


Figure 3-19 the name of Event Link Controller (ELC) in file tree

3.2.7 Improve the specification of input source and output pin in SAU

For supporting new ELCL feature (See 2.3.5 Support new ELCL feature for details), Smart Configurator updates the specification of input source and output pin in SAU.

- SAU CSI specification: When using CSImn as Reception or Transmission/reception, the user can select input source for SCKmn ("Transfer clock mode" should set to "External clock (slave)") and SImn. (mn = 00, 01)

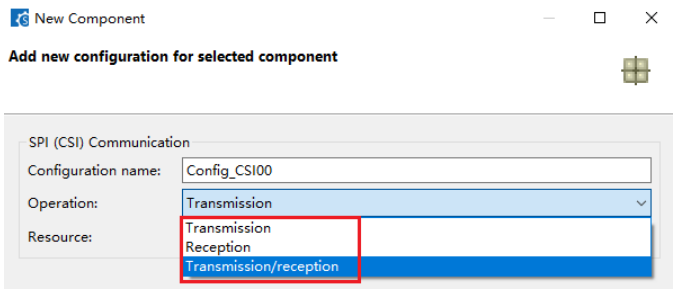


Figure 3-20 Operation selection when adding SAU CSI

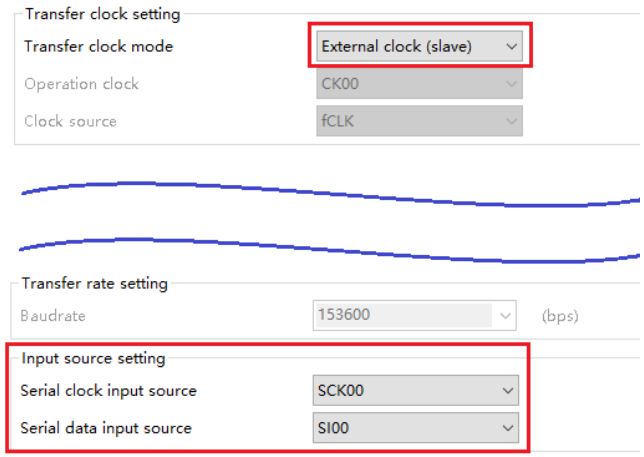


Figure 3-21 "Input source setting" in SAU CSI

When using CSImn as Transmission or Transmission/reception, the user can select whether to output SCKmn ("Transfer clock mode" should set to "Internal clock (master)") and SOmn signal. (mn = 00, 01)

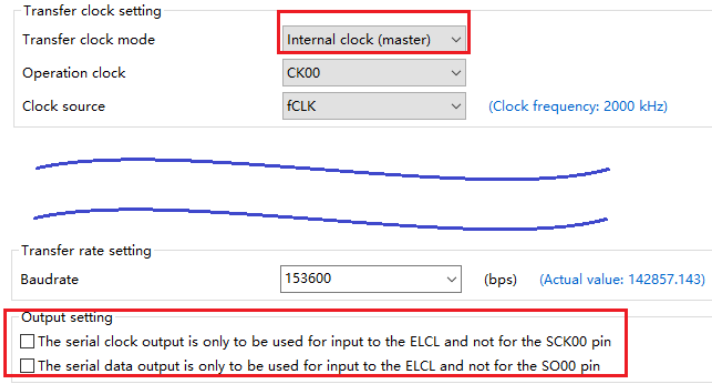


Figure 3-22 "Output setting" in SAU CSI

- SAU UART specification: When using UART0 as Transmission or Transmission/reception, the user can select whether to output TxD0 signal.

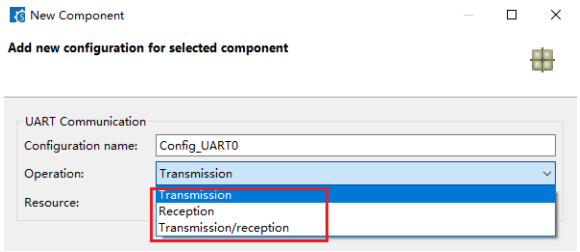


Figure 3-23 Operation selection when adding SAU UART

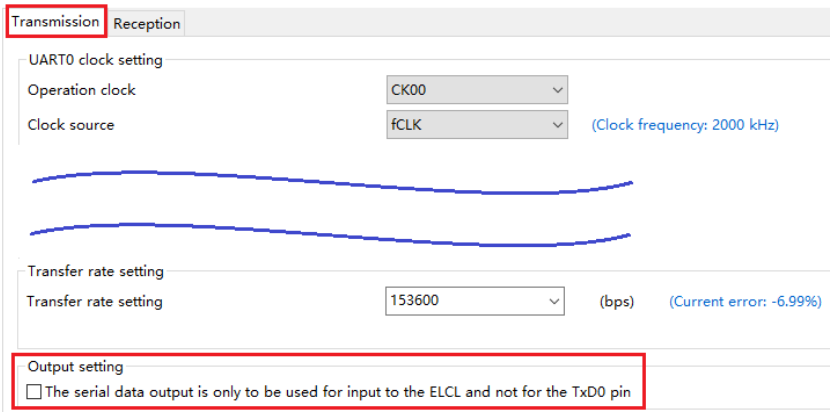


Figure 3-24 "Output setting" in SAU UART

- SAU IIC specification: When using IICmn, the user can select whether to output SCLmn signal. (mn = 00, 01)

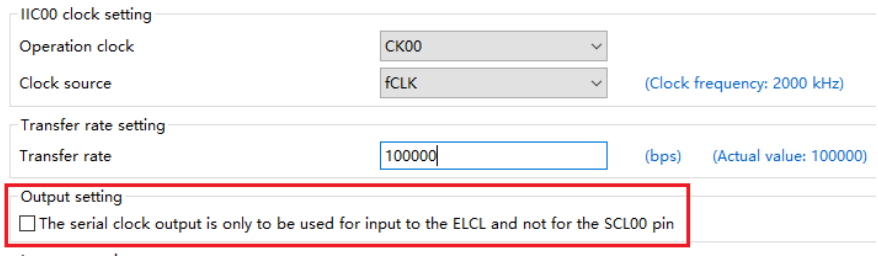


Figure 3-25 "Output setting" in SAU IIC

3.2.8 Improve the specification of output pin in UARTA

For supporting new ELCL feature (See 2.3.5 Support new ELCL feature for details), Smart Configurator updates the specification of output pin in UARTA.

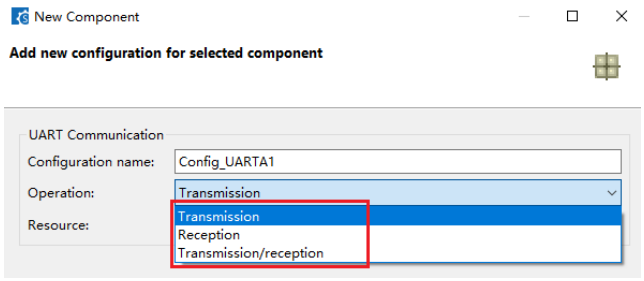
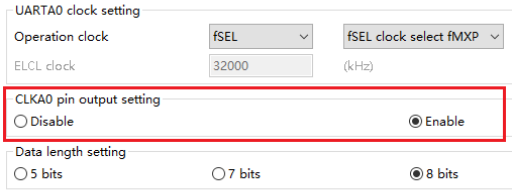


Figure 3-26 Operation selection when adding UARTA

- UARTA0 specification: When using UARTA0, Smart Configurator updates the GUI and driver code.

Old GUI



Current GUI

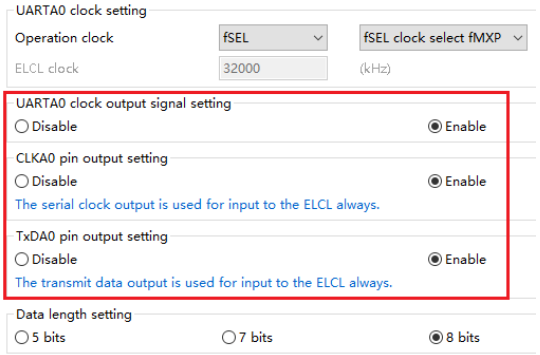


Figure 3-27 UARTA0 GUI

- When using UARTA0 as Transmission or Transmission/reception, Smart Configurator changes the groupbox name from “CLKA0 pin output setting” to “UARTA0 clock output signal setting” and updates the driver code about setting UTA0CK.UTA0OEN.

[Before]

```
void R_Config_UARTA0_Create(void)
{
    ...
    ASIMA00 = _00_UARTA_TRANSFER_END;
    UTA0CK = _80_UARTA_CLKA0_OUTPUT_ENABLE | _10_UARTA_FSEL_SELECT_FMXP | _00_UARTA0_SELECT_FSEL;
    /* Set CLKA0 pin */
    PFOE1 |= 0x20U;
    P8 &= 0xDFU;
    PM8 &= 0xDFU;
    ...
}

void R_Config_UARTA0_Start(void)
{
    volatile uint8_t w_count;

    UARTAEN0 = 1U;
    TXEA0 = 1U;
    ...
}

void R_Config_UARTA0_Stop(void)
{
    TXEA0 = 0U;
    UARTAEN0 = 0U;
}
```

[After]

```
void R_Config_UARTA0_Create(void)
{
    ...
    ASIMA00 = _00_UARTA_TRANSFER_END;
    UTA0CK = _10_UARTA_FSEL_SELECT_FMXP | _00_UARTA0_SELECT_FSEL;
    /* Set CLKA0 pin */
    PFOE1 |= 0x20U;
    P8 &= 0xDFU;
    PM8 &= 0xDFU;
    ...
}

void R_Config_UARTA0_Start(void)
{
    volatile uint8_t w_count;

    UARTAEN0 = 1U;
    UTA0CK |= _80_UARTA_CLKA0_OUTPUT_ENABLE;
    TXEA0 = 1U;
    ...
}

void R_Config_UARTA0_Stop(void)
{
    TXEA0 = 0U;
    UTA0CK &= (uint8_t)~_80_UARTA_CLKA0_OUTPUT_ENABLE;
    UARTAEN0 = 0U;
}
```

Note: UTA0CK.UTA0OEN setting will change in API R_Config_UARTA0_Start() according to GUI setting.

- When using UARTA0 as Transmission or Transmission/reception, Smart Configurator adds the groupbox “CLKA0 pin output setting” and “TxDA0 pin output setting” and the user can select whether to output CLKA0 ("UARTA0 clock output signal setting" should set to "Enable") and TxDA0 signal.

- When using UARTA0 as Reception, Smart Configurator removes the groupbox “CLKA0 pin output setting” and removes the driver code about setting UTA0CK.UTA0OEN.

- UARTA1 specification: When using UARTA1, Smart Configurator updates the GUI and driver code.

Figure 3-28 UARTA1 GUI

- When using UARTA1 as Transmission or Transmission/reception, Smart Configurator changes the groupbox name from “CLKA1 pin output setting” to “UARTA1 clock output signal setting” and updates the driver code about setting UTA1CK.UTA1OEN.

[Before]

```
void R_Config_UARTA1_Create(void)
{
    ...
    UTA0CK |= _10_UARTA_FSEL_SELECT_FMXP;
    UTA1CK = _80_UARTA_CLKA1_OUTPUT_ENABLE | _00_UARTA1_SELECT_FSEL;
    /* Set CLKA1 pin */
    P3 &= 0xFBU;
    PM3 &= 0xFBU;
    ...
}

void R_Config_UARTA1_Start(void)
{
    volatile uint8_t w_count;

    UARTAEN1 = 1U;
    TXEA1 = 1U;
    ...
}

void R_Config_UARTA1_Stop(void)
{
    TXEA1 = 0U;
    UARTAEN1 = 0U;
}
```

[After]

```
void R_Config_UARTA1_Create(void)
{
    ...
    UTA0CK |= _10_UARTA_FSEL_SELECT_FMXP;
    UTA1CK = _00_UARTA1_SELECT_FSEL;
    /* Set CLKA1 pin */
    P3 &= 0xFBU;
    PM3 &= 0xFBU;
    ...
}

/***********************************************************************
* Function Name: R_Config_UARTA1_Start
* Description  : This function starts UARTA1 module operation.
* Arguments    : None
* Return Value : None
***********************************************************************/
void R_Config_UARTA1_Start(void)
{
    volatile uint8_t w_count;

    UARTAEN1 = 1U;
    UTA1CK |= _80_UARTA_CLKA1_OUTPUT_ENABLE;
    TXEA1 = 1U;
    ...
}

/***********************************************************************
* Function Name: R_Config_UARTA1_Stop
* Description  : This function stops UARTA1 module operation.
* Arguments    : None
* Return Value : None
***********************************************************************/
void R_Config_UARTA1_Stop(void)
{
    TXEA1 = 0U;
    UTA1CK &= (uint8_t)~_80_UARTA_CLKA1_OUTPUT_ENABLE;
    UARTAEN1 = 0U;
}
```

Note: UTA1CK.UTA1OEN setting will change in API R_Config_UARTA1_Start() according to GUI setting.

- When using UARTA1 as Reception, Smart Configurator removes the groupbox “CLKA1 pin output setting” and removes the driver code about setting UTA1CK.UTA1OEN.

3.2.9 Improve the specification of output pin in TAU

For supporting new ELCL feature (See 2.3.5 Support new ELCL feature for details), Smart Configurator updates the specification of output pin in TAU. When using TAU - Square Wave Output, Divider Function, One-Shot Pulse Output and PWM Output, the user can select whether to output TO0n signal. (n = 0 - 7)

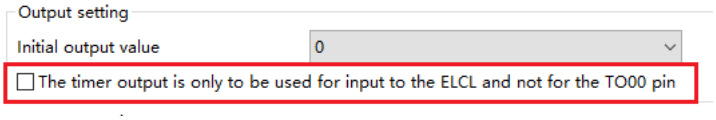


Figure 3-29 "Output setting" in TAU

3.2.10 Improve the specification of input source in PORT

For supporting new ELCL feature (See 2.3.5 Support new ELCL feature for details), Smart Configurator updates the specification of input source in PORT. When using PORT as Out, the user can select input source from ELCL.

Figure 3-30 PORT GUI

4. List of RENESAS TOOL NEWS AND TECHNICAL UPDATE

Below is a list of notifications delivered by RENESAS TOOL NEWS and TECHNICAL UPDATE.

Issue date	Document No.	Description	Applicable MCUs	Fixed version
Oct. 01, 2021	R20TS0757	1. Notes on creating LLVM for Renesas RL78 C/C++ Executable Project 2. Notes on using Port Input buffer function https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rl78	RL78/G23	V1.2.0
Mar. 16, 2022	R20TS0822	1. Notes when build or clean e2 studio Smart Configurator project https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rl78-0	RL78/G23	V1.3.0
Dec. 01, 2022	R20TS0895	1. Notes when changing version of Board Support Program (BSP) or RL78 Software Integration System (SIS) modules https://www.renesas.com/us/en/document/tnn/notes-e-studio-smart-configurator-rl78-plug-smart-configurator-rl78	RL78/G23 RL78/F24 RL78/G15	V1.5.0

5. Points for Limitation

This section describes points for limitation regarding the Smart Configurator for RL78 V1.12.0.

5.1 List of Limitation

Table 5-1 List of Limitation (1/2) ✓: Applicable, -: Not Applicable

No	Description	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	RL78/F25	Remarks
1	Note on extra help document issue	✓	✓	✓	✓	✓	✓	✓	✓	
2	Note on ELCL D flip flop component GUI warning display incorrectly	✓	–	–	–	–	–	–	–	
3	Note on the unsupported setting items for some ELCL components	✓	–	–	–	–	–	–	–	
4	Note on the user code protection feature will only be supported on the files that are generated by the Code Generation component	✓	✓	✓	✓	✓	✓	✓	✓	
5	Note on Flexible Application Accelerator (FAA) component does not support LLVM project	–	–	–	–	–	–	✓	–	
6	Note on not using Flexible Application Accelerator (FAA) component in Mac OS and Linux	–	–	–	–	–	–	✓	–	
7	Note on not using SNOOZE Mode Sequencer (SMS) component in Mac OS and Linux	✓	–	–	–	✓	–	–	–	
8	Note on not correcting the errors in the User's Manual	–	✓	–	✓	–	–	–	–	
9	Note on UI display with High Contrast theme on Linux OS	✓	✓	✓	✓	✓	✓	✓	✓	

Table 5-2 List of Limitation (2/2) ✓: Applicable, -: Not Applicable

No	Description	RL78/F22	Remarks
1	Note on extra help document issue	✓	
2	Note on ELCL D flip flop component GUI warning display incorrectly	–	
3	Note on the unsupported setting items for some ELCL components	–	
4	Note on the user code protection feature will only be supported on the files that are generated by the Code Generation component	✓	
5	Note on Flexible Application Accelerator (FAA) component does not support LLVM project	–	
6	Note on not using Flexible Application Accelerator (FAA) component in Mac OS and Linux	–	
7	Note on not using SNOOZE Mode Sequencer (SMS) component in Mac OS and Linux	–	
8	Note on not correcting the errors in the User's Manual	–	
9	Note on UI display with High Contrast theme on Linux OS	✓	

5.2 Details of Limitation

5.2.1 Note on extra help document issue

For Smart Configurator, there is an extra help “Smart Browser” under “[Help] > [Help Contents]”.
Please ignore it.

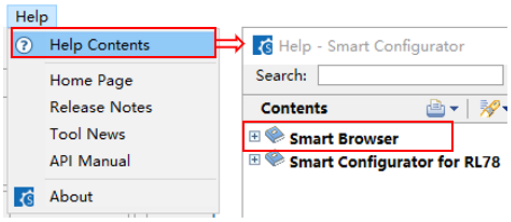


Figure 5-1 Extra help issue

5.2.2 Note on ELCL D flip flop component GUI warning display incorrectly

When selecting the event signal in ELCL D flip flop component, even if the selected signal consists with the hardware specification, there still displays the warning on the GUI.

[Workaround]
Make reference to the hardware manual and set the selectable event signal though warning appeared in GUI, the waring is no impact for the code generation.

The following is example of using flip-flop 0 and flip-flop 1 in ELCL logic cell block L1.

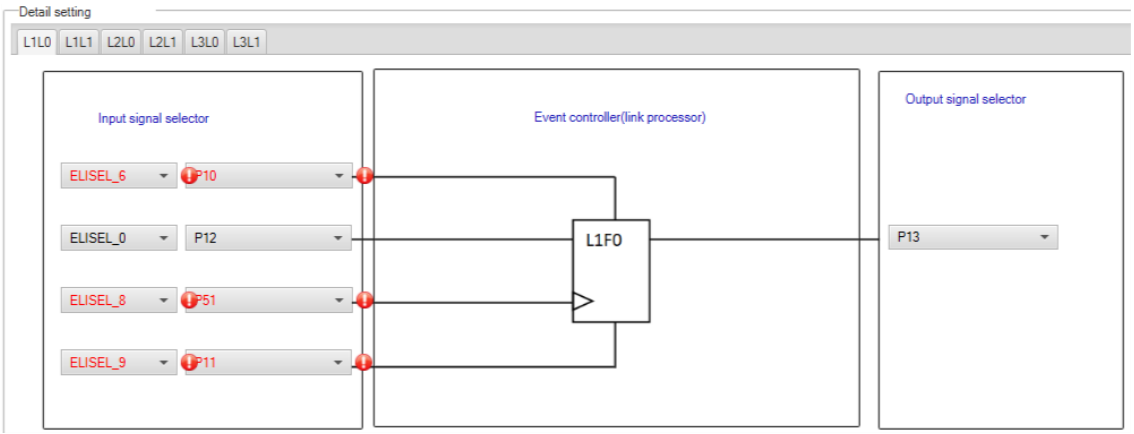


Figure 5-2 The flip-flop 0 in ELCL logic cell block L1 usage example

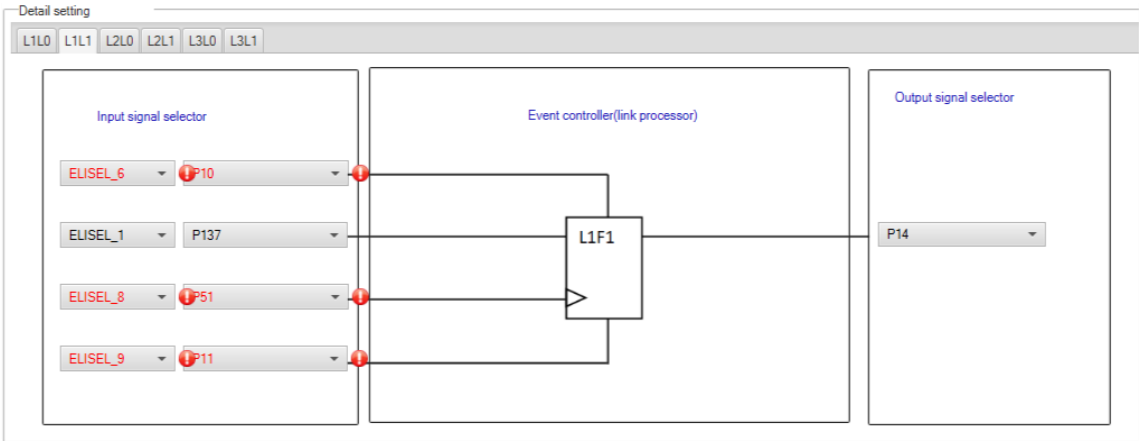


Figure 5-3 The flip-flop 1 in ELCL logic cell block L1 usage example

5.2.3 Note on the unsupported setting items for some ELCL components

In the following ELCL modules, it is not possible to set “no selection (fixed to 0)” as the input signal of the logic cell block and “negative logic output (inverted)” as the output level of the event signal.

- ELCL AND
- ELCL D flip flop
- ELCL EXOR
- ELCL selector
- ELCL Through

[Workaround] None

5.2.4 Note on the user code protection feature will only be supported on the files that are generated by the Code Generation component

The user code protection feature will only be supported on the files that are generated by the Code Generation component. Hence, the user code protection feature is not available for non-Code Generation components.

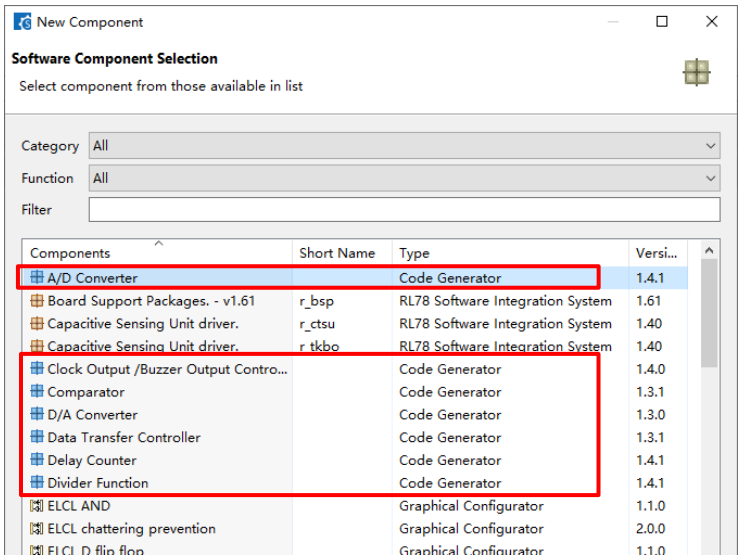


Figure 5-4 Code Generation component in red frame

5.2.5 Note on Flexible Application Accelerator (FAA) component does not support LLVM project

In Smart Configurator for RL78 V1.7.0 or later, Flexible Application Accelerator component was not supported for LLVM project. Though the user can add Flexible Application Accelerator component under LLVM project, but the generated Flexible Application Accelerator source code can’t be built successfully and works for running and debugging.

5.2.6 Note on not using Flexible Application Accelerator (FAA) component in Mac OS and Linux

In Smart Configurator for RL78 V1.10.0 or later, Flexible Application Accelerator component was not supported in Mac OS and Linux. Though the user can add Flexible Application Accelerator component in Mac OS and Linux, but the generated Flexible Application Accelerator source code can’t be built successfully and works for running and debugging.

5.2.7 Note on not using SNOOZE Mode Sequencer (SMS) component in Mac OS and Linux

In Smart Configurator for RL78 V1.10.0 or later, SNOOZE Mode Sequencer component was not supported in Mac OS and Linux. Though the user can add SNOOZE Mode Sequencer component in Mac OS and Linux, but the generated SNOOZE Mode Sequencer source code can't be built successfully and works for running and debugging.

5.2.8 Note on not correcting the errors in the User's Manual

There are some errors in RL78/F23 and RL78/F24 User's Manual (R01UH0944EJ0100). Smart Configurator will correct these errors in next release. Please refer to the document TN-RL*-A0139A/E for details.

5.2.9 Note on UI display with High Contrast theme on Linux OS

When using e² studio with High Contrast theme on Linux OS, some display texts of Smart Configurator can't be seen. To avoid this issue, please use other themes.

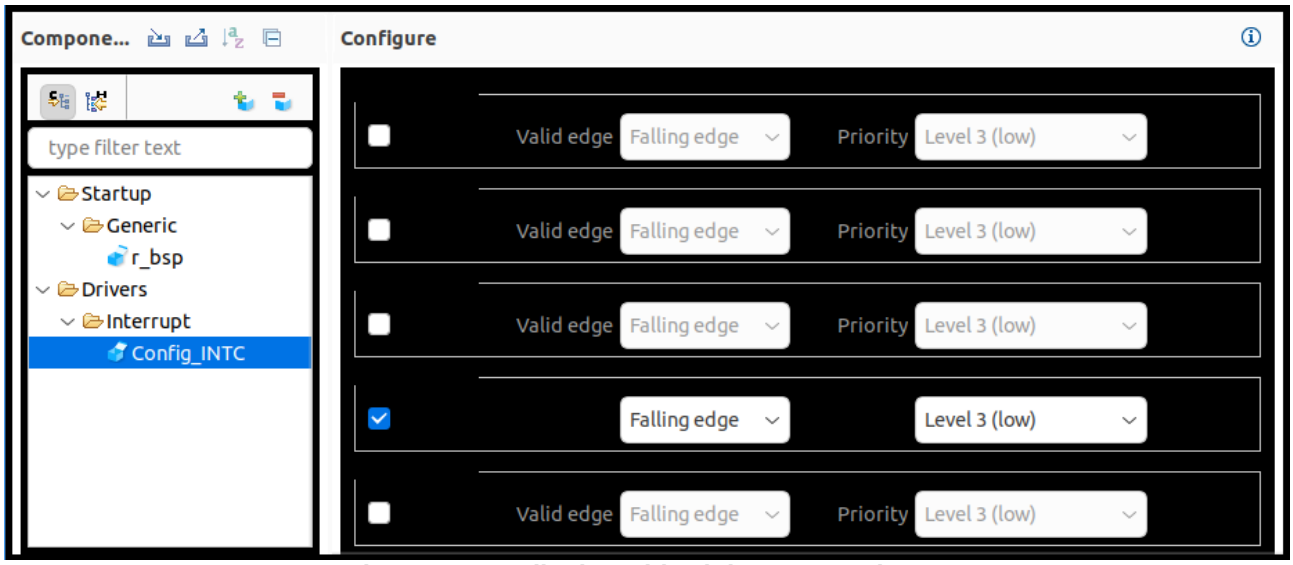


Figure 5-5 UI display with High Contrast theme

6. Points for Caution

This section describes points for caution regarding the Smart Configurator for RL78 V1.12.0.

6.1 List of Caution

Table 6-1 List of Caution (1/2) ✓: Applicable, -: Not Applicable

No	Description	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	RL78/F25	Remarks
1	Note on the build error message such as "section .bss virtual address range overlaps with .dtc_vectortable"	✓	✓	–	✓	✓	–	✓	✓	
2	Note on the installation of the Smart Configurator	✓	✓	✓	✓	✓	✓	✓	✓	
3	Note on using TRDIOA0 for Input capture and TRDIOB0 for Output compare at same time	–	✓	–	–	–	–	✓	✓	
4	Note on pulse width calculation of Timer RD input capture function	–	✓	–	–	–	–	✓	✓	
5	Note on the include path update issue when renaming the component's configuration name	✓	✓	✓	✓	✓	✓	✓	✓	
6	Note on TAU Input Signal High/Low level Measurement components.	✓	✓	✓	✓	✓	✓	✓	✓	
7	Note on CC-RL V1.12 C++ project	✓	✓	✓	✓	✓	✓	✓	✓	
8	Note on browsing "Release Notes" and "Tool News" URL from the help menu	✓	✓	✓	–	–	–	–	–	
9	Note on using the user code protection feature	✓	✓	✓	✓	✓	✓	✓	✓	
10	Note on IAR build error when using SNOOZE Mode Sequencer (SMS) function	✓	–	–	–	–	–	–	–	
11	Note on A/D conversion time setting after performing [Change device] or [Change resource]	✓	✓	✓	✓	✓	✓	✓	✓	
12	Note on changing Hardware Debug Configuration on project generation wizard	✓	✓	✓	✓	✓	✓	✓	✓	
13	Note on Pin Number maybe wrong in [Pins] page when loading project	–	–	–	–	–	–	✓	–	
14	Note on Pin assignment with PIOR maybe wrong in [Pins] page when changing device	✓	✓	✓	✓	✓	✓	✓	✓	

Table 6-2 List of Caution (2/2) ✓: Applicable, -: Not Applicable

No	Description	RL78/F22	Remarks
1	Note on the build error message such as "section .bss virtual address range overlaps with .dtc_vectortable"	✓	
2	Note on the installation of the Smart Configurator	✓	
3	Note on using TRDIOA0 for Input capture and TRDIOB0 for Output compare at same time	✓	
4	Note on pulse width calculation of Timer RD input capture function	✓	
5	Note on the include path update issue when renaming the component's configuration name	✓	
6	Note on TAU Input Signal High/Low level Measurement components.	✓	
7	Note on CC-RL V1.12 C++ project	✓	
8	Note on browsing "Release Notes" and "Tool News" URL from the help menu	-	
9	Note on using the user code protection feature	✓	
10	Note on IAR build error when using SNOOZE Mode Sequencer (SMS) function	-	
11	Note on A/D conversion time setting after performing [Change device] or [Change resource]	✓	
12	Note on changing Hardware Debug Configuration on project generation wizard	✓	
13	Note on Pin Number maybe wrong in [Pins] page when loading project	-	
14	Note on Pin assignment with PIOR maybe wrong in [Pins] page when changing device	✓	

6.2 Details of Caution

6.2.1 Note on the build error message such as "section .bss virtual address range overlaps with .dtc_vectortable"

When the user uses many components and DTC component together, the generated code build might fail due to some section address overlaps.

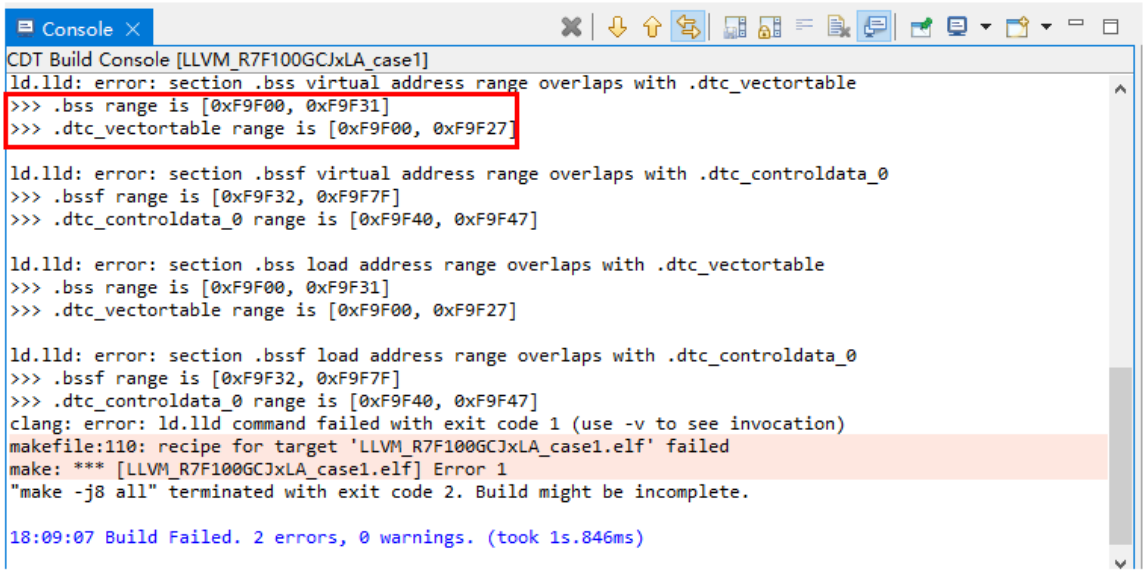


Figure 6-1 Build error message

[Workaround]
The Smart Configurator cannot set ".bss" and ".bssf" section address. So user should consider to modify ".bss" and ".bssf" section address manually in "linker_script.ld" file or change the DTC base address to avoid such section overlap error.

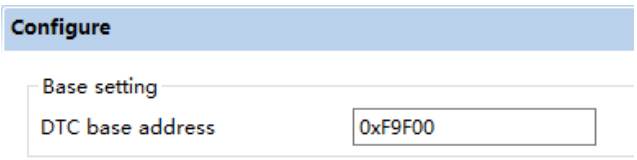


Figure 6-2 DTC base address setting

6.2.2 Note on the installation of the Smart Configurator

Do not set more than 64 characters for the installation directory.
The user might see an error message "The specified path is too long" and will not be able to install Smart Configurator.

6.2.3 Note on using TRDIOA0 for Input capture and TRDIOB0 for Output compare at same time

If the user sets up TRDIOA0 for Input capture and TRDIOB0 for Output compare at the same time. Smart Configurator will output a Peripheral conflict error.
The user can ignore this Smart Configurator error message and use these two functions at the same time.

6.2.4 Note on pulse width calculation of Timer RD input capture function

The pulse width calculation code is with the assumption that the counter is not cleared between two interrupts occurrence, except the input pulse width which is selected as counter clear trigger on GUI.
For example, when "Clear by TRDGRA*n* input capture" is selected, only TRDIOA*n* pulse width calculation handle counter clear, other input pulse width calculation doesn't handle counter clear.

Figure 6-3 Counter clear setting in Input capture function

6.2.5 Note on the include path update issue when renaming the component's configuration name

When renaming the added component's configuration in e2 studio Smart Configurator project that has self-defined include path setting for any folder or file, include path setting for that folder or file will keep the old name setting after code generation. This will cause build error when compiling the newly generated codes so please manually update the include path.

The folder or file which has self-defined include path setting can be recognized by checking the overlay icon ( ) on that folder or file. Below is an example on how to handle the include path update after renaming Compare Match Timer component configuration.

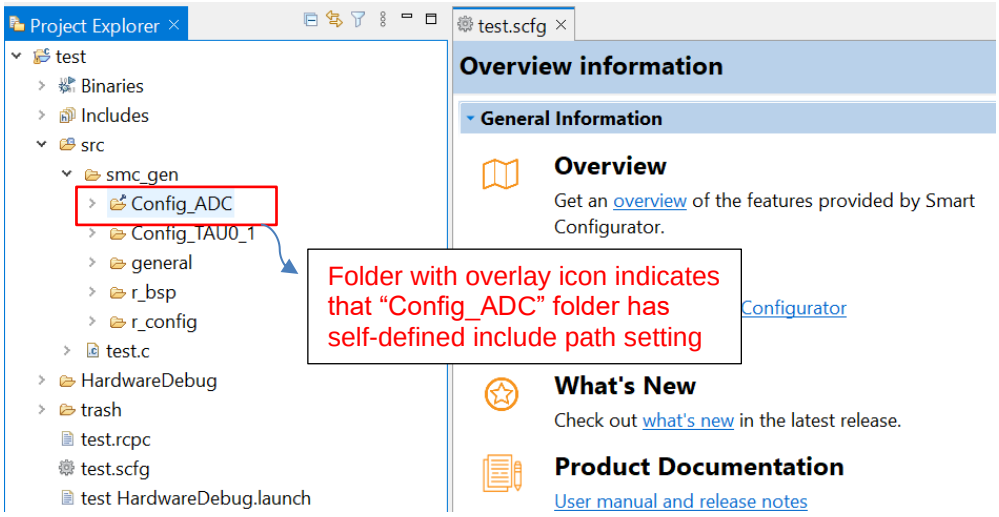


Figure 6-4 Interval Timer component configuration before renaming

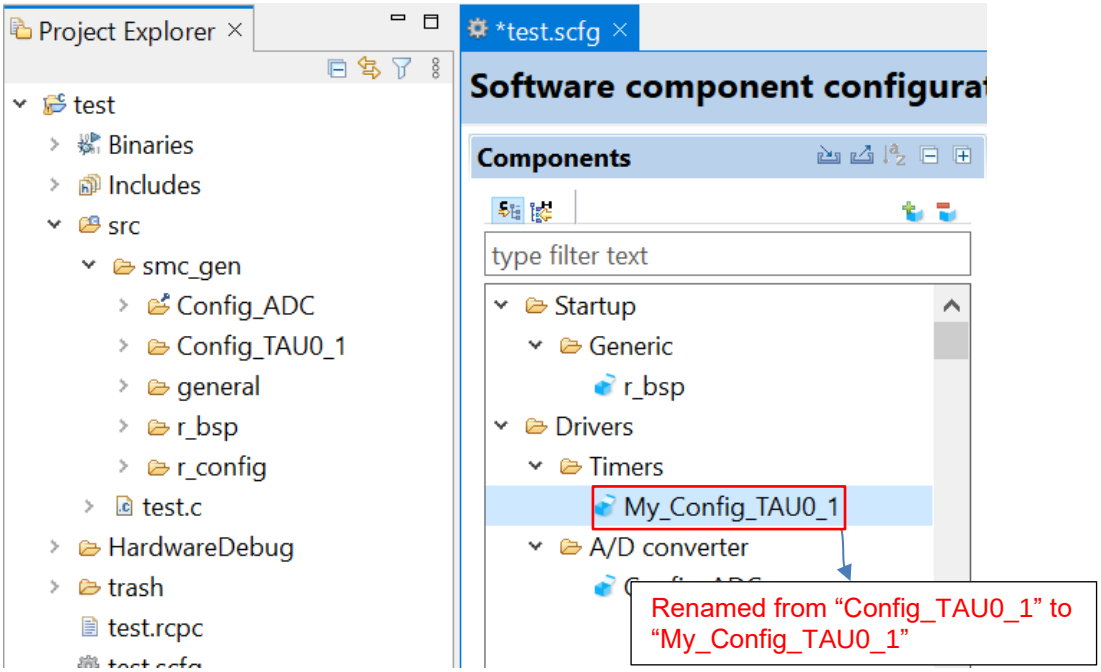


Figure 6-5 The Interval Timer component configuration after renaming

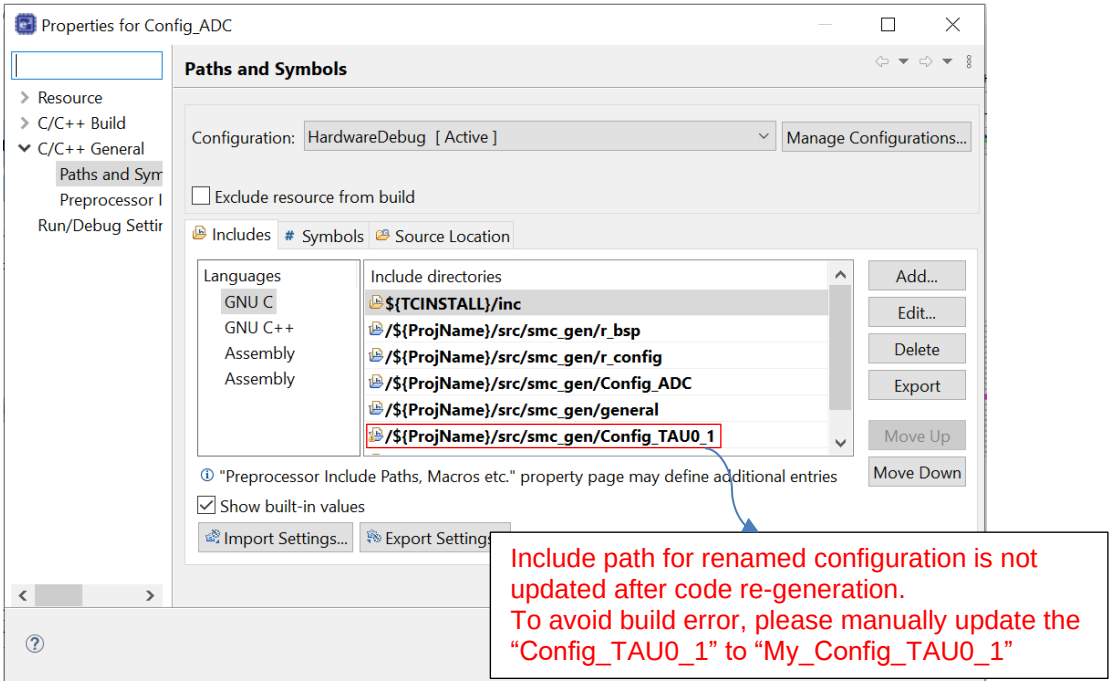


Figure 6-6 Include path setting for the "Config_ADC" configuration

6.2.6 Note on TAU Input Signal High/Low level Measurement component

When using TAU Input Signal High/Low level Measurement component, after used noise filter function for TImn input pulse, please make sure the High/Low level width min value needs to be greater than two times the minimum value prompted on the UI.
For example, the High/Low level width min value is 0.032us (min value), when use noise filter function, the width min value should be 0.064us.

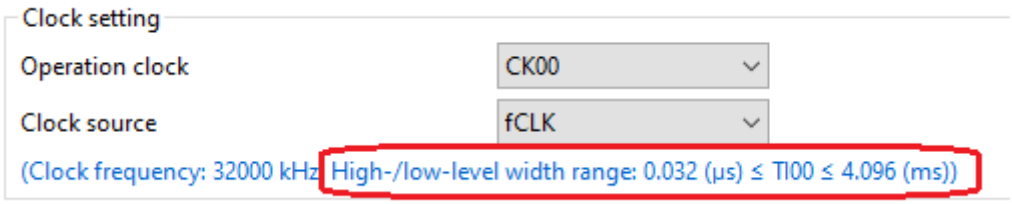


Figure 6-7 High/Low level width min value

6.2.7 Note on CC-RL V1.12 C++ project

In CC-RL V1.12 or later C++ project, there are some dummy issues such as “EI()” in editor. However this is editor specification and does not affect the program operation. Please ignore it.

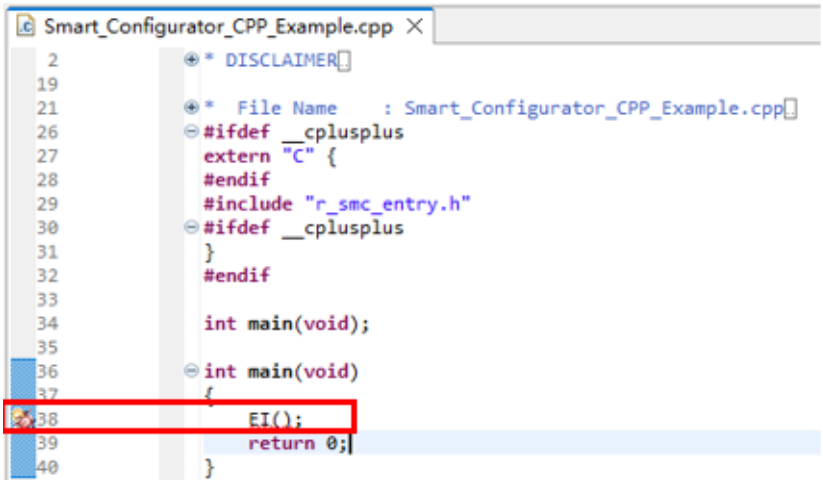


Figure 6-8 CODAN issue in CC-RL V1.12 C++ project

6.2.8 Note on browsing "Release Notes" and "Tool News" URL from the help menu

For Smart Configurator for RL78 V1.4.0 or before version, "Release Notes" and "Tools News" in the help menu cannot access the correct URL. This issue has been fixed from this version.
Please access the URL below directly for Smart Configurator for RL78 V1.4.0 or before version.
Release Notes: https://www.renesas.com/rl78-smart-configurator-release-note
Tool News: https://www.renesas.com/rl78-smart-configurator-tn-notes

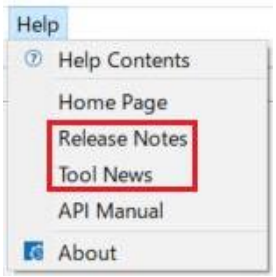


Figure 6-9 Release Notes and Tool News in Smart Configurators

6.2.9 Note on using the user code protection feature

From Smart Configurator for RL78 V1.5.0 onwards, the user code protection feature will be supported for all Code Generation components. Please use the following specific tags to add user code when using the user code protection feature. If the specific tags do not match exactly, inserted user code will not be protected after the code generation.

```
/* Start user code */
User code can be added between the specific tags
/* End user code */
```

6.2.10 Note on IAR build error when using SNOOZE Mode Sequencer (SMS) component

When using SNOOZE Mode Sequencer (SMS) component, if the following build error is met in IAR Embedded workbench, please check the build order setting in project [Options…] -> [Custom Build] page.

1) When using IAR Embedded workbench V5.10, select "Run before compiling/assembling" (refer to Figure 6-11)
2) When using IAR Embedded workbench V4.21, make “Run this tool before all other tools” checked (refer to Figure 6-12)

The above setting can eliminate this build error.

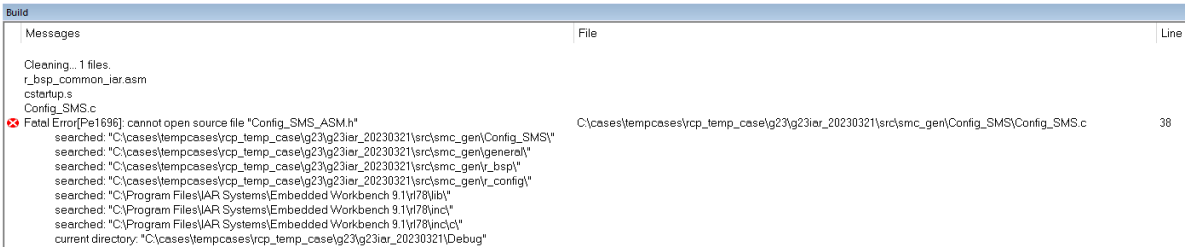


Figure 6-10 IAR build error

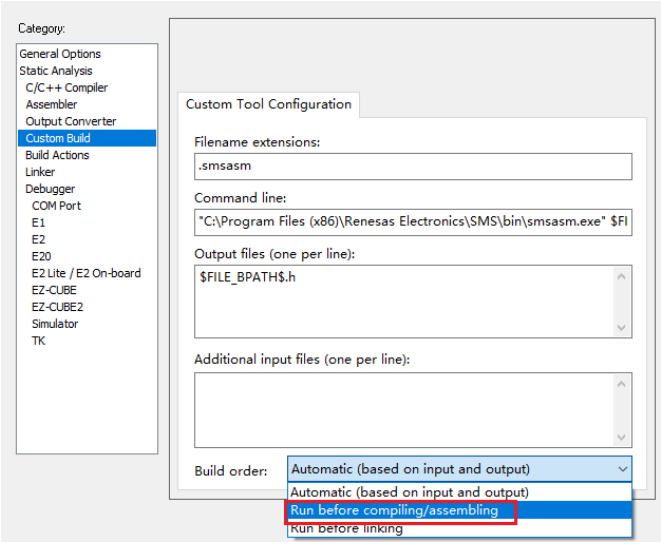


Figure 6-11 "Build order" setting of IAR Embedded workbench V5.10

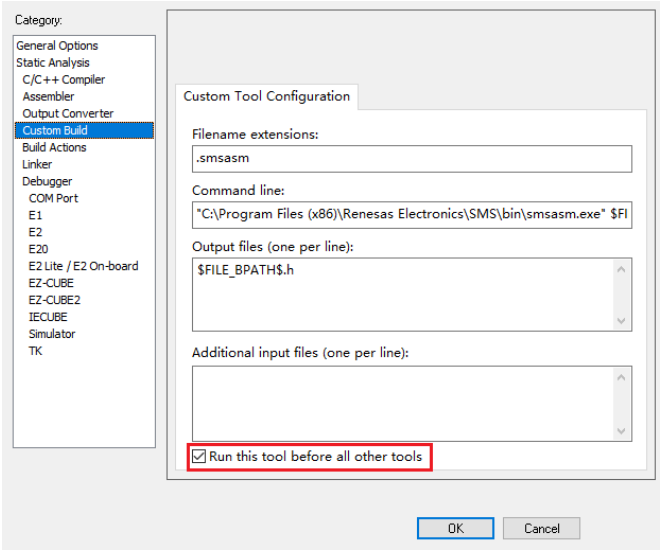


Figure 6-12 Custom build setting of IAR Embedded workbench V4.21

6.2.11 Note on A/D conversion time setting after performing [Change device] or [Change resource]

After performing [Change device] (for example, change from RL78/G23 to RL78/G24), the A/D conversion time setting can't be kept. The user should take note to reconfirm the conversion time setting as he wants.

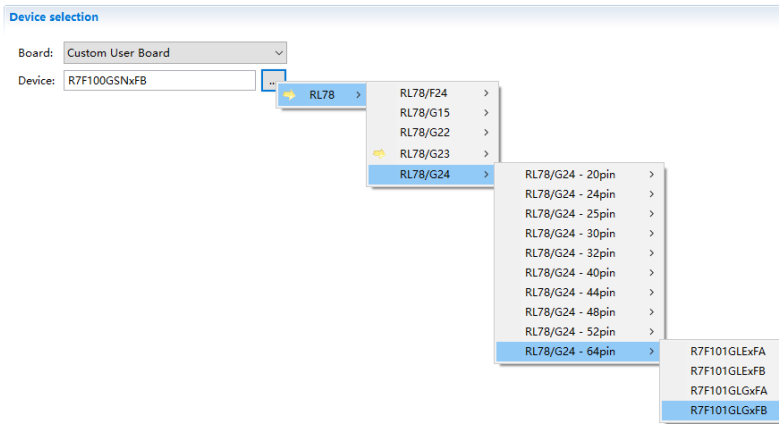


Figure 6-13 [Change device] operation

Figure 6-14 A/D conversion time setting

When changing resource, for example from RL78/G24 normal A/D and RL78/G24 advanced A/D, the A/D conversion time can't be kept.

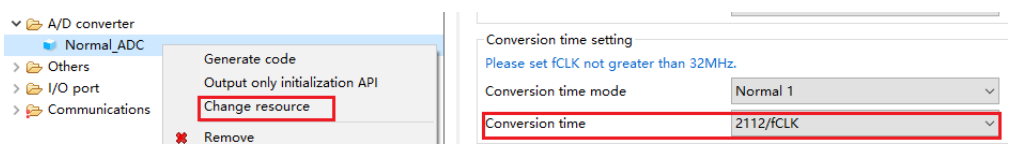


Figure 6-15 [Change resource] operation

6.2.12 Note on changing Hardware Debug Configuration on project generation wizard

When a target board (except custom) is selected during creating a new project, please don't change the Hardware Debug Configuration manually. The reason is that the Hardware Debug Configuration has be decided by target board automatically. The user setting can't be reflected into Smart Configurator.

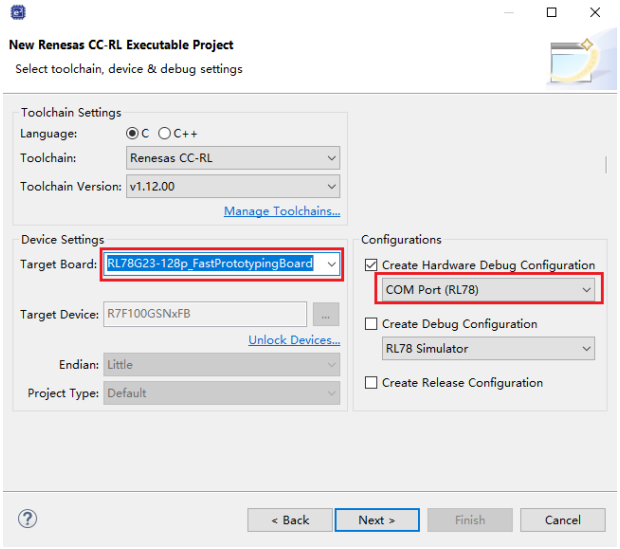


Figure 6-16 Select a target board when creating a project in e2 studio

6.2.13 Note on Pin Number maybe wrong in [Pins] page when loading project

The Pin Number maybe wrong for SCL00, SDA00, SI00, SO00, SCK00 when the user loads a 48/52/64pin project. The user needs to re-assign these pins manually.

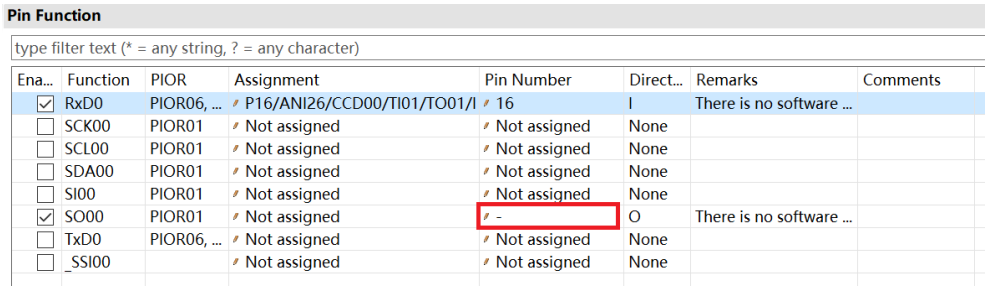


Figure 6-17 Pin Number maybe wrong in [Pins] page

6.2.14 Note on Pin assignment with PIOR maybe wrong in [Pins] page when changing device

After performing [Change device] (for example, change from RL78/G23 to RL78/F24), the Pin assignment with PIOR may change according to PIOR setting automatically. When it has pin conflict, Smart Configurator will output pin conflict message and doesn't change pin assignment automatically. The user needs to re-assign these pins manually.

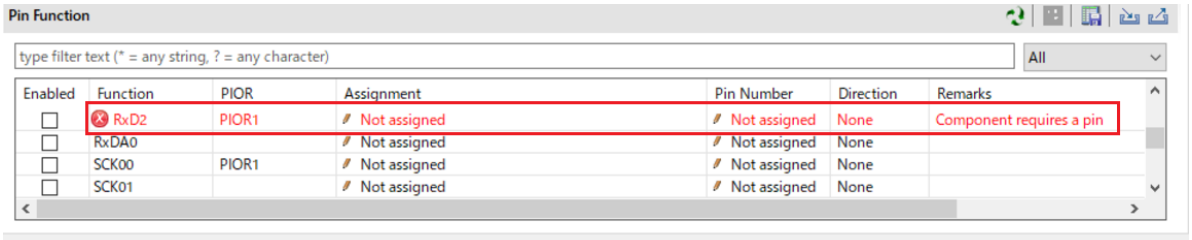


Figure 6-18 Pin assignment with PIOR maybe wrong in [Pins] page

Revision History

Rev.	Section	Description
1.00	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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