

## Smart Configurator for RL78 Plug-in in e<sup>2</sup> studio 2025-01 Smart Configurator for RL78 V1.12.0

## Release Note

## Introduction

Thank you for using the Smart Configurator for RL78.

This document describes the restrictions and points for caution. Read this document before using the product.

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## 1. Introduction

Smart Configurator is a utility for combining software to meet your needs. It supports the following three functions related to the embedding of Renesas drivers in your systems: importing middleware, generating driver code, and setting pins.

Smart Configurator for RL78 V1.12.0 is equivalent to Smart Configurator for RL78 Plug-in in e<sup>2</sup> studio 2025-01.

## 1.1 System Requirements

The operating environment is as follows.

## 1.1.1 Windows PC

 System: x64/x86 based processor Windows® 11

Windows® 10 (64-bit version)

- Memory capacity: We recommend 4 GB or more.
- Capacity of hard disk: At least 300 MB of free space.
- Display: Graphics resolution should be at least 1024 x 768, and the mode should display at least 65,536 colors.
- Processor: 1 GHz or higher (must support hyper-threading, multi-core CPUs)

## 1.1.2 Linux PC

Smart Configurator for RL78 plug-in in e<sup>2</sup> studio 2023-01 or later is supported on Linux OS.

• System: x64 based processor, 2 GHz or faster (with multicore CPUs)

Ubuntu 22.04 LTS Desktop (64-bit version) Ubuntu 20.04 LTS Desktop (64-bit version)

- Memory capacity: We recommend 2 GB or more.
- Capacity of hard disk: At least 2 GB of free space.

### 1.1.3 Mac OS

Smart Configurator for RL78 plug-in in e<sup>2</sup> studio 2024-04 or later is supported on Mac OS.

• System: 1.8 GHz or faster 64-bit processor. Dual-core or better recommended. Apple Silicon (arm64) processors are only supported.

MacOS 13 (Ventura)

- Memory capacity: 4 GB of RAM; 8 GB of RAM recommended.
- Capacity of hard disk: At least 2 GB of free space.
- A screen resolution of 1280 x 800 or higher.

Note: Only LLVM is available for Mac OS.



## 1.1.4 Development Environments

- Renesas Electronics Compiler for RL78 [CC-RL] V1.14 or later (Windows PC)
- LLVM for Renesas RL78 17.0.1.202409 or later (Windows PC, Linux PC, Mac OS)
- IAR Embedded Workbench for Renesas RL78 V5.10.3 or later (Windows PC)
- SMS Assembler V1.00.00 or later (Windows PC)
- FAA Assembler V1.04.02 or later (Windows PC)
- CS+ for CC V8.13.00 Note1 or later (Windows PC)

Note:

1.Smart Configurator for RL78 V1.12.0 has been evaluated in the CS+ for CC V8.13.00 environment. When using Smart Configurator for RL78 V1.11.0 or lower, please refer to Release Note (R20UT5533EC0100) about the target version of CS+ for CC.



## 2. Support List

## 2.1 Support Devices List

Below is a list of devices supported by the Smart Configurator for RL78 V1.12.0.

Table 2-1 Support Devi	ces (1/2)	Du la sura
Group	PIN	Device name
PI 78/C23 Group	30nin	
(P011 H0896E 10120)	Supin	R7F100GAFX3F, R7F100GAGX3F, R7F100GAIX3F, R7F100GAJX3F
(101010030230120)	32pin	R7E100GBEVEP R7E100GBGVEP R7E100GBHVEP R7E100GBIVEP
	36nin	RZE100GCEVI A RZE100GCGVI A RZE100GCHVI A RZE100GC IVI A
	40pin	R7E100GEEVNP R7E100GEGVNP R7E100GEHVNP R7E100GE VNP
	торіп	R7E100GEEVEP R7E100GEGVEP R7E100GEHVEP R7E100GE VEP
	44pin	R7E100GEKxEP_R7E100GELxEP_R7E100GENxEP
		R7E100GGEVEB R7E100GGGVEB R7E100GGHVEB R7E100GG VEB
		R7E100GGKxEB R7E100GGLxEB R7E100GGNxEB R7E100GGExNP
	48pin	R7F100GGGxNP, R7F100GGHxNP, R7F100GGJxNP, R7F100GGKxNP,
		R7F100GGLxNP, R7F100GGNxNP
	=0 ·	R7F100GJFxFA, R7F100GJGxFA, R7F100GJHxFA, R7F100GJJxFA,
	52pin	R7F100GJKxFA, R7F100GJLxFA, R7F100GJNxFA
		R7F100GLFxFA, R7F100GLGxFA, R7F100GLHxFA, R7F100GLJxFA,
		R7F100GLKxFA, R7F100GLLxFA, R7F100GLNxFA, R7F100GLFxFB,
	Gánin	R7F100GLGxFB, R7F100GLHxFB, R7F100GLJxFB, R7F100GLKxFB,
	64pin	R7F100GLLxFB, R7F100GLNxFB, R7F100GLFxLA, R7F100GLGxLA,
		R7F100GLHxLA, R7F100GLJxLA, R7F100GLKxLA, R7F100GLLxLA,
		R7F100GLNxLA
		R7F100GMGxFA, R7F100GMHxFA, R7F100GMJxFA, R7F100GMKxFA,
	80pin	R7F100GMLxFA, R7F100GMNxFA, R7F100GMGxFB, R7F100GMHxFB,
		R7F100GMJxFB, R7F100GMKxFB, R7F100GMLxFB, R7F100GMNxFB
	400 .	R7F100GPGxFB, R7F100GPHxFB, R7F100GPJxFB, R7F100GPKxFB,
	100pin	R7F100GPLxFB, R7F100GPNxFB, R7F100GPGxFA, R7F100GPHxFA,
	400 .	R/F100GPJXFA, R/F100GPKXFA, R/F100GPLXFA, R/F100GPNXFA
	128pin	R/F100GSJXFB, R/F100GSKXFB, R/F100GSLXFB, R/F100GSIXFB
RL78/F24 Group	32pin	
(R010H0944EJ0100)	48pin	
	64pin	R/F124FLJ3XFB, R/F124FLJ4XFB, R/F124FLJ5XFB
	80pin	
	100pin	R/F124FPJ3XFB, R/F124FPJ4XFB, R/F124FPJ5XFB
(B01) H00505 (0100)	8pin 40min	R5F12008XNS, R5F12007XNS, R5F12008XSN
(R010H0959EJ0100)	10pin	R5F12018XSP, R5F12017XSP
	16pin	R5F12048XNA, R5F12047XNA, R5F12048XSP, R5F12047XSP
	20pin	R5F12068X5P, R5F12067X5P
(B01) H0044E 10100	32pin	R/F123FBG3XNP, R/F123FBG4XNP, R/F123FBG5XNP
(KUTUHU944EJUTUU)	40pin 64pin	
	04pin	
	00pin 10pin	
(B01) H0078E 10100)	10pin 20pin	
(RUTUHU978EJUTUU)	20pin	
	24pin 25pin	
	20pin	
	30pin 22pin	
	32pin 26pin	
	30pin 40pin	
	400111 440in	
	44010 490in	
1	чоріп	TATE TOZOGENED, RAFTOZOGENNE, RAFTOZOGONED, RAFTOZOGONNE

## Table 2-1 Support Devices (1/2)



Group	PIN	Device name
(HW Manual number)		
RL78/G24 Group	20pin	R7F101G6GxSP, R7F101G6ExSP
(R01UH0961EJ0100)	24pin	R7F101G7GxNP, R7F101G7ExNP
	25pin	R7F101G8GxLA, R7F101G8ExLA
	30pin	R7F101GAGxSP, R7F101GAExSP
	32pin	R7F101GBGxNP, R7F101GBExNP, R7F101GBGxFP, R7F101GBExFP
	40pin	R7F101GEGxNP, R7F101GEExNP
	44pin	R7F101GFGxFP, R7F101GFExFP
	48pin	R7F101GGGxFB, R7F101GGExFB, R7F101GGGxNP, R7F101GGExNP
	52pin	R7F101GJGxFA, R7F101GJExFA
	64pin	R7F101GLGxFA, R7F101GLGxFB, R7F101GLExFA, R7F101GLExFB
RL78/G16 Group	10pin	R5F1211AxSP, R5F1211CxSP
(R01UH0980EJ0100)	16pin	R5F1214AxNA, R5F1214AxSP, R5F1214CxNA, R5F1214CxSP
	20pin	R5F1216AxSP, R5F1216CxSP
	24pin	R5F1217AxNA, R5F1217CxNA
	32pin	R5F121BAxFP, R5F121BAxNA, R5F121BCxFP, R5F121BCxNA
RL78/F25 Group	48pin	R7F125FGL3xFB, R7F125FGL4xFB
(R01UH1061EJ0050)	64pin	R7F125FLL3xFB, R7F125FLL4xFB
	80pin	R7F125FML3xFB, R7F125FML4xFB
	100pin	R7F125FPL3xFB, R7F125FPL4xFB
RL78/F22 Group	24pin	R7F122F7G3xNP, R7F122F7G4xNP
(R01UH1061EJ0050)	32pin	R7F122FBG3xNP, R7F122FBG4xNP
	48pin	R7F122FGG3xFB, R7F122FGG4xFB



## 2.2 Support Components List

Below is a list of Components supported by the Smart Configurator for RL78 V1.12.0.

## Table 2-3 Support Components (1/2)

✓: Support, -: Non-support

No	Components	Mode	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	RL78/F25	Remarks
1	12 Bit A/D Single Scan	-	-	1	-	1	-	-	-	<	
2	12 Bit A/D Continuous Scan	-	-	1	-	$\checkmark$	-	-	-	1	
3	12 Bit A/D Group Scan	-	-	1	-	1	-	-	-	1	
4	A/D Converter	Normal mode	1	-	1	-	1	1	1	-	Only RL78/G24 A/D
		Advanced mode	-	-	-	-	-	-	1	-	converter has mode selection GUI. For other devices, the default mode is "Normal mode" and no GUI is provided for mode selection.
5	Clock Output/Buzzer Output Controller	-	1	~	~	1	1	1	1	~	
6	Comparator	-	$\checkmark$	✓	✓	-	-	1	✓	✓	
7	D/A Converter	-	$\checkmark$	✓	-	-	-	-	✓	✓	
8	Data Transfer Controller	-	$\checkmark$	1	-	$\checkmark$	1	-	1	1	
9	Delay Counter	-	$\checkmark$	✓	✓	$\checkmark$	✓	1	✓	✓	
10	Divider Function	-	$\checkmark$	✓	1	$\checkmark$	✓	1	✓	✓	
11	Event Link Controller	-	-	✓	-	-	✓	-	✓	✓	
12	External Event Counter	-	$\checkmark$	1	1	$\checkmark$	1	1	1	1	
13	IIC Communication (Master mode)	-	1	~	1	1	~	1	~	1	
14	IIC Communication (Slave mode)	-	1	~	1	1	~	~	~	1	
15	Input Capture Function	-	-	✓	-	<	-	-	✓	✓	
16	Input Pulse Interval/Period Measurement	-	1	~	1	1	~	~	~	1	
17	Input Signal High-/Low- Level Width Measurement	-	1	~	1	1	~	1	~	1	
18	Interrupt Controller	-	✓	1	1	1	1	1	1	1	
19	Interval Timer	8 bit count mode	✓	1	✓	1	1	1	1	1	
		12 bit count mode	-	-	1	-	-	1	-	-	
		16 bit count mode	✓	1	✓	1	1	1	1	1	
		16 bit capture mode	✓	-	-	-	<	-	<	-	
		32 bit count mode	✓	-	-	-	✓	-	✓	I	
20	Key Interrupt	-	✓	<	-	✓	<	-	<	<	
21	One-Shot Pulse Output	One-Shot Pulse Output	✓	1	1	1	1	1	1	1	
		Two-Channel Input with One- Shot Pulse Output	-	-	1	-	-	1	-	-	
22	Output Compare Function	-	-	1	-	1	-	-	1	1	
23	Ports	-	✓	1	1	1	1	1	1	✓	
24	PWM Option Unit A		-	1	_	$\checkmark$	-	-	1	✓	
25	DALI Communication (Control devices)	-	-	-	-	-	-	-	1	-	
26	DALI Communication	-	_	_	_	_	_	_	1	_	
07	(Control gear)						<u> </u>		Ľ	-	
27	Real-Time Clock	F	✓	✓		✓	✓	✓	✓	<ul> <li>Image: A start of the start of</li></ul>	



## Release Note

## Table 2-4 Support Components (2/2)

✓: Support, -: Non-support

			<b>I</b>	1	1	1	1	1	<b>I</b>		
No	Components	Mode		RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	RL78/F25	Remarks
28	PWM Output	PWM Mode	1	1	1	1	1	1	1	1	
		PWM3 Mode	_	1	-	1	_	_	./	· /	
		Extended PWM Mode	_	· /	-	/	_	-			
		PWM2 Mode	_	-	-	-	_	_	· /	-	
		Timer KB3 PWM Output Gate									
		Mode	_	-	-	_	_	_	~	-	
		Standalone Mode (Period controlled by the TKBCRn0 register)	-	_	-	-	_	_	~	-	
		Standalone Mode (Period controlled by external trigger input)	_	-	-	_	_	_	~	-	
		Simultaneous Start/Stop Mode (Period controlled by the TKBCRn0 register)	-	_	-	-	-	-	~	-	
		Simultaneous Start/Stop Mode (Period controlled by external trigger input)	-	-	-	-	-	-	~	-	
		Simultaneous Start/Clear Mode (Period controlled by master)	_	_	-	-	-	-	~	-	
		Interleaved PFC Output Mode	-	-	-	-	-	-	✓	-	
29	Remote Control Signal Receiver	-	1	-	-	-	-	-	-	-	
30	SNOOZE Mode Sequencer	-	~	í –	-	-	$\checkmark$	-	-	-	
31	SPI (CSI) Communication	Transmission	-	1	✓	1	✓	1	1	✓	
		Reception	~		1	1	1	1	1	1	
		Transmission/reception	-	1	1	1	✓	✓	1	1	
32	Square Wave Output		~		~	~	~	~	~	~	
33	Three-phase PWM Output	Reset Synchronous PWM Mode	-	1	-	1	-	1	1	✓	
		Complementary PWM Mode	-	1	-	1	-	1	1	1	
		Extended Complementary PWM Mode	-	1	-	1	-	1	1	✓	
34	UART Communication	Iransmission	~	1	~	1	✓	~	~	~	
		Reception	<ul> <li></li> </ul>	<ul> <li>Image: A start of the start of</li></ul>	✓	1	✓	<ul> <li>Image: A start of the start of</li></ul>	✓	✓	
05		I ransmission/reception	✓ ✓	<ul> <li></li> <li></li> </ul>	~	✓ ✓	✓ ✓	~	✓ ✓	<ul> <li></li> </ul>	
35	Voltage Detector	-	✓ ✓	✓ ✓	-	✓ ✓	✓ ✓	-	✓ ✓	✓ ✓	
30	Watchdog Timer	-	~	~	~	~	~	~	~	~	To upo El Cl. modulos of
37	Controller	-	1	-	-	-	-	-	-	-	fixed function, need download in Smart Configurator RL78.
38	Phase Counting Mode	-	_		-				1	-	
39	Programmable Gain Amplifier		-	-	-	-	-	-	1	-	
40	Flexible Application Accelerator	-	-	-	-	-	-	-	~	-	



Release Note

Table 2-5	Support Components	(1/2)
-----------	--------------------	-------

✓: Support, -: Non-support

No	Components	Mode	RL78/F22	Remarks
1	12 Bit A/D Single Scan	-	✓	
2	12 Bit A/D Continuous Scan	-	1	
3	12 Bit A/D Group Scan	-	✓	
4	A/D Converter	Normal mode Advanced mode	-	Only RL78/G24 A/D converter has mode selection GUI. For other devices, the default mode is "Normal mode" and no GUI is provided for mode selection.
5	Clock Output/Buzzer Output Controller	-	$\checkmark$	
6	Comparator	-	-	
7	D/A Converter	-	-	
8	Data Transfer Controller	-	$\checkmark$	
9	Delay Counter	-	✓	
10	Divider Function	-	✓	
11	Event Link Controller	-	-	
12	External Event Counter	-	$\checkmark$	
13	IIC Communication (Master mode)	-	✓	
14	IIC Communication (Slave mode)	-	$\checkmark$	
15	Input Capture Function	-	✓	
16	Input Pulse Interval/Period Measurement	-	1	
17	Input Signal High-/Low-Level Width Measurement	-	1	
18	Interrupt Controller	-	✓	
19	Interval Timer	8 bit count mode	✓	
		12 bit count mode	-	
		16 bit count mode	$\checkmark$	
		16 bit capture mode	-	
		32 bit count mode	-	
20	Key Interrupt	-	✓	
21	One-Shot Pulse Output	One-Shot Pulse Output	✓	
		Two-Channel Input with One- Shot Pulse Output	-	
22	Output Compare Function	-	✓	
23	Ports	-	$\checkmark$	
24	PWM Option Unit A	-	$\checkmark$	
25	DALI Communication (Control devices)	-	-	
26	DALI Communication (Control gear)	-	-	
27	Real-Time Clock	-	1	



**Release Note** 

## Table 2-6 Support Components (2/2)

✓ : Support, -: Non-support

No	Components	Mode	RL78/F22	Remarks
28	PWM Output	PWM Mode	1	
		PWM3 Mode	1	
		Extended PWM Mode	1	
		PWM2 Mode	-	
		Timer KB3 PWM Output Gate Mode	-	
		Standalone Mode (Period controlled by the TKBCRn0 register)	I	
		Standalone Mode (Period controlled by external trigger input)	I	
		Simultaneous Start/Stop Mode (Period controlled by the TKBCRn0 register)	-	
		Simultaneous Start/Stop Mode (Period controlled by external trigger input)	-	
		Simultaneous Start/Clear Mode (Period controlled by master)	-	
		Interleaved PFC Output Mode	-	
29	Remote Control Signal Receiver	-	-	
30	SNOOZE Mode Sequencer	-	-	
31	SPI (CSI) Communication		✓ ✓	
			<b>/</b>	
	Original Maria Original	I ransmission/reception	<i>✓</i>	
32	Square wave Output	- Deset Suzebrezeus D\\/\\ Mada	✓ ✓	
33	Inree-phase PWW Output	Reset Synchronous PWW Mode	✓ ✓	
		Complementary PWW Wode	~	
		Mode	1	
34	UART Communication	Transmission	1	
		Reception	1	
		Transmission/reception	1	
35	Voltage Detector	-	1	
36	Watchdog Timer	-	✓	
37	Logic & Event Link Controller	-	-	To use ELCL modules of fixed function, need download in Smart Configurator RL78.
38	Phase Counting Mode	-	-	
39	Programmable Gain Amplifier	-	-	
40	Flexible Application Accelerator	-	-	



## 2.3 New support

## 2.3.1 BSP (Board Support Package) revision update

BSP rev1.80 is supported and will be added as default BSP when creating Smart Configurator project.

## 2.3.2 Support RL78/F22 devices

See 2.1 Support Devices List for details on supported packages.

## 2.3.3 Support CMake generation for Smart Configurator with Visual Studio Code

From Smart Configurator for RL78 V1.12.0, when using Visual Studio Code (VS Code) with Renesas Debug extension v25.3.0 or later to create RL78 project by choosing "Renesas: Create RL78 project with Smart Configurator", CMake project is generated for easier build the driver code generated by Smart Configurator for RL78 on Visual Studio Code. Both CCRL toolchain and LLVM toolchain are supported for CMake generation. For detailed how to use the CMake generation for Smart Configurator, please refer to <u>Renesas</u> <u>VS Code Extensions User Guide</u>.

>	
Renesas: Create RL78 project with Smart Configurator	recently used 😂
CMake: Build	
CMake: Delete Cache and Reconfigure	
Renesas: Create RH850 project with Smart Configurator	
Renesas: Open Renesas Support Files Manager	
CMake: Configure	
Renesas: Create RX project with Smart Configurator	
Create LLVM for RL78 project files	
CMake: Clean	
Developer: Reset Welcome Page Walkthrough Progress	
Test: Toggle Test History in Peek	Alt + H
CMake: Build Target	Shift + F7 💱

Figure 2-1 Select "Renesas: Create RL78 project with Smart Configurator" in VS Code





> .settings
$\sim$ .vscode
{} settings.json
{} tasks.json
> build
$\sim$ cmake
∽ src
∽ smc_gen
> general
> r_bsp
> r_config
> r_pincfg
≣ linker_script.ld
C main.c
M CMakeLists.txt
E Config.cmake
≡ demo.scfg
CMake LLVM project erecto

#### Figure 2-3 CMake LLVM project created for VS Code

Note: Smart Configurator doesn't support Flexible Application Accelerator (FAA) component and SNOOZE Mode Sequencer (SMS) component in CMake project.

#### 2.3.4 Show Smart Configurator version at Overview tab

From Smart Configurator for RL78 V1.12.0, Smart Configurator version is displayed at Overview page.



Figure 2-4 Smart Configurator version at Overview page



## 2.3.5 Support new ELCL feature

From Smart Configurator for RL78 V1.12.0, new ELCL feature was supported which can let user to implement flexible circuit creation in GUI by drag & drop and configure the ELCL elements.



Figure 2-5 New ELCL feature



## 3. Changes

This chapter describes changes to the Smart Configurator for RL78 V1.12.0.

## 3.1 Correction of issues/limitations

### Table 3-1 List of Correction of issues/limitations (1/2)

r	No	Description	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	RL78/F25	Remarks
	1	Fixed the issue of the setting of subsystem clock pin operation is wrong when fCLK is from fMP and fSL is from fIL	-	~	-	1	-	-	-	~	
	2	Fixed the issue of 16 bit capture mode with channel 0 and 1 can't be used together with 16 bit count mode with channel 2 and 3	1	-	-	-	1	-	1	_	

#### Table 3-2 List of Correction of issues/limitations (2/2)

✓: Applicable, -: Not Applicable

✓: Applicable, -: Not Applicable

No	Description	RL78/F22	Remarks
1	Fixed the issue of the setting of subsystem clock pin operation is wrong when fCLK is from fMP and fSL is from fIL	~	
2	Fixed the issue of 16 bit capture mode with channel 0 and 1 can't be used together with 16 bit count mode with channel 2 and 3	-	

# 3.1.1 Fixed the issue of the setting of subsystem clock pin operation is wrong when fCLK is from fMP and fSL is from fIL

When fCLK is from fMP and fSL is from fIL, the generated code about CMC.[EXCLKS, OSCSELS] is wrong in r\_bsp\_config.h. From Smart Configurator for RL78 V1.12.0, this issue is fixed.



Figure 3-1 fCLK is from fMP and fSL is from fIL in [Clocks] page



# 3.1.2 Fixed the issue of 16 bit capture mode with channel 0 and 1 can't be used together with 16 bit count mode with channel 2 and 3

If the user wants to use 16 bit count mode with channel 2 and 3 when the user selects 16 bit capture mode and doesn't set "ITLCMP01 compare match interrupt" as "Capture trigger", the user can check "Use 16-bit counter (ITL012 + ITL013)" and sets "Operation clock (fITL1)" and "Interval value".

type filter text	Clock setting Operation clock (fITL0)	fIHP		~			
👻 🗁 Startup	Clock source	fITLO		$\sim$	(Clock frequency: 32000 kHz)		
✓ Generic Image: Im	Capture trigger setting						
✓ ➢ Drivers	Capture trigger	fSXP		$\sim$			
V 🗁 Timers	□ 16-bit counter (ITL000 + ITL001) clear after capture is complete						
Config_IIL000_IIL001	Use 16-bit counter (ITL012 + ITL013)						
Component : Interval Timer	16-bit counter (ITL012 + ITL01	3) setting					
Operation : 16 bit capture mode	Operation clock (fITL1)	fIHP		$\sim$			
- <u></u>	Interval value	100	μs	$\sim$	(Actual value: 100)		
	Interrupt setting						
	Detection of compare match/capture completion (INTITL)						
	Priority	Level 3 (low)		$\sim$			

Figure 3-2 Use 16 bit count mode with channel 2 and 3 in 16 bit capture mode



#### **Specification changes** 3.2

### Table 3-3 List of Specification changes (1/2)

Table	e 3-3 List of Specification changes (1/2)					1	: Ap	plic	able	e, -: Not Applicable
No	Description								RL78/F25	Remarks
1	Improvement for changing "debug monitor" specification	-	-	1		-	1	-	-	
2	Improvement for changing CCRL link options about trace RAM and hot plug-in RAM	1	1	-	1	-	-	1	1	
3	Improvement for delete RL78/F23 LLVM support in Smart Configurator	-	-	I	>	-	-	-	-	
4	Improvement for displaying an error icon when VDD and fCLK are not meeting the conditions for I2S communication function	-	_	-	-	-	-	-	~	
5	Improvement for updating the specification when using Low current conversion mode in A/D Converter	-	-	I	I	-	-	-	~	
6	Improvement for updating the name of Event Link Controller (ELC) in component tree	-	1	-	-	~	-	~	~	
7	Improve the specification of input source and output pin in SAU	1	-	I	1	1	-	-	-	
8	Improve the specification of output pin in UARTA	1	-	-		I	Ι		-	
9	Improve the specification of output pin in TAU	$\checkmark$	_	-	-	-	-	-	-	
10	Improve the specification of input source in PORT	1	-	-	-	-	-	-	-	

## Table 3-4 List of Specification changes (2/2)

✓: Applicable, -: Not Applicable

No	Description	RL78/F22	Remarks
1	Improvement for changing "debug monitor" specification	-	
2	Improvement for changing CCRL link options about trace RAM and hot plug-in RAM	1	
3	Improvement for delete RL78/F23 LLVM support in Smart Configurator	-	
4	Improvement for displaying an error icon when VDD and fCLK are not meeting the conditions for I2S communication function	1	
5	Improvement for updating the specification when using Low current conversion mode in A/D Converter	1	
6	Improvement for updating the name of Event Link Controller (ELC) in component tree	-	
7	Improve the specification of input source and output pin in SAU	-	
8	Improve the specification of output pin in UARTA	-	
9	Improve the specification of output pin in TAU	-	
10	Improve the specification of input source in PORT	-	



## 3.2.1 Improvement for changing "debug monitor" specification

Smart Configurator will set "debug monitor" when setting "On-chip debug operation setting" to "Use emulator" or "COM Port".

On-chip debug operation setting O Unused Use emulator COM Port Figure 3-3 Using "On-chip debug operation setting" in [System] page Device Yes(-OCDBG) Set enable/disable on-chip debug by link option Option byte values for OCD HEN 05 Yes(-DEBUG\_MONITOR) ebug mo Set user option byte Yes(-USER\_OPT\_BYTE) EFF7F9 User option byte value Reserve working memory for RRM/DMM function No Output Code No Specify execution start address Set debug monitor area Specifies whether to set the debug monitor area. This option corresponds to the -DEBUG\_MONITOR option of the rlink command. Common Options / Compile Options / AssembleOptions Link Options Hex

Figure 3-4 Set compiler property "debug monitor" in CS+

Persource       Builders       Configuration:       HardwareDebug [Active]       Manage Configuration:         Builders       Configuration:       HardwareDebug [Active]       Manage Configuration:         Environment JSON Compilation Data Logging       Stotings:       Tool Chain Editor       000000000000000000000000000000000000		Settings		← ▼ ⇒				
C/C++ Build       Configuration:       HardwareDebug       [Active]       Manage Configuration:         Build Variables       Environment       JSON Compilation Dat:       Tool Settings       Dot Configuration:       Build Steps       Build Artifact       Binary Parsers       Error Parsers         Settings       Tool Settings       Tool Settings       Dot Configuration:       Security Id       Dot000000000000000000000000000000000000	Resource							
JSON Compilation Dat.       Tool Settings Toolchain Device       Puild Steps       Build Attifact       Binary Parsers       Error Parsers         Settings       Tool Chain Editor       CPU       Security ID value (-security id)       000000000000000000000000000000000000	C/C++ Build Build Variables Environment	Configuration: HardwareDebug	g [Active]	<ul> <li>Manage Configuration</li> </ul>				
Tool Chain Editor CC++ General Project Natures Project References Renesas QE Run/Debug Settings       Serial Programming Security ID value (-flash_security_id)         Serial Programming Security ID value (-flash_security_id)       Serial Programming Security ID value (-flash_security_id)         Wiscellaneous       Secure working memory for RRM/DMM function (-rrm)         Surves       Secure memory area of OCD monitor - debug monitor)         Memory area (-debug monitor = start address>cend address>)       Memory area (-debug monitor)         Output Code       Wiscellaneous       Miscel aneous         MisAC Rule Check       Set earoption byte (-user_opt_byte= -value>)       EFF7F9         Source       Set escurity option byte value (-ocdbg= -value>)       85         Source       Set escurity option byte value (-ocdbg= -value>)       85         Source       Set escurity option byte value (-ocdbg= -value>)       85         Source       Security option byte value (-security_opt_byte= -value>)       86         Source       Do l	JSON Compilation Dat. Logging Settings	Solution Settings Toolchain Dev	Security ID value (-security id)	2arsers 0000000000000000000000000000000000				
C/C++ General       Device       Reserve working memory for RRM/DMM function (-rrm)         Project References       Source       Secure memory area of OCD monitor (-debug_monitor)         Run/Debug Settings       Source       Secure memory area of OCD monitor (-debug_monitor)         Miscellaneous       Secure memory area of OCD monitor (-debug_monitor)         Miscellaneous       Secure area (-area opt. byte)         Deprimization       Secure option byte (-user_opt. byte)         Miscellaneous       Secure option byte (-user_opt. byte)         Miscellaneous       Set security option byte (-user_opt. byte)         Miscellaneous       Secure         Miscellaneous       Set security option byte (-user_opt. byte)         Miscellaneous       Secure         Miscellaneous       Set security option byte (-user_opt. byte)         Secure       Secure         Source       Secure         Source       Secure         Source       Secure         Secure       Secure option byte (-user_opt_byte)         Secure       Secure         Secure       Secure         Secure       Secure         Secure       Secure         Secure       Secure         Source       Secure         Super	Tool Chain Editor	🚵 CPU	Serial Programming Security ID value (-flash security id)					
Project Natures       Wiscellaneous       Start address area (rm= <value>)       FFB00         Renesas QE       Source       Secure memory area of OCD monitor (-debug_monitor)       Memory area (-debug_monitor)         Nun/Debug Settings       Optimization       Secure remory area (-debug_monitor) = <start address=""> - <end address="">)         Wiscellaneous       Output Code       User option byte (-user_opt_byte=       Secure         Wiscellaneous       Secure the control walue (-user_opt_byte=       BS         Wiscellaneous       Set security option byte value (-user_opt_byte=       BS         Wiscellaneous       Secure       Security option byte (-user_opt_byte=         Wiscellaneous       Set security option byte (-security_opt_byte)       BS         Wiscellaneous       Secure       Security option byte (-security_opt_byte)       BS         Wiscellaneous       Security option byte (-security_opt_byte)       Security option byte (-security_opt_byte)       Security option byte (-security_opt_byte)         Source       Security option byte walue (-security_opt_byte)       Security option byte walue (-security_opt_byte)       Security option byte walue (-security_opt_byte)         Source       Security option byte walue (-security_opt_byte)       Security option byte walue (-security_opt_opt_byte)       Security option byte walue (-security_opt_opt_byte)         Source       Suppress checking sec</end></start></value>	C/C++ General	Device	Reserve working memory for RRM/DMM function (-rrm)					
Toget References       Implicit doubles and state of the specifications of the specification	Project Natures	Miscellaneous     Miscellaneous	Start address area (-rrm-cvalues)	FEBOO				
Run/Debug Settings	Project References Renesas OF	v 🖉 Source	Service memory area of QCD monitor (-debug monitor)	11000				
Object       User option byte (-user_opt_byte)         Output Code       User option byte (-user_opt_byte)         Miscellaneous       Set enable/disable on-chip debug by link option (-ocdbg)         Miscellaneous       Set enable/disable on-chip debug by link option (-ocdbg)         Miscellaneous       Set enable/disable on-chip debug by link option (-ocdbg)         Miscellaneous       Set enable/disable on-chip debug by link option (-ocdbg)         Miscellaneous       Set enable/disable on-chip debug by link option (-ocdbg)         Saurce       Set enable/disable on-chip debug by link option (-ocdbg)         Saurce       Security option byte (-security_opt_byte)         Saurce       Security option byte (-security_opt_byte)         Saurce       Security option byte (-security_opt_byte)         Saurce       Security option byte value (-security_opt_byte)	Run/Debug Settings	🖉 Language	Memory area (-debug, monitor= <start address="">-<end address=""></end></start>	)				
Optimization       User option byte value (-user_opt_byte «value»)       EFF79         Miscellaneous       Set enable/disable on-chip debug by link option (-ocdbg)       On-chip debug control value (-ocdbg= <value»)< td="">       85         State       Set enable/disable on-chip debug by link option (-ocdbg)       On-chip debug control value (-ocdbg=<value»)< td="">       85         State       Set enable/disable on-chip debug pointo byte (-security_opt byte)       Set security option byte (-security_opt byte)         State       Set security option byte value (-security_opt byte= value&gt;)       Area to be excluded from RAM area (-selfy-codtr)       None         Object       Area to be excluded from RAM area (-selfy-codtr) - ocdhpi)       None       Output warning message if sections are allocated to the specified area (-selfw/-ocdtrw/-ocdhpiw)         Miscellaneous       Check specifications of device (-check_device)       Suppress checking section allocation that crosses (64K8-1) boundary (-check_64k_only)         Stating       Do not check memory allocation of sections (-no_check_section_layout)       Address range of memory type (-cpu)         Stating       Optimization       Socion       Socion       Socion         Optimization       Socion       Socion       Socion       Socion         Optimization       Socion       Socion       Socion       Socion         Optimization       Socion       Socion       S</value»)<></value»)<>		Object	Set user option byte (-user opt byte)					
Miscellaneous		Dutput Code	User option byte value (-user opt byte= <value>)</value>	EFF7E9				
MISRA C Rule Check       On-chip debug control value (-ocdbg= <values)< td="">       85         Set       Set security option byte (-security_opt_byte)       Image: Set security option byte (-security_opt_byte)         Set       Set security option byte value (-security_opt_byte)       Image: Set security option byte value (-security_opt_byte)         Set       Security option byte value (-security_opt_byte)       Image: Set security option byte value (-security_opt_byte)         Set       Security option byte value (-security_opt_byte)       Image: Set security option byte value (-security_opt_byte)         Set       Area to be excluded from RAM area (-self/-ocdtr/-ocdhpi)       Image: Set Security option byte value (-security_opt_byte)         Set       Set       Image: Set Security option byte value (-security_opt_byte)         Set       Image: Set Security option of sections are allocation that crosses (64KB-1) boundary (-check_64k_only)         Image: Security optimization       Image: Security option of sections (-no_check_section_layout)         Security optimization       Security Securi</values)<>		Miscellaneous	Set enable/disable on-chip debug by link option (-ocdbg)					
Ver      Sextion     Sext		MISRA C Rule Check	On-chip debug control value (-ocdbg= <value>)</value>	85				
Source Security option byte value (-security.opt.byte= <value>) Area to be excluded from RAM area (-self/-ocdtr/-ocdtpi) None Object Object Object Output warning message if sections are allocated to the specified area (-selfw/-ocdthw/-ocdthw/-ocdthw/) Gutput warning message if sections are allocated to the specified area (-selfw/-ocdthw/-ocdthw/) Gutput warning message if sections are allocated to the specified area (-selfw/-ocdthw/-ocdthw/) Gutput warning message if sections are allocated to the specified area (-selfw/-ocdthw/-ocdthw/) Gutput warning message if sections are allocated to the specified area (-selfw/-ocdthw/-ocdthw) Gutput warning message if sections of device (-check_device) Gutput warning message if section allocation that crosses (64KB-1) boundary (-check_64k_only) Gutput warning message of memory type (-cpu) Address range of memory type (-cpu)</value>		Ser Ser	Set security option byte (-security opt byte)					
ⓐ Language         ⓑ Object           Area to be excluded from RAM area (-self/-ocdtr/-ocdtpi)           None             ⓑ Objinization           ○utput warning message if sections are allocated to the specified area (-selfw/-ocdtnw/-ocdtpiw)           None             ⓑ Miscellaneous           □ Check specifications of device (-check_device)           □ suppress checking section allocation that crosses (64KB-1) boundary (-check_64k_only)             ⓑ Advanced           ⓑ Advanced           △ Address range of memory type (-cpu)             ⓑ Optimization           ⓑ Optimization           ⓑ Dowice		✓ 🦉 Source	Security option byte value (-security opt byte= <value>)</value>					
Work       Output warning message if sections are allocated to the specified area (-selfw/-ocdtpiw)         Miscellaneous       Check specifications of device (-check_device)         User       Suppress checking section allocation that crosses (64KB-1) boundary (-check_64k_only)         Inter       Do not check memory allocation of sections (-no_check_section_layout)         Address range of memory type (-cpu)         Continue         Optimization         Continue         Device		🚵 Language	Area to be excluded from RAM area (-self/-ocdtr/-ocdhpi)	None				
Miscellaneous     User     Suppress checking section allocation of sections (-no_check_section_layout)     Superss checking section allocation of sections (-no_check_section_layout)     Address range of memory type (-cpu)     Suppress checking section allocation of sections     Optimization     Suppress checking section allocation of sections     Optimization     Suppress checking section allocation of sections     Optimization     Suppress checking section allocation of sections     Suppress		Object Optimization	Output warning message if sections are allocated to the speci	fied area (-selfw/-ocdtrw/-ocdbpiw)				
User       Suppress checking section allocation that crosses (64KB-1) boundary (-check_64k_only)         Inker       Do not check memory allocation of sections (-no_check_section_layout)         Advanced       Address range of memory type (-cpu)         Optimization       Section         Device       Device		A Miscellaneous	Check specifications of device (-check_device)					
Gunker     Minker     Monte in the interval of section of sections (-no_check_section_layout)     Advanced     Substanced     Optimization     Societie     Device		🚵 User	Suppress checking section allocation that crosses (64KB-1) boundary (-check 64k only)					
Advanced     Adverse range of memory type (-cpu)     Section     Section     Device		N 😸 Linker	Do not check memory allocation of sections (-no_check_sectio	n_layout)				
≥ List ⊘ Optimization ≫ Coertion ≫ Device		Advanced	Address range of memory type (-cpu)					
Optimization		🖉 List						
Device		Optimization						
Device		A Contion						
× @ Output		Z Output						
Advanced		Advanced						

Figure 3-5 Set compiler property "debug monitor" in e<sup>2</sup> studio

Note: The supported compilers only include CCRL.



## 3.2.2 Improvement for changing CCRL link options about trace RAM and hot plug-in RAM

When "On-chip debug operation setting" is set to "Use emulator" or "COM Port" and "Trace function setting" is set to "Used", the compiler property will be changed after generating code.

<ul> <li>On-chip debug setting</li> </ul>		
On-chip debug operation	setting	O COM Port
Emulator setting	• E2 Lite	
Pseudo-RRM/DMM funct	ion setting	
Start/Stop function setting Unused	) Used	
Monitoring point function <ul> <li>Unused</li> </ul>	setting Used	
Trace function setting	• Used	

Figure 3-6 Use trace function in [System] page

Smart Configurator will set [Control allocation to trace RAM area] property to [Yes(Exclude trace RAM area)(-STRIDE\_OCDTR\_AREA)] in CS+.

-		
~	Device	
	Set enable/disable on-chip debug by link opt	i Yes(-OCDBG)
	Option byte values for OCD	HEX A4
	Set security option byte	Yes(-SECURITY_OPT_BYTE)
	Security option byte value	HEX FE
	Set debug monitor area	Yes(Specify address range)(-DEBUG_MONITOR= <address range="">)</address>
	Range of debug monitor area	1FE00-1FFFF
	Set user option byte	Yes(-USER_OPT_BYTE)
	User option byte value	HEX EFFAF8
	Control allocation to trace RAM area	Yes(Exclude trace RAM area)(-STRIDE_OCDTR_AREA)
	Control allocation to hot plug-in RAM area	No
~	Output Code	
	Specify execution start address	No
Co Spe ase are Thi	ntrol allocation to trace RAM area acifies the control of the allocation to the trace signed excluding the trace RAM, self RAM are thion allocation to the trace RAM, self RAM are assigned striding over the trace RAM area. V s option corresponds to the -OCDTR/-OCDT	RAM and self RAM areas. When "Yes(Error message)(-OCDTR)" is specified, as. When "Yes(Warning message)(-OCDTRW)" is specified, a warning is outpu as. When "Yes(Exclude trace RAM area)(-STRIDE_OCDTR_AREA)" is specified when "No" is specified, the trace RAM area is used as an internal RAM area. RW/-STRIDE_OCDTR_AREA options of the rlink command.
~	umman Ontinga / Compile Ontings / Argon	ha Ontio Link Ontions Hay Output Ont Standard Librar / 1/0 H

Figure 3-7 [Control allocation to trace RAM area] property in CS+



Smart Configurator will check [Exclude trace RAM area from RAM area (-stride\_ocdtr\_area)] property in e<sup>2</sup> studio with CCRL v1.15.



Figure 3-8 [Exclude trace RAM area from RAM area (-stride\_ocdtr\_area)] property in e<sup>2</sup> studio

When "On-chip debug operation setting" is set to "Use emulator" or "COM Port" and "Hot plug-in function setting" is set to "Used", the compiler property will be changed after generating code.

<ul> <li>On-chip debug setting</li> </ul>		
On-chip debug operation set	tting Use emulator	○ COM Port
Emulator setting C E20	○ E2	• E2 Lite
Pseudo-RRM/DMM function	setting Used	
Start/Stop function setting Unused	OUsed	
Monitoring point function se Unused	tting Used	
Trace function setting	OUsed	
Hot plug-in function setting	• Used	

Figure 3-9 Use hot plug-in function in [System] page



Smart Configurator will set [Control allocation to hot plug-in RAM area] property to [Yes(Exclude hot plug-in RAM area)(-STRIDE\_OCDHPI\_AREA)] in CS+.



Figure 3-10 [Control allocation to hot plug-in RAM area] property in CS+

Smart Configurator will check [Exclude hot plug-in RAM area from RAM area (-stride\_ocdhpi\_area)] property in e<sup>2</sup> studio with CCRL v1.15.



Figure 3-11 [Exclude hot plug-in RAM area from RAM area (-stride\_ocdhpi\_area)] property in e<sup>2</sup> studio

Note: The specification is keeped in  $e^2$  studio with CCRL v1.14 or before.

### 3.2.3 Improvement for delete RL78/F23 LLVM support in Smart Configurator

Smart Configurator doesn't support RL78/F23 LLVM from Smart Configurator for RL78 V1.12.0.



# 3.2.4 Improvement for displaying an error icon when VDD and fCLK are not meeting the conditions for I2S communication function

The User's Manual (R01UH1061EJ0050) has an error about I2S communication function. If the user wants to use I2S communication function, it should meet the conditions: 2.7 V  $\leq$  VDD  $\leq$  5.5 V and 8 MHz  $\leq$  fCLK  $\leq$  40 MHz. Smart Configurator for RL78 V1.12.0 adds the judgment about VDD and fCLK. If the conditions are not meeted, an error icon will display after checkbox "Enable" in I2S communication function. The User's Manual (R01UH1061EJ0100) will fix this error.



Figure 3-12 VDD and fCLK setting in [Clocks] page

Please set 2.7 V $\leq$ VDD $\leq$ 5.5 V,	8 N	1Hz ≤ fCLK ≤ 40 MHz wh	en using I2S communication.	
		Disable	◯ Enable 😈	
		Please set TAU12 to in	terval timer mode and TAU13 to event counter mode when I2S communication is enab	bled.

Figure 3-13 The error icon in I2S communication function

# 3.2.5 Improvement for updating the specification when using Low current conversion mode in A/D Converter

The User's Manual (R01UH1061EJ0050) lacks some Notes when using Low current conversion mode in A/D Converter. Smart Configurator updated A/D Converter GUI and code specification. The User's Manual (R01UH1061EJ0100) will fix these errors.



Figure 3-14 VDD setting in [Clocks] page



• GUI specification: Change the sampling time range of ANIn and the conversion time in groupbox "Input sampling time setting". (n = 0 - 29)

Input sampling time setting							
ANI0/Self-diagnosis	1	(µs) (Actual value: 1)					
ANI1	0.325	(μs) (Actual value: 6.5)					
ANI2	0.525	(μs) (Actual value: 0.5)					
ANI3	0.525	(μs) (Actual value: 0.5)					
ANI4	0.325	(μs) (Actual value: 6.5)					
ANI5	0.325	(μs) (Actual value: 6.5)					
ANI6	0.325	(μs) (Actual value: 6.5)					
ANI7	0.325	(μs) (Actual value: 6.5)					
ANI8	0.325	(μs) (Actual value: 6.5)					
ANI9	0.325	(μs) (Actual value: 6.5)					
ANI10	0.325	(μs) (Actual value: 6.5)					
ANI16-ANI29	6	(µs) (Actual value: 6)					
	(First cycle conver	(First cycle conversion time: 74µs)					
	(Subsequent cycle	(Subsequent cycle conversion time: 72µs)					

Figure 3-15 Input sampling time setting

When selecting VDD as "4.0 V  $\leq$  VDD  $\leq$  5.5 V" or "2.7 V  $\leq$  VDD  $\leq$  5.5 V", the min sampling time of ANI0 - ANI15 is 0.337 µs and the min sampling time of ANI16 - ANI29 is 1.012 µs.

When selecting VDD as "1.8 V  $\leq$  VDD  $\leq$  5.5 V", the min sampling time of ANI0 - ANI15 is 1.688 µs and the min sampling time of ANI16 - ANI29 is 2.563 µs.

When selecting VDD as "1.8 V  $\leq$  VDD  $\leq$  5.5 V", the time for conversion by successive approximation changes to 40.5  $\times$  ADCLK. Smart Configurator updates the messages about conversion time values for "First cycle conversion time" and "Subsequent cycle conversion time".

• GUI specification: When selecting VDD as "1.8 V  $\leq$  VDD  $\leq$  5.5 V", Smart Configurator adds an error icon after ANI1 and ANI2.

- Advanced setting		
A/D sample-and-hold circuit setting	Please set VDD > = 2.7V when using A/D sample-and-hold circuit	-
🗹 ANI1 😉		
Dedicated sample and hold circuit	4 (μs) (Actual value: 4)	

Figure 3-16 The message after ANI1 and ANI2 when VDD is "1.8 V  $\leq$  VDD  $\leq$  5.5 V"

• GUI specification: When selecting VDD as "1.8 V ≤ VDD ≤ 5.5 V", Smart Configurator adds an error icon when Clock source is greater than 8MHz.

Setting	g is no	ot valid, clock source can't be set to a fr	equency greater than 8	MHz.	
		Clock source	fCLK	× 🕘	(Clock frequency: 16000 kHz)

Figure 3-17 The message when "Clock source" is greater than 8MHz

• Code specification: When selecting VDD as "4.0 V  $\leq$  VDD  $\leq$  5.5 V" or "2.7 V  $\leq$  VDD < 5.5 V", ADCSR.ADHSC will be set to 0 in API R\_Config\_S12AD0\_Create().

Old driver code	Current driver code
	/* Set INTAD low priority */
/* Set INTAD low priority */	ADPR1 = 1U;
ADPR1 = 1U;	ADPR0 = 1U;
ADPR0 = 1U;	ADCSR &= (~ 0400 AD LOW CURRENT CONVERSION ENABLE);
/* Set transition analog block to operation mode */	<pre>/* Set transition analog block to operation mode */</pre>
ADWINR = _08_AD_ADGSPCR_ADHVREFCNT_RW_ENABLE;	ADWINR = 08 AD ADGSPCR ADHVREFCNT RW ENABLE;
Figure 3-18 Set ADCSR.ADHSC in	API R_Config_S12AD0_Create()



**3.2.6** Improvement for updating the name of Event Link Controller (ELC) in component tree Smart Configurator updates the name of Event Link Controller (ELC) in component tree.

Old name in file tree	
Components	èn da la₂ ⊟ 🕀
5월 [][]	10 T
type filter text	
👻 🗁 Startup	
🗸 🗁 Generic	
💣 r_bsp	
Logic and event link controller	
Config_ELC	

Current name in file	tree
Components	ù 🕹 📲 🗉 🕀
5日 時	ت ن
type filter text	
🗸 🗁 Startup	
👻 🗁 Generic	
💣 r_bsp	
<ul> <li>Drivers</li> <li>Event link controller</li> <li>Config_ELC</li> </ul>	

## Figure 3-19 the name of Event Link Controller (ELC) in file tree

### 3.2.7 Improve the specification of input source and output pin in SAU

For supporting new ELCL feature (See 2.3.5 Support new ELCL feature for details), Smart Configurator updates the specification of input source and output pin in SAU.

 SAU CSI specification: When using CSImn as Reception or Transmission/reception, the user can select input source for SCKmn ("Transfer clock mode" should set to "External clock (slave)") and SImn. (mn = 00, 01)

	🔇 New Component			×	
A	dd new configuration f	or selected component			
	SPI (CSI) Communicatio	on			
	Configuration name:	Config_CSI00			
	Operation:	Transmission		~	
	Resource:	Transmission Reception			
		Transmission/reception			

Figure 3-20 Operation selection when adding SAU CSI

Transfer clock setting		
Transfer clock mode	External clock (slave)	$\sim$
Operation clock	СК00	$\sim$
Clock source	fCLK	$\sim$
Transfer rate setting		
Baudrate	153600	∨ (bps)
Input source setting		
Serial clock input source	SCK00	$\sim$
Serial data input source	S100	$\sim$

Figure 3-21 "Input source setting" in SAU CSI



When using CSImn as Transmission or Transmission/reception, the user can select whether to output SCKmn ("Transfer clock mode" should set to "Internal clock (master)") and SOmn signal. (mn = 00, 01)

Transfer clock setting			
Transfer clock mode	Internal clock (master)	$\sim$	
Operation clock	СК00	$\sim$	
Clock source	fCLK	✓ (Clock frequency: 2000 kHz)	
Transfer rate setting			
Baudrate	153600	V (bps) (Actual value: 142857.1	43)
Output setting			
The serial clock output is only to	be used for input to the ELCL	and not for the SCK00 pin	
The serial data output is only to b	e used for input to the ELCL	and not for the SO00 pin	

Figure 3-22 "Output setting" in SAU CSI

 SAU UART specification: When using UART0 as Transmission or Transmission/reception, the user can select whether to output TxD0 signal.

Kew Component			×
Add new configuration	for selected component	ł	
UART Communication			
Configuration name:	Config_UART0		
Operation:	Transmission		~
Resource	Transmission		
Resource.	Reception Transmission/reception		

Figure 3-23 Operation selection when adding SAU UART

Deration clock	CK00	
Clock source	fCLK v (Clock frequency: 2000 kF	Hz)
Fransfer rate setting		
Transfer rate setting Transfer rate setting	153600 V (bps) (Current error	: -6.99

Figure 3-24 "Output setting" in SAU UART



SAU IIC specification: When using IICmn, the user can select whether to output SCLmn signal. (mn = 00, 01)

IIC00 clock setting				
Operation clock	СК00	~		
Clock source	fCLK	~	(Clock	frequency: 2000 kHz)
Transfer rate setting				
Transfer rate	100000		(bps)	(Actual value: 100000)
Output setting				
☐ The serial clock output is only to b	e used for input to the ELCL and not	t for the SCL	.00 pin	

Figure 3-25 "Output setting" in SAU IIC

## 3.2.8 Improve the specification of output pin in UARTA

For supporting new ELCL feature (See 2.3.5 Support new ELCL feature for details), Smart Configurator updates the specification of output pin in UARTA.

ổ New Component			×
Add new configuration f	or selected component		
UART Communication			
Configuration name:	Config_UARTA1		
Operation:	Transmission		~
Resource:	Transmission Reception		
	Transmission/reception		

Figure 3-26 Operation selection when adding UARTA

• UARTA0 specification: When using UARTA0, Smart Configurator updates the GUI and driver code.

Old GUI				Current (	GUI	
			UARTA0 clock setting Operation clock ELCL clock	<b>fSEL</b> 32000	~	fSEL clock select fMXP (kHz)
UARTA0 clock setting           Operation clock         fSEL         fSEL clock select fMXP v           ELCL clock         32000         (kHz)			UARTA0 clock output signal setting Disable CLKA0 pin output setting Disable			<ul> <li>Enable</li> <li>Enable</li> </ul>
CLKA0 pin output setting O Disable Data length setting		Enable	The serial clock output is TxDA0 pin output setting Disable	used for input to the	ELCL alw	ays. ● Enable
○ 5 bits	⊖7 bits	8 bits	The transmit data output	is used for input to th	he ELCL a	lways.

## Figure 3-27 UARTA0 GUI

 When using UARTA0 as Transmission or Transmission/reception, Smart Configurator changes the groupbox name from "CLKA0 pin output setting" to "UARTA0 clock output signal setting" and updates the driver code about setting UTA0CK.UTA0OEN.



#### [Before]



## [After]



Note: UTA0CK.UTA0OEN setting will change in API R\_Config\_UARTA0\_Start() according to GUI setting.

- When using UARTA0 as Transmission or Transmission/reception, Smart Configurator adds the groupbox "CLKA0 pin output setting" and "TxDA0 pin output setting" and the user can select whether to output CLKA0 ("UARTA0 clock output signal setting" should set to "Enable") and TxDA0 signal.
- When using UARTA0 as Reception, Smart Configurator removes the groupbox "CLKA0 pin output setting" and removes the driver code about setting UTA0CK.UTA0OEN.



• UARTA1 specification: When using UARTA1, Smart Configurator updates the GUI and driver code.

	Old GUI	Current	GUI
CLKA1 pin output setting	○ Enable	UARTA1 clock output signal setting O Disable	Enable

Figure 3-28 UARTA1 GUI

- When using UARTA1 as Transmission or Transmission/reception, Smart Configurator changes the groupbox name from "CLKA1 pin output setting" to "UARTA1 clock output signal setting" and updates the driver code about setting UTA1CK.UTA10EN.

[Before]
<pre>void R_Config_UARTA1_Create(void) { UTAOCK  = 10 UARTA FSEL SELECT FMXP; UTAICK = 80_UARTA_CLKA1_OUTPUT_ENABLE } _00_UARTA1_SELECT_FSEL /* Set CLKA1 pin */ P3 &amp;= 0xFBU; PM3 &amp;= 0xFBU;</pre>
<pre>void R_Config_UARTA1_Start(void) {     volatile uint8_t w_count;     HAPTAEN1 = 10;     TXEA1 = 10; }</pre>
1
<pre>void R_Config_UARTA1_Stop(void) {     TYER1 = 0U;     UARTAEN1 = 0U; }</pre>

## [After]

void R_Config_UARTA1_Create(void)
UTAOCK = 10_UARTA_FSEL_SELECT_FMXP;
UTA1CK = 00_UARTA1_SELECT_FSEL;
/* Set CLRAl pin */
PM3 = 0xFBU;
-)
/*****
* Function Name: R_Config_UARTA1_Start
* Description : This function starts UARTA1 module operation.
* Arguments : None * Return Value : None
*****
<pre>void R_Config_UARTA1_Start(void)</pre>
<pre>{     relatile wint0 t u count. </pre>
Volatile dinte_t w_count,
UARTAEN1 = 1U;
UTA1CK  = 80_UARTA_CLKA1_OUTPUT_ENABLE;
TXEAT = 10;
-)
/
* Function Name: R Config UARTA1 Stop
* Description : This function stops UARTA1 module operation.
* Arguments : None
* Return Value : None
void R Config UARTA1 Stop(void)
(
TXEA1 = 011;
UARTAENI = 00;
h



Note: UTA1CK.UTA1OEN setting will change in API R\_Config\_UARTA1\_Start() according to GUI setting.

- When using UARTA1 as Reception, Smart Configurator removes the groupbox "CLKA1 pin output setting" and removes the driver code about setting UTA1CK.UTA10EN.

### 3.2.9 Improve the specification of output pin in TAU

For supporting new ELCL feature (See 2.3.5 Support new ELCL feature for details), Smart Configurator updates the specification of output pin in TAU. When using TAU - Square Wave Output, Divider Function, One-Shot Pulse Output and PWM Output, the user can select whether to output TO0n signal. (n = 0 - 7)

Output setting	
Initial output value	0 ~
The timer output is only to be used	d for input to the ELCL and not for the TO00 pin

Figure 3-29 "Output setting" in TAU

#### 3.2.10 Improve the specification of input source in PORT

For supporting new ELCL feature (See 2.3.5 Support new ELCL feature for details), Smart Configurator updates the specification of input source in PORT. When using PORT as Out, the user can select input source from ELCL.

P01						
⊖ Unused	$\bigcirc$ In	Out	Pull-up	TTL buffer	Output 1	□ Output ELCL output signal

Figure 3-30 PORT GUI



## 4. List of RENESAS TOOL NEWS AND TECHNICAL UPDATE

Below is a list of notifications delivered by RENESAS TOOL NEWS and TECHNICAL UPDATE.

Issue date	Document No.	Description	Applicabl e MCUs	Fixed version
Oct. 01, 2021	R20TS0757	1. Notes on creating LLVM for Renesas RL78 C/C++ Executable Project 2. Notes on using Port Input buffer function https://www.renesas.com/document/tnn/notes- e-studio-smart-configurator-plug-smart- configurator-rl78	RL78/G23	V1.2.0
Mar. 16, 2022	R20TS0822	1. Notes when build or clean e <sup>2</sup> studio Smart Configurator project <u>https://www.renesas.com/document/tnn/notes-</u> <u>e-studio-smart-configurator-plug-smart-</u> <u>configurator-rl78-0</u>	RL78/G23	V1.3.0
Dec. 01, 2022	R20TS0895	1. Notes when changing version of Board Support Program (BSP) or RL78 Software Integration System (SIS) modules <u>https://www.renesas.com/us/en/document/tnn/</u> <u>notes-e-studio-smart-configurator-rl78-plug-</u> <u>smart-configurator-rl78</u>	RL78/G23 RL78/F24 RL78/G15	V1.5.0



## 5. Points for Limitation

This section describes points for limitation regarding the Smart Configurator for RL78 V1.12.0.

#### 5.1 List of Limitation

## Table 5-1 List of Limitation (1/2)

Table 5-1List of Limitation (1/2) <t< th=""><th>-: Not Applicable</th></t<>							-: Not Applicable			
No	Description	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	RL78/F25	Remarks
1	Note on extra help document issue	$\checkmark$	✓	1	✓	✓	✓	1	1	
2	Note on ELCL D flip flop component GUI warning display incorrectly	1	-	-	-	_	-	-	-	
3	Note on the unsupported setting items for some ELCL components	1	-	-	-	-	-	-	-	
4	Note on the user code protection feature will only be supported on the files that are generated by the Code Generation component	~	~	~	~	~	~	~	<	
5	Note on Flexible Application Accelerator (FAA) component does not support LLVM project	-	-	-	-	-	-	1	-	
6	Note on not using Flexible Application Accelerator (FAA) component in Mac OS and Linux	-	-	-	-	_	-	~	-	
7	Note on not using SNOOZE Mode Sequencer (SMS) component in Mac OS and Linux	1	-	-	-	1	_	-	-	
8	Note on not correcting the errors in the User's Manual	-	✓	-	✓	-	-	-	-	
9	Note on UI display with High Contrast theme on Linux OS	1	~	1	1	1	1	1	✓	

## Table 5-2 List of Limitation (2/2)

✓: Applicable, -: Not Applicable

No	Description	RL78/F22	Remarks
1	Note on extra help document issue	✓	
2	Note on ELCL D flip flop component GUI warning display incorrectly	-	
3	Note on the unsupported setting items for some ELCL components	-	
4	Note on the user code protection feature will only be supported on the files that are generated by the Code Generation component	~	
5	Note on Flexible Application Accelerator (FAA) component does not support LLVM project	-	
6	Note on not using Flexible Application Accelerator (FAA) component in Mac OS and Linux	-	
7	Note on not using SNOOZE Mode Sequencer (SMS) component in Mac OS and Linux	_	
8	Note on not correcting the errors in the User's Manual	-	
9	Note on UI display with High Contrast theme on Linux OS	1	



## 5.2 Details of Limitation

## 5.2.1 Note on extra help document issue

For Smart Configurator, there is an extra help "Smart Browser" under "[Help] > [Help Contents]". Please ignore it.

Hel	p	
?	Help Contents	🔿 🚺 Help - Smart Configurator
-	Home Page	Search:
	Release Notes	Contents 👜 🚽 🚀 🕇
	Tool News	🗄 🧇 Smart Browser
	API Manual	🗄 🥯 Smart Configurator for RL78
ß	About	





## 5.2.2 Note on ELCL D flip flop component GUI warning display incorrectly

When selecting the event signal in ELCL D flip flop component, even if the selected signal consists with the hardware specification, there still displays the warning on the GUI.

#### [Workaround]

Make reference to the hardware manual and set the selectable event signal though warning appeared in GUI, the waring is no impact for the code generation.

The following is example of using flip-flop 0 and flip-flop 1 in ELCL logic cell block L1.



Figure 5-2 The flip-flop 0 in ELCL logic cell block L1 usage example



Figure 5-3 The flip-flop 1 in ELCL logic cell block L1 usage example



## 5.2.3 Note on the unsupported setting items for some ELCL components

In the following ELCL modules, it is not possible to set "no selection (fixed to 0)" as the input signal of the logic cell block and "negative logic output (inverted)" as the output level of the event signal.

- ELCL AND
- ELCL D flip flop
- ELCL EXOR
- ELCL selector
- ELCL Through

## [Workaround] None

# 5.2.4 Note on the user code protection feature will only be supported on the files that are generated by the Code Generation component

The user code protection feature will only be supported on the files that are generated by the Code Generation component. Hence, the user code protection feature is not available for non-Code Generation components.

🔞 New Component									
Software Component Selection									
1	Select com	nponent from those available in li	st						
	<b>C</b> -1	All							
Category All									
Function All							$\sim$		
	Filter						_		
	Compon	ents	Short Name	Туре		Versi	^		
	⊞ A/D C	onverter		Code Generator		1.4.1			
	🖶 Board	l Support Packages v1.61	r_bsp	RL78 Software Integration Syster	n	1.61			
	🖶 Capac	itive Sensing Unit driver.	r_ctsu	RL78 Software Integration System	n	1.40			
	🕀 Capac	itive Sensing Unit driver.	r tkbo	RL78 Software Integration Syster	n	1.40			
	🖶 Clock	Output /Buzzer Output Contro		Code Generator		1.4.0			
	🖶 Comp	arator		Code Generator		1.3.1			
	🖶 D/A C	onverter		Code Generator		1.3.0			
	🖶 Data 1	Fransfer Controller		Code Generator		1.3.1			
	🖶 Delay	Counter		Code Generator		1.4.1			
	🖶 Divide	r Function		Code Generator		1.4.1			
	S ELCL /	AND		Graphical Configurator		1.1.0			
	St ELCL o	chattering prevention		Graphical Configurator		2.0.0			
		D flip flop		Graphical Configurator		1.1.0			

Figure 5-4 Code Generation component in red frame

# 5.2.5 Note on Flexible Application Accelerator (FAA) component does not support LLVM project

In Smart Configurator for RL78 V1.7.0 or later, Flexible Application Accelerator component was not supported for LLVM project. Though the user can add Flexible Application Accelerator component under LLVM project, but the generated Flexible Application Accelerator source code can't be built successfully and works for running and debugging.

# 5.2.6 Note on not using Flexible Application Accelerator (FAA) component in Mac OS and Linux

In Smart Configurator for RL78 V1.10.0 or later, Flexible Application Accelerator component was not supported in Mac OS and Linux. Though the user can add Flexible Application Accelerator component in Mac OS and Linux, but the generated Flexible Application Accelerator source code can't be built successfully and works for running and debugging.



## 5.2.7 Note on not using SNOOZE Mode Sequencer (SMS) component in Mac OS and Linux

In Smart Configurator for RL78 V1.10.0 or later, SNOOZE Mode Sequencer component was not supported in Mac OS and Linux. Though the user can add SNOOZE Mode Sequencer component in Mac OS and Linux, but the generated SNOOZE Mode Sequencer source code can't be built successfully and works for running and debugging.

## 5.2.8 Note on not correcting the errors in the User's Manual

There are some errors in RL78/F23 and RL78/F24 User's Manual (R01UH0944EJ0100). Smart Configurator will correct these errors in next release. Please refer to the document <u>TN-RL\*-A0139A/E</u> for details.

## 5.2.9 Note on UI display with High Contrast theme on Linux OS

When using  $e^2$  studio with High Contrast theme on Linux OS, some display texts of Smart Configurator can't be seen. To avoid this issue, please use other themes.



Figure 5-5 UI display with High Contrast theme



Smart Configurator for RL78 Plug-in in e<sup>2</sup> studio 2025-01

Smart Configurator for RL78 V1.12.0

## 6. Points for Caution

This section describes points for caution regarding the Smart Configurator for RL78 V1.12.0.

## 6.1 List of Caution

## Table 6-1 List of Caution (1/2)

✓: Applicable, -: Not Applicable

No	Description	RL78/G23	RL78/F24	RL78/G15	RL78/F23	RL78/G22	RL78/G16	RL78/G24	RL78/F25	Remarks
1	Note on the build error message such as "section .bss virtual address range overlaps with .dtc_vectortable"	~	1	-	1	1	-	1	~	
2	Note on the installation of the Smart Configurator	1	1	1	1	✓	1	1	✓	
3	Note on using TRDIOA0 for Input capture and TRDIOB0 for Output compare at same time	-	1	-	-	-	-	1	~	
4	Note on pulse width calculation of Timer RD input capture function	-	1	-	-	-	-	1	~	
5	Note on the include path update issue when renaming the component's configuration name	1	1	1	1	1	1	1	~	
6	Note on TAU Input Signal High/Low level Measurement components.	1	1	1	~	1	1	1	~	
7	Note on CC-RL V1.12 C++ project	1	1	<	✓	<	✓	✓	<	
8	Note on browsing "Release Notes" and "Tool News" URL from the help menu	~	1	1	-	-	-	-	-	
9	Note on using the user code protection feature	1	✓	✓	1	✓	1	1	1	
10	Note on IAR build error when using SNOOZE Mode Sequencer (SMS) function	1	-	-	-	-	-	-	-	
11	Note on A/D conversion time setting after performing [Change device] or [Change resource]	~	1	1	1	~	1	1	<	
12	Note on changing Hardware Debug Configuration on project generation wizard	1	1	1	1	1	1	1	~	
13	Note on Pin Number maybe wrong in [Pins] page when loading project	-	-	_	-	-	-	1	-	
14	Note on Pin assignment with PIOR maybe wrong in [Pins] page when changing device	1	1	1	1	1	1	1	~	



Release Note

## Table 6-2 List of Caution (2/2)

✓ : Applicable, -: Not Applicable

No	Description	RL78/F22	Remarks
1	Note on the build error message such as "section .bss virtual address range overlaps with .dtc_vectortable"	1	
2	Note on the installation of the Smart Configurator	1	
3	Note on using TRDIOA0 for Input capture and TRDIOB0 for Output compare at same time	1	
4	Note on pulse width calculation of Timer RD input capture function	1	
5	Note on the include path update issue when renaming the component's configuration name	1	
6	Note on TAU Input Signal High/Low level Measurement components.	1	
7	Note on CC-RL V1.12 C++ project	1	
8	Note on browsing "Release Notes" and "Tool News" URL from the help menu	-	
9	Note on using the user code protection feature	1	
10	Note on IAR build error when using SNOOZE Mode Sequencer (SMS) function	-	
11	Note on A/D conversion time setting after performing [Change device] or [Change resource]	1	
12	Note on changing Hardware Debug Configuration on project generation wizard	1	
13	Note on Pin Number maybe wrong in [Pins] page when loading project	-	
14	Note on Pin assignment with PIOR maybe wrong in [Pins] page when changing device	1	



## 6.2 Details of Caution

# 6.2.1 Note on the build error message such as "section .bss virtual address range overlaps with .dtc\_vectortable"

When the user uses many components and DTC component together, the generated code build might fail due to some section address overlaps.

Console × X ↓ ↓ ↓ ↓ ↓ ↓	
CDT Build Console [LLVM_R7F100GCJxLA_case1]	
ld.lld: error: section .bss virtual address range overlaps with .dtc_vectortable	^
<pre>&gt;&gt;&gt; .dtc_vectortable range is [0xF9F00, 0xF9F27]</pre>	
ld.lld: error: section .bssf virtual address range overlaps with .dtc_controldata_0	
<pre>&gt;&gt;&gt; .dtc_controldata_0 range is [0xF9F40, 0xF9F47]</pre>	
ld.lld: error: section .bss load address range overlaps with .dtc_vectortable >>> .bss range is [0xF9F00, 0xF9F31]	
<pre>&gt;&gt;&gt; .dtc_vectortable range is [0xF9F00, 0xF9F27]</pre>	
ld.lld: error: section .bssf load address range overlaps with .dtc_controldata_0 >>> .bssf range is [0xF9F32, 0xF9F7F]	
>>> .dtc_controldata_0 range is [0xF9F40, 0xF9F47]	
clang: error: ld.lld command failed with exit code 1 (use -v to see invocation)	
maketile:10: recipe for target 'LLVM_R/F100GCJXLA_Casel.eff' tailed make: *** [LLVM_R7F100GCJXLA_case1.elf] Error 1	
"make -j8 all" terminated with exit code 2. Build might be incomplete.	
18:09:07 Build Failed. 2 errors, 0 warnings. (took 1s.846ms)	

Figure 6-1 Build error message

#### [Workaround]

The Smart Configurator cannot set ".bss" and ".bssf" section address. So user should consider to modify ".bss" and ".bssf" section address manually in "linker\_script.ld" file or change the DTC base address to avoid such section overlap error.

Configure	
Base setting	
DTC base address	0xF9F00

Figure 6-2 DTC base address setting



## 6.2.2 Note on the installation of the Smart Configurator

Do not set more than 64 characters for the installation directory.

The user might see an error message "The specified path is too long" and will not be able to install Smart Configurator.

# 6.2.3 Note on using TRDIOA0 for Input capture and TRDIOB0 for Output compare at same time

If the user sets up TRDIOA0 for Input capture and TRDIOB0 for Output compare at the same time. Smart Configurator will output a Peripheral conflict error.

The user can ignore this Smart Configurator error message and use these two functions at the same time.

## 6.2.4 Note on pulse width calculation of Timer RD input capture function

The pulse width calculation code is with the assumption that the counter is not cleared between two interrupts occurrence, except the input pulse width which is selected as counter clear trigger on GUI. For example, when "Clear by TRDGRA*n* input capture" is selected, only TRDIOA*n* pulse width calculation handle counter clear, other input pulse width calculation doesn't handle counter clear.

nter setting	
nter clear	Clear by TRDGRA0 input capture
<pre>tatic voidnear r_Config_TRD0_trd0_interrupt uint16_t tmrd_pul_a_cur = TRDGRA0; uint16_t tmrd_pul_b_cur = TRDGR0; uint16_t tmrd_pul_c_cur = TRDGR00; uint16_t tmrd_pul_d_cur = TRDGRD0; uint8_t trdier0_temp = TRDIER0; TRDIER0 = 0x000; (/ unr51m_presser t/)</pre>	; (void)
<pre>/* OVEFILO PICOESS // UTRD_INTOV_GENERATE_FLAG) {     TRDSR0 &amp;=  uint8_t) ~_10_TRD_INTOV_GENER     g_tmrd0_ovf_a += 10;     g_tmrd0_ovf_b += 10;     g_tmrd0_ovf_c += 10;     g_tmrd0_ovf_d += 10; } /* TEDGEN0 ipput capture intervent */</pre>	== _10_TRD_INTOV_GENERATE_FLAG)
<pre>if ((TRDSR0 &amp; _01_TRD_INTA_GENERATE_FLAG) = {     TRDSR0 &amp;= (uint8_t)~_01_TRD_INTA_GENERA     if (0U == g_tmrd0_ovf_a)     {         g_tmrd0_active_width_a = (uint32_t)     }     else     {         g_tmrd0_active_width_a = (uint32_t)         g_tmrd0_active_width_a = (uint32_t)     } }</pre>	<pre>= _01_TRD_INTA_GENERATE_FLAG) TE_FLAG; tmrd_pul_a_cur; ((0x10000UL * (uint32_t)g_tmrd0_ovf_a) + (uint32_t)tmrd_pul_a_cur);</pre>
<pre>g_tmrd0_inactive_width_a = 0UL The p }</pre>	ulse width calculation handle counter clear.
<pre>/* TEDGERO input carture intertupt */ if ((TRDSRO &amp; _02_TRD_INTB_GENERATE_FLAG) = {     TRDSRO &amp;= (uint8_t)~_02_TRD_INTB_GENERA     if (OU == g_tmrd0_ovf_b)     {         g_tmrd0_active_width_b = (uint32_t)         }     else     {         g_tmrd0_active_width_b = (uint32_t)        </pre>	<pre>02_TRD_INTB_GENERATE_FLAG) TTE_FLAG; ((uint32_t)tmrd_pul_b_cur - (uint32_t)g_tmrd0_trdgrb_old); (((0x10000UL * (uint32_t)g_tmrd0_ovf_b) + (uint32_t)tmrd_pul_b_cur) 32_t)g_tmrd0_trdgrb_old);</pre>
g_tmrd0_inactive_width_b = 0UL; g_tmrd0_trdgrb_old = tmrh_e.pilese W	vidth calculation doesn't handle counter clear.

Figure 6-3 Counter clear setting in Input capture function



# 6.2.5 Note on the include path update issue when renaming the component's configuration name

When renaming the added component's configuration in e<sup>2</sup> studio Smart Configurator project that has selfdefined include path setting for any folder or file, include path setting for that folder or file will keep the old name setting after code generation. This will cause build error when compiling the newly generated codes so please manually update the include path.

The folder or file which has self-defined include path setting can be recognized by checking the overlay icon

() on that folder or file. Below is an example on how to handle the include path update after renaming Compare Match Timer component configuration.



Figure 6-4 Interval Timer component configuration before renaming



Figure 6-5 The Interval Timer component configuration after renaming



## **Release Note**

🗐 Properties for Cor	nfig_ADC					×
	Paths and Symbols				⇔ ▼ ⇔	- 8
<ul> <li>Resource</li> <li>C/C++ Build</li> <li>C/C++ General</li> <li>Paths and Sym Preprocessor I Run/Debug Settir</li> </ul>	Configuration: Hardw	areDebug [Active] om build s 🤗 Source Locatio	] ~   on	Manage C	onfigurati	ons
	Languages GNU C GNU C++ Assembly Assembly	Include directorie \${TCINSTALL}, \$/\${ProjName}, \$/\${ProjName}, \$/\${ProjName}, \$/\${ProjName}, \$/\${ProjName}, \$/\${ProjName},	's /inc /src/smc_gen/r_bsp /src/smc_gen/r_config /src/smc_gen/Config_ADC /src/smc_gen/general /src/smc_gen/Config_TAU0_1		Add Edit Delet Export	e tUp
	<ol> <li>"Preprocessor Inclu Show built-in value Mport Settings</li> </ol>	de Paths, Macros e s SExport Setting	tc." property page may define additional	entries	Move D	own
< >> ?			updated after code re-g To avoid build error, ple "Config_TAU0_1" to "My	enerat ase m y_Con	tion. anuall ifig_TA	ly update \U0_1"

Figure 6-6 Include path setting for the "Config\_ADC" configuration

## 6.2.6 Note on TAU Input Signal High/Low level Measurement component

When using TAU Input Signal High/Low level Measurement component, after used noise filter function for TImn input pulse, please make sure the High/Low level width min value needs to be greater than two times the minimum value prompted on the UI.

For example, the High/Low level width min value is 0.032us (min value), when use noise filter function, the width min value should be 0.064us.

Clock setting		
Operation clock	СК00	$\sim$
Clock source	fCLK	$\sim$
(Clock frequency: 32000 kHz High-/low-leve	l width range: 0.032 (µs	s) ≤ TI00 ≤ 4.096 (ms))

Figure 6-7 High/Low level width min value



## 6.2.7 Note on CC-RL V1.12 C++ project

In CC-RL V1.12 or later C++ project, there are some dummy issues such as "EI()" in editor. However this is editor specification and does not affect the program operation. Please ignore it.

C Smart_Co	nfigurator_CPP_Example.cpp ×
2	* DISCLAIMER
19	
21	* File Name : Smart_Configurator_CPP_Example.cpp.
26	⊖ #ifdefcplusplus
27	extern "C" {
28	#endif
29	<pre>#include "r_smc_entry.h"</pre>
30	<pre> #ifdefcplusplus </pre>
31	}
32	#endif
33	
34	<pre>int main(void);</pre>
35	
36	⊖ int main(void)
37	l.
38	EI();
39	return 0;
40	}

Figure 6-8 CODAN issue in CC-RL V1.12 C++ project

## 6.2.8 Note on browsing "Release Notes" and "Tool News" URL from the help menu

For Smart Configurator for RL78 V1.4.0 or before version, "Release Notes" and "Tools News" in the help menu cannot access the correct URL. This issue has been fixed from this version. Please access the URL below directly for Smart Configurator for RL78 V1.4.0 or before version. Release Notes: <u>https://www.renesas.com/rl78-smart-configurator-release-note</u> Tool News: <u>https://www.renesas.com/rl78-smart-configurator-tn-notes</u>



Figure 6-9 Release Notes and Tool News in Smart Configurators

### 6.2.9 Note on using the user code protection feature

From Smart Configurator for RL78 V1.5.0 onwards, the user code protection feature will be supported for all Code Generation components. Please use the following specific tags to add user code when using the user code protection feature. If the specific tags do not match exactly, inserted user code will not be protected after the code generation.





## 6.2.10 Note on IAR build error when using SNOOZE Mode Sequencer (SMS) component

When using SNOOZE Mode Sequencer (SMS) component, if the following build error is met in IAR Embedded workbench, please check the build order setting in project [Options...] -> [Custom Build] page.

- 1) When using IAR Embedded workbench V5.10, select "Run before compiling/assembling" (refer to Figure 6-11)
- 2) When using IAR Embedded workbench V4.21, make "Run this tool before all other tools" checked (refer to Figure 6-12)

The above setting can eliminate this build error.

uild		
Messages	File	Line
Cleaning 1 files. r_bsp_common_jer.asm cstantups Conting_SMS.c Conting_SMS.c Tetal Error[Pre1696]: cannot open source file "Config_SMS_ASM.h" searched: "Ciccases\tempcasesVcp_temp_case\g23\g23\g23\g23\g232\tractsrc_gen/Config_SMS\" searched: "Ciccases\tempcasesVcp_temp_case\g23\g23\g23\g232\tractsrc_gen/genera\" searched: "Ciccases\tempcasesVcp_temp_case\g23\g23\g23\g232\g232\g232\g232\g232\g2	C\cases\tempcases\vcp_temp_case\g23\g23iar_20230321\src\smc_gen\Config_SMS\Config_SMS.c	38
Figure 6-1	10 IAR build error	

IU IAR Dulla errol

Category:			
General Options	]		
Static Analysis			
C/C++ Compiler			
Assembler	Custom Tool Co	onfiguration	
Output Converter			
Custom Build	Filename exte	nsions:	
Build Actions Linker	.smsasm		
Debugger COM Port	Command line	ə:	
E1	"C:\Program	Files (x86)\Renesas Electronics\SMS\bin\smsasm.e	xe" \$FI
E20	Output files (c	one per line):	
E2 Lite / E2 On-board E7-CLIBE	\$FILE_BPATH	\$.h	$\sim$
EZ-CUBE2			
Simulator			~
ТК	Additional inp	ut files (one per line):	
			^
			$\sim$
	Build order:	Automatic (based on input and output)	~
		Automatic (based on input and output)	
		Run before compiling/assembling	
		Kun before linking	

Figure 6-11 "Build order" setting of IAR Embedded workbench V5.10



Category:	
General Options	
Static Analysis	
C/C++ Compiler	
Assembler	Custom Tool Configuration
Output Converter	
Custom Build	Filename extensions:
Build Actions	smsasm
Linker	131130311
Debugger	Command line:
COM Port	"CA Designer Files (#86)) Barrass Electronics) CMC(his) annound #61
E1	C:\Program Files (xoo)\Refesas Electronics\Sivis\bin\smsasm.exe \$Fi
E2 E20	Output files (one per line):
E21 ite / E2 On-board	
FZ-CUBE	\$FILE_BPATH\$.n
EZ-CUBE2	
IECUBE	U
Simulator	
тк	Additional input files (one per line):
	A
	v
	Run this tool before all other tools
	Kun this tool before all other tools
	OK Carool
	UK Calicei

Figure 6-12 Custom build setting of IAR Embedded workbench V4.21

## 6.2.11 Note on A/D conversion time setting after performing [Change device] or [Change resource]

After performing [Change device] (for example, change from RL78/G23 to RL78/G24), the A/D conversion time setting can't be kept. The user should take note to reconfirm the conversion time setting as he wants.





Conversion time mode	Normal 1	~
Conversion time	184/fCLK	~

Figure 6-14 A/D conversion time setting

When changing resource, for example from RL78/G24 normal A/D and RL78/G24 advanced A/D, the A/D conversion time can't be kept.

✓ ➢ A/D converter			Conversion time setting		
> Chers	Generate co	ode	Please set fCLK not greater than	32MHz.	
> 🗁 I/O port > 📂 Communications	Change res	ource	Conversion time mode	Normal 1	~
	Remove		Conversion time		Ť

Figure 6-15 [Change resource] operation



## 6.2.12 Note on changing Hardware Debug Configuration on project generation wizard

When a target board (except custom) is selected during creating a new project, please don't change the Hardware Debug Configuration manually. The reason is that the Hardware Debug Configuration has be decided by target board automatically. The user setting can't be reflected into Smart Configurator.

Toolchain Set	tings	
Language:		
Toolchain:	Renesas CC-RL $\sim$	
Toolchain Ver	sion: v1.12.00 ~	
	Manage Toolchains	
Device Setting	35	Configurations
Target Board:	RL78G23-128p_FastPrototypingBoard	Create Hardware Debug Configuration
		COM Port (RL78)
Target Device	R7F100GSNxFB	
	Unlock Devices	Create Debug Configuration
Endian	: Little 🗸	RL/8 Simulator V
Project Type	· Default ·	Create Release Configuration
	- Donance -	

Figure 6-16 Select a target board when creating a project in e<sup>2</sup> studio

## 6.2.13 Note on Pin Number maybe wrong in [Pins] page when loading project

The Pin Number maybe wrong for SCL00, SDA00, SI00, SO00, SCK00 when the user loads a 48/52/64pin project. The user needs to re-assign these pins manually.

Pin Fur	Pin Function						
type fi	lter text (* =	any string,	? = any character)				
Ena	Function	PIOR	Assignment	Pin Number	Direct	Remarks	Comments
$\checkmark$	RxD0	PIOR06,	P16/ANI26/CCD00/TI01/TO01/I	/ 16	1	There is no software	
	SCK00	PIOR01	Not assigned	Not assigned	None		
	SCL00	PIOR01	Not assigned	Not assigned	None		
	SDA00	PIOR01	Not assigned	Not assigned	None		
	SI00	PIOR01	Not assigned	Not assigned	None		
$\checkmark$	SO00	PIOR01	Not assigned	/ -	0	There is no software	
	TxD0	PIOR06,	Not assigned	Not assigned	None		
	SSI00		Not assigned	Not assigned	None		

Figure 6-17 Pin Number maybe wrong in [Pins] page

# 6.2.14 Note on Pin assignment with PIOR maybe wrong in [Pins] page when changing device

After performing [Change device] (for example, change from RL78/G23 to RL78/F24), the Pin assignment with PIOR may change according to PIOR setting automatically. When it has pin conflict, Smart Configurator will output pin conflict message and doesn't change pin assignment automatically. The user needs to reassign these pins manually.

2 m Function							
type filter	text (* = any stri	ng, ? = any chara	cter)			All	$\sim$
Enabled	Function	PIOR	Assignment	Pin Number	Direction	Remarks	^
	🐼 RxD2	PIOR1	Not assigned	Not assigned	None	Component requires a pin	
	RxDA0		Not assigned	Not assigned	None		
	SCK00	PIOR1	Not assigned	Not assigned	None		
	SCK01		Not assigned	Not assigned	None		~
<							>

Figure 6-18 Pin assignment with PIOR maybe wrong in [Pins] page



## Smart Configurator for RL78 Plug-in in e<sup>2</sup> studio 2025-01

Smart Configurator for RL78 V1.12.0

## **Revision History**

Rev.	Section	Description
1.00	-	First edition issued



#### General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

#### 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

#### 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the reset process is supplied until the power reaches the level at which resetting is specified.

#### 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pullup power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

#### 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external oscillator while program execution is in progress, wait until the target clock signal is stable.

#### 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.)

#### 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

#### 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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