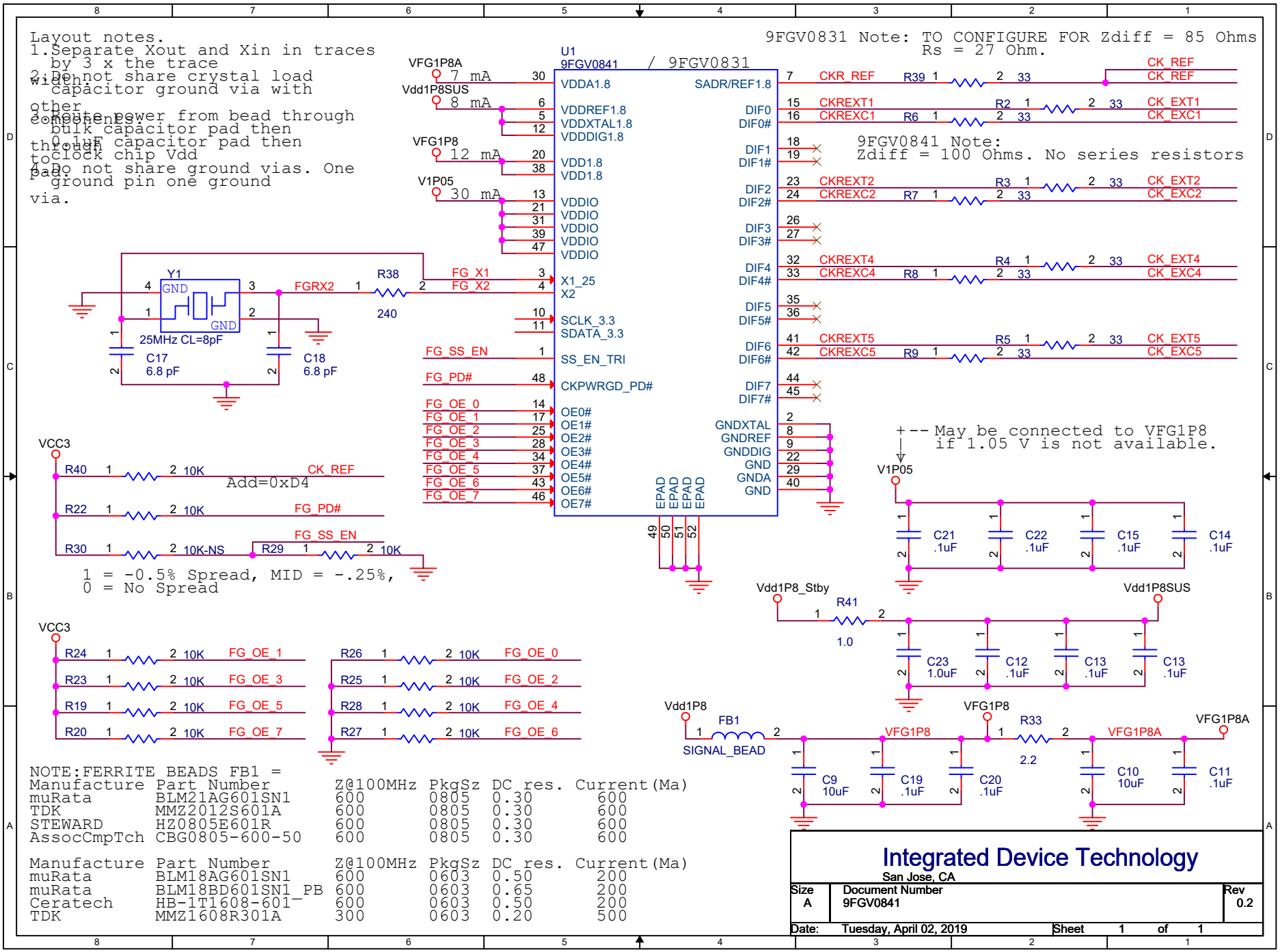
Layout notes.
1.Separate Xout and Xin in traces by 3 x the trace width.
2.Do not share crystal load capacitor ground via with other components.
3.Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.
4.Do not share ground vias. One ground pin one ground via.
9FGV0831 Note: TO CONFIGURE FOR Zdiff = 85 Ohms Rs = 27 Ohm.
U1
9FGV0841 / 9FGV0831
VFG1P8A
7 mA
Vdd1P8SUS
8 mA
VFG1P8
12 mA
V1P05
30 mA
VDDA1.8
VDDREF1.8
VDDXTAL1.8
VDDDIG1.8
VDD1.8
VDD1.8
VDDIO
VDDIO
VDDIO
VDDIO
VDDIO
X1_25
X2
SCLK_3.3
SDATA_3.3
SS_EN_TRI
CKPWRGD_PD#
OE0#
OE1#
OE2#
OE3#
OE4#
OE5#
OE6#
OE7#
SADR/REF1.8
DIF0
DIF0#
DIF1
DIF1#
DIF2
DIF2#
DIF3
DIF3#
DIF4
DIF4#
DIF5
DIF5#
DIF6
DIF6#
DIF7
DIF7#
GNDXTAL
GNDREF
GNDDIG
GND
GNDA
GND
EPAD
EPAD
EPAD
EPAD
CKR_REF
R39
33
CK_REF
CK_REF
CKREXT1
CKREXC1
R6
R2
CK_EXT1
CK_EXC1
9FGV0841 Note:
Zdiff = 100 Ohms. No series resistors
CKREXT2
CKREXC2
R7
R3
CK_EXT2
CK_EXC2
CKREXT4
CKREXC4
R8
R4
CK_EXT4
CK_EXC4
CKREXT5
CKREXC5
R9
R5
CK_EXT5
CK_EXC5
Y1
GND
GND
25MHz CL=8pF
FGRX2
R38
240
FG_X1
FG_X2
C17
6.8 pF
C18
6.8 pF
FG_SS_EN
FG_PD#
VCC3
R40
10K
CK_REF
Add=0xD4
R22
10K
FG_PD#
R30
10K-NS
R29
10K
FG_SS_EN
1 = -0.5% Spread, MID = -.25%,
0 = No Spread
+-- May be connected to VFG1P8
if 1.05 V is not available.
V1P05
C21
.1uF
C22
.1uF
C15
.1uF
C14
.1uF
Vdd1P8_Stby
R41
1.0
Vdd1P8SUS
C23
1.0uF
C12
.1uF
C13
.1uF
C13
.1uF
VCC3
R24
10K
FG_OE_1
R23
10K
FG_OE_3
R19
10K
FG_OE_5
R20
10K
FG_OE_7
R26
10K
FG_OE_0
R25
10K
FG_OE_2
R28
10K
FG_OE_4
R27
10K
FG_OE_6
Vdd1P8
FB1
SIGNAL_BEAD
VFG1P8
R33
2.2
VFG1P8A
C9
10uF
C19
.1uF
C20
.1uF
C10
10uF
C11
.1uF
NOTE:FERRITE BEADS FB1 =
Manufacture Part Number Z@100MHz PkgSz DC res. Current(Ma)
muRata BLM21AG601SN1 600 0805 0.30 600
TDK MMZ2012S601A 600 0805 0.30 600
STEWARD HZ0805E601R 600 0805 0.30 600
AssocCmpTch CBG0805-600-50 600 0805 0.30 600
Manufacture Part Number Z@100MHz PkgSz DC res. Current(Ma)
muRata BLM18AG601SN1 600 0603 0.50 200
muRata BLM18BD601SN1_PB 600 0603 0.65 200
Ceratech HB-1T1608-601 600 0603 0.50 200
TDK MMZ1608R301A 300 0603 0.20 500
Integrated Device Technology
San Jose, CA
Size
A
Document Number
9FGV0841
Rev
0.2
Date:
Tuesday, April 02, 2019
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