

DA1469x Reference Design

Design Name	2522-db-vfbga86
Ref. Number	331-19-D
Version	D
Date	11/Dec/2018
Designer	Panos Raftopoulos

History Table

Version	Date	Comments
A1.0	19/Mar/2018	Internal review release
A1.1	20/Mar/2018	Added pull-down resistor R24 to P1_1 Added options for DA14691/DA14695 - D9 single RED LED (D1 set as NP) - R25, R26 shorting LED pins to GND - R27, R28 shorting haptic driver pins to GND
A1.2	21/Mar/2018	Added RF filter option close to RFIOp (Z4,Z5,Z6) Changed L1 (DCDC inductor) to DFE201610E-R47M
	27/Mar/2018	Released for manufacturing
	10/Sep/2018	Added a current limiter mosfet on V30 (Q4) -> external loads now connect to the current-limited rail (V30x) Corrected the mismatch of the UART signals on J4 Added 0402 NP capacitor close to J3 pin-1 (C14)
B1.0	18/Sep/2018	Released for manufacturing
	04/Oct/2018	Changed R27, R28 to N.P. Changed C13 value to 2.2uF/25V Modified options for the QSPI flash package: - U2 --> 8SOIC 208mil - U2X --> 8USON 2x3mm - U2Y --> 8SOIC 150mil
C1.0	05/Oct/2018	Released to internal review
C1.1	15/Nov/2018	Changed ESD protection D7 D8 from ESD206B102ELSE6327XTSA1 (EOL) to ESD102U102ELSE6327XTSA1 (note: this part is polarized) Updated several parts as obsoleted/EOL and some with environmental compliance problems (K2, J3)
D1.0	11/Dec/2018	Added 0 ohm resistor (R29) shorting V18F to V18P Changed USB connector (J3) type to Molex 67503-1020 Changed default part# for 4.7uF capacitors to GRM155R61A475MEAAD

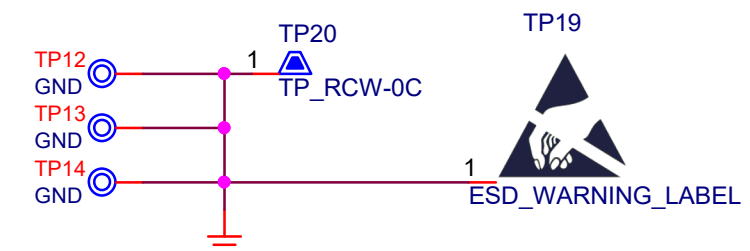
Configuration note

NOTE box

Changes in this Version.

—○ TP10 FIDUCIAL

—○ TP11 FIDUCIAL

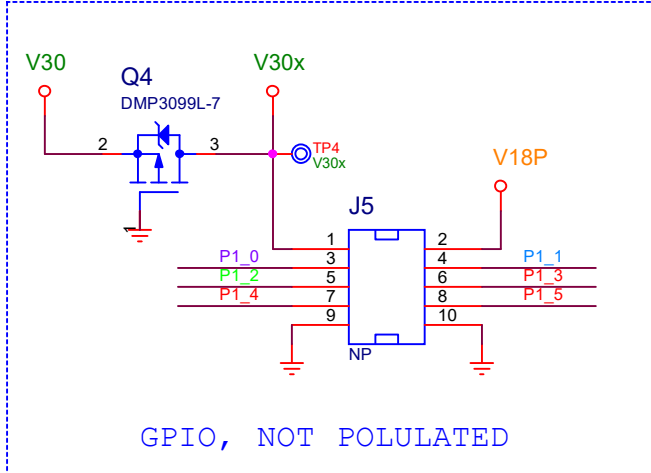
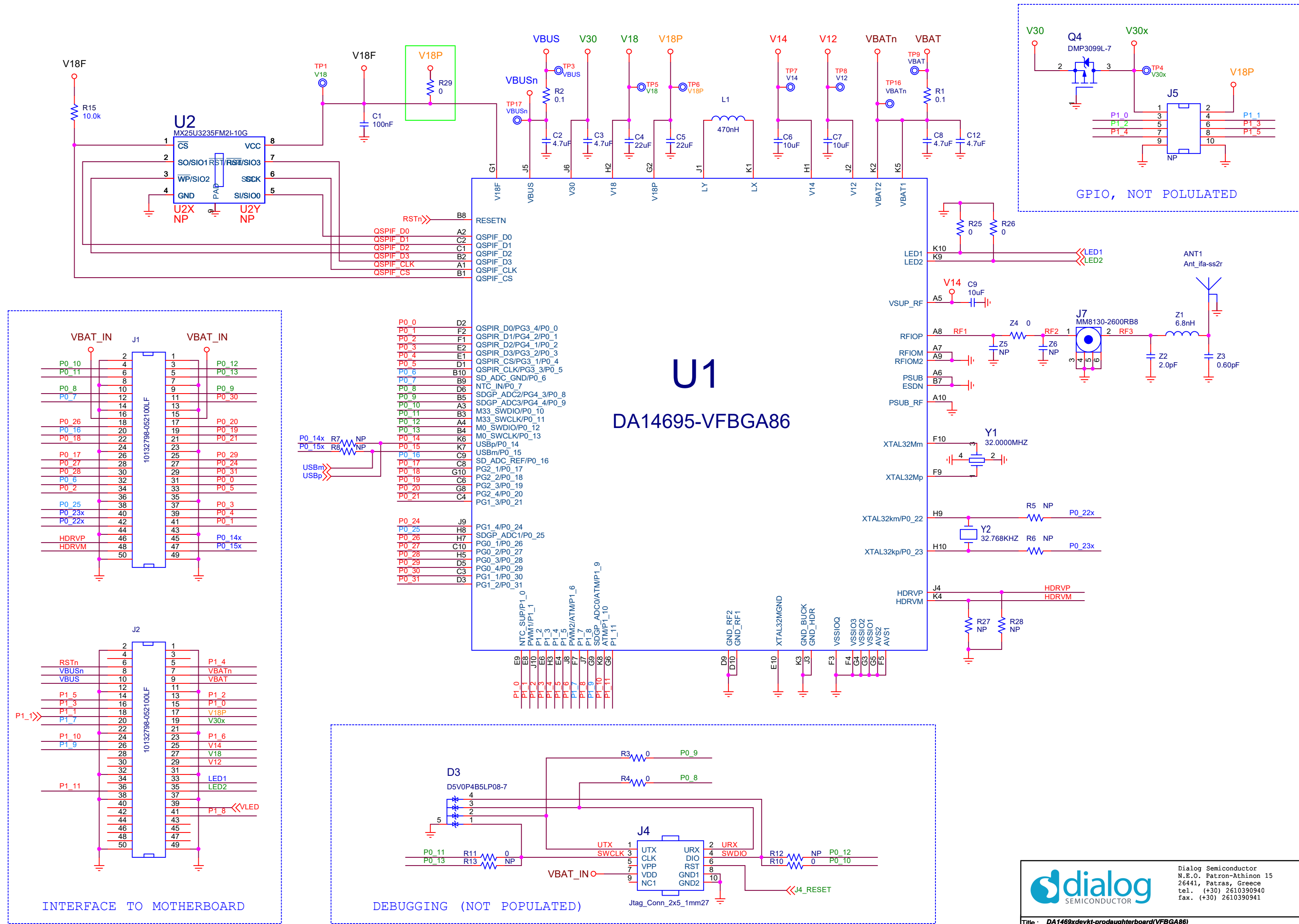


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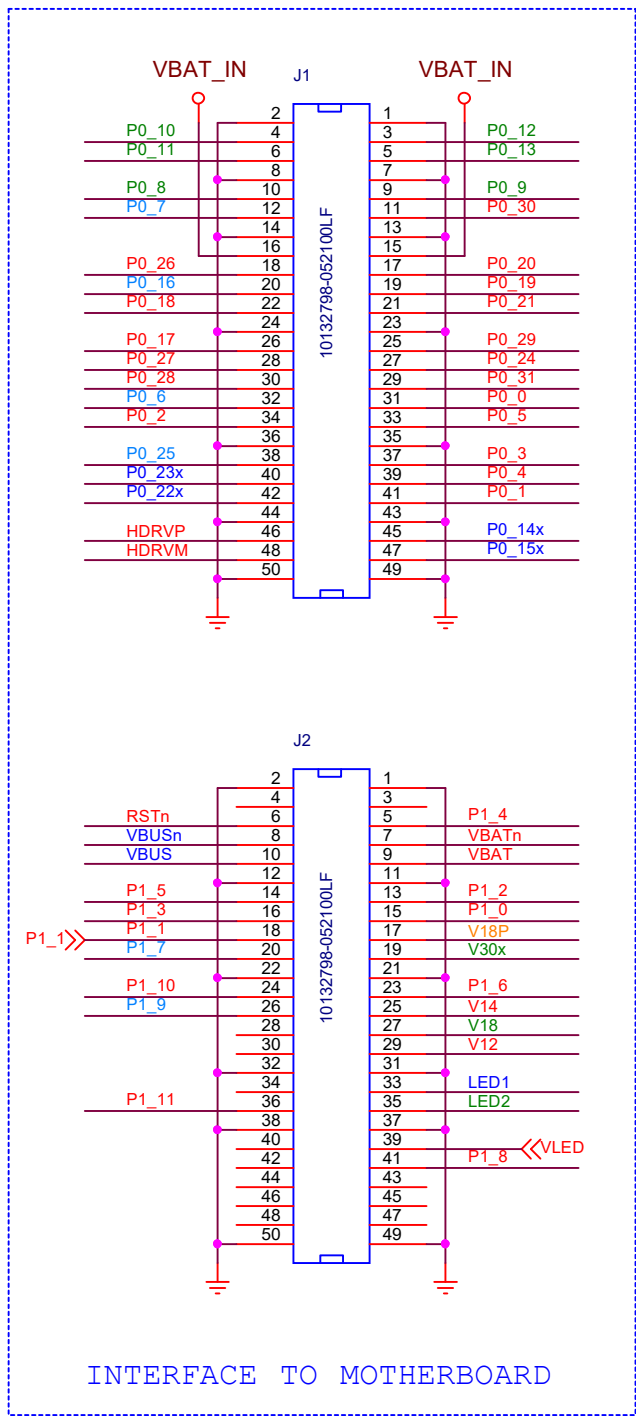
Title : DA1469x devkt-pro daughterboard (VFBGA86)

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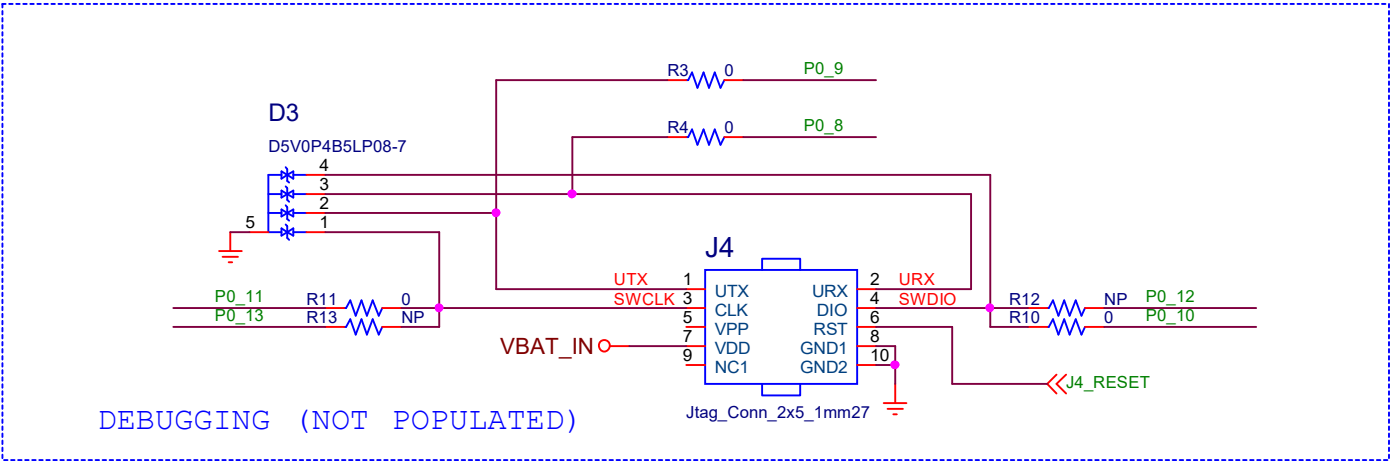
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GPIO, NOT POLULATED



INTERFACE TO MOTHERBOARD



DEBUGGING (NOT POPULATED)

P0_0	D2	QSPIR_D0/PG3_4/P0_0
P0_1	F2	QSPIR_D1/PG4_2/P0_1
P0_2	F1	QSPIR_D2/PG4_1/P0_2
P0_3	E2	QSPIR_D3/PG3_2/P0_3
P0_4	E1	QSPIR_CLK/PG3_1/P0_4
P0_5	D1	SD_ADC_GND/P0_6
P0_6	B10	NTC_IN/P0_7
P0_7	B9	SDGP_ADC2/PG4_3/P0_8
P0_8	D6	SDGP_ADC3/PG4_4/P0_9
P0_9	B5	M33_SWCLK/P0_10
P0_10	A3	M33_SWCLK/P0_11
P0_11	B3	M0_SWCLK/P0_12
P0_12	A4	M0_SWCLK/P0_13
P0_13	B4	USBp/P0_14
P0_14	K6	USBm/P0_15
P0_15	K7	SD_ADC_REF/P0_16
P0_16	C9	PG2_1/P0_17
P0_17	C8	PG2_2/P0_18
P0_18	G10	PG2_3/P0_19
P0_19	C6	PG2_4/P0_20
P0_20	G8	PG1_1/P0_21
P0_21	C4	PG1_2/P0_21
P0_24	J9	PG1_4/P0_24
P0_25	H8	SDGP_ADC1/P0_25
P0_26	H7	PG0_1/P0_26
P0_27	C10	PG0_2/P0_27
P0_28	H5	PG0_3/P0_28
P0_29	D5	PG0_4/P0_29
P0_30	C3	PG1_1/P0_30
P0_31	D3	PG1_2/P0_31
P1_0	E8	NTC_SUP/P1_0
P1_1	E8	PWM1/P1_1
P1_2	J10	P1_2
P1_3	E6	P1_3
P1_4	H3	P1_4
P1_5	E4	P1_5
P1_6	J8	P1_6
P1_7	F7	P1_7
P1_8	J7	P1_8
P1_9	G9	P1_9
P1_10	K8	SDGP_ADC0/ATMP1_9
P1_11	G6	ATMP1_10
P1_11	G6	ATMP1_11

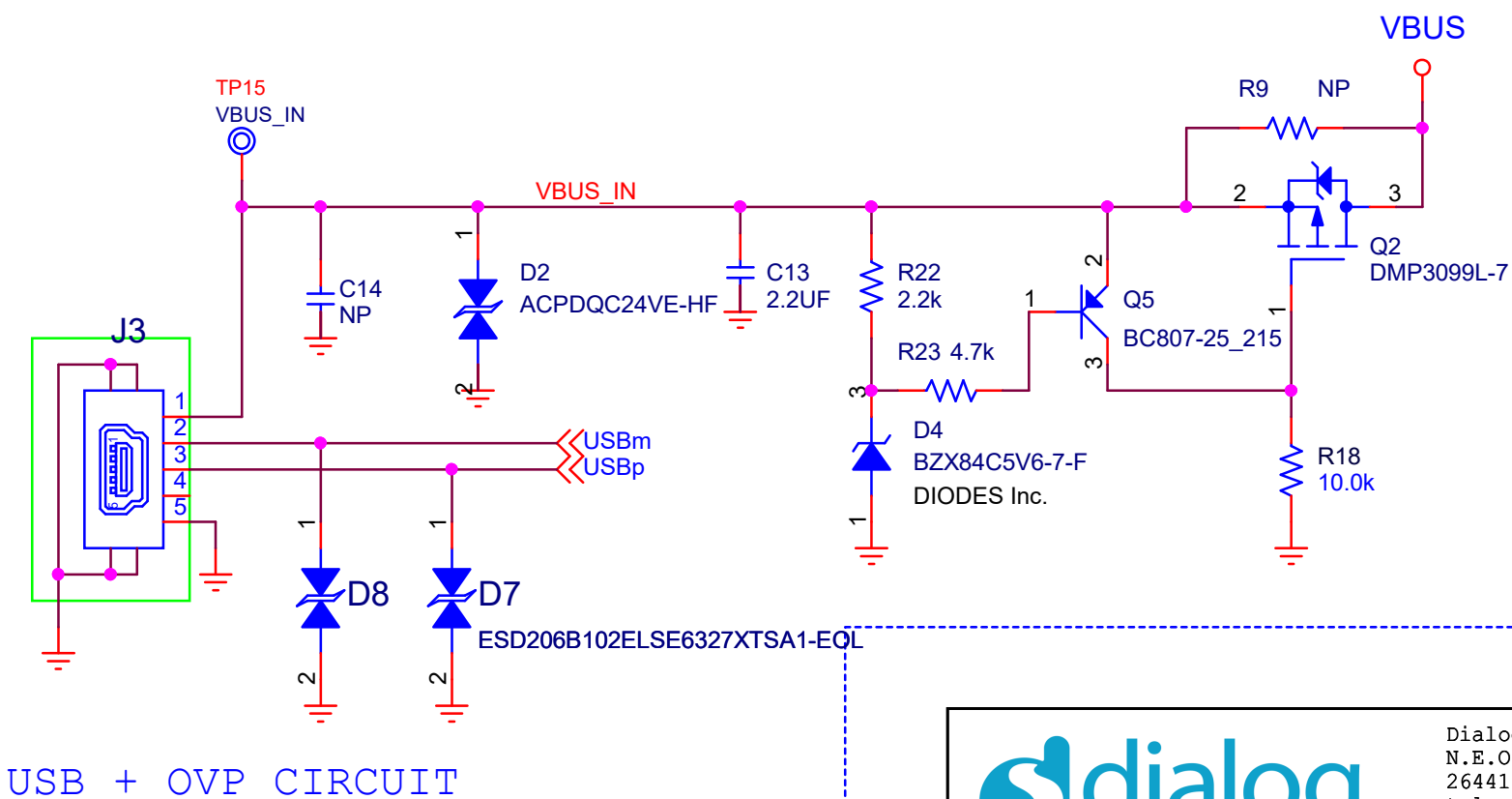
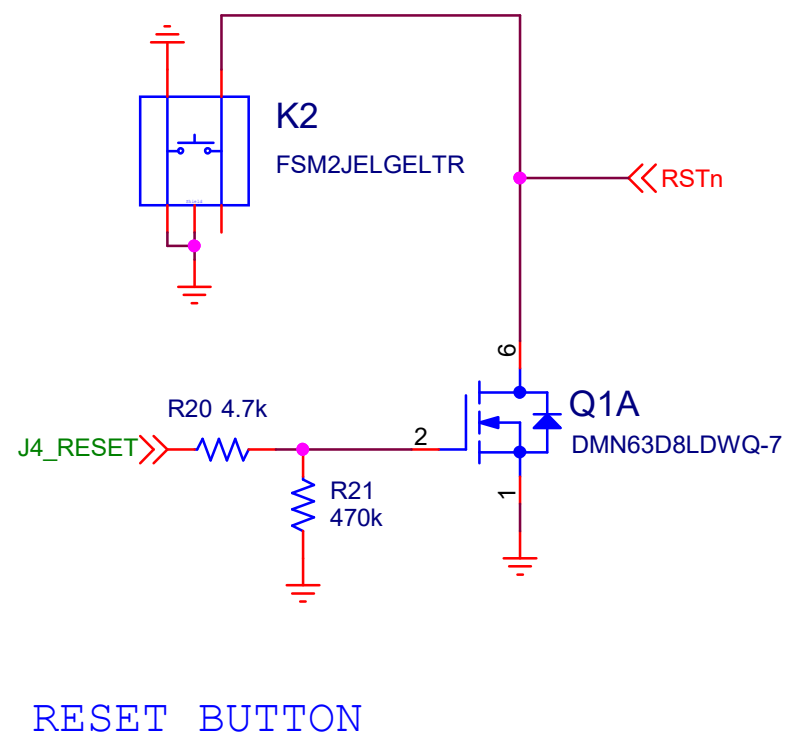
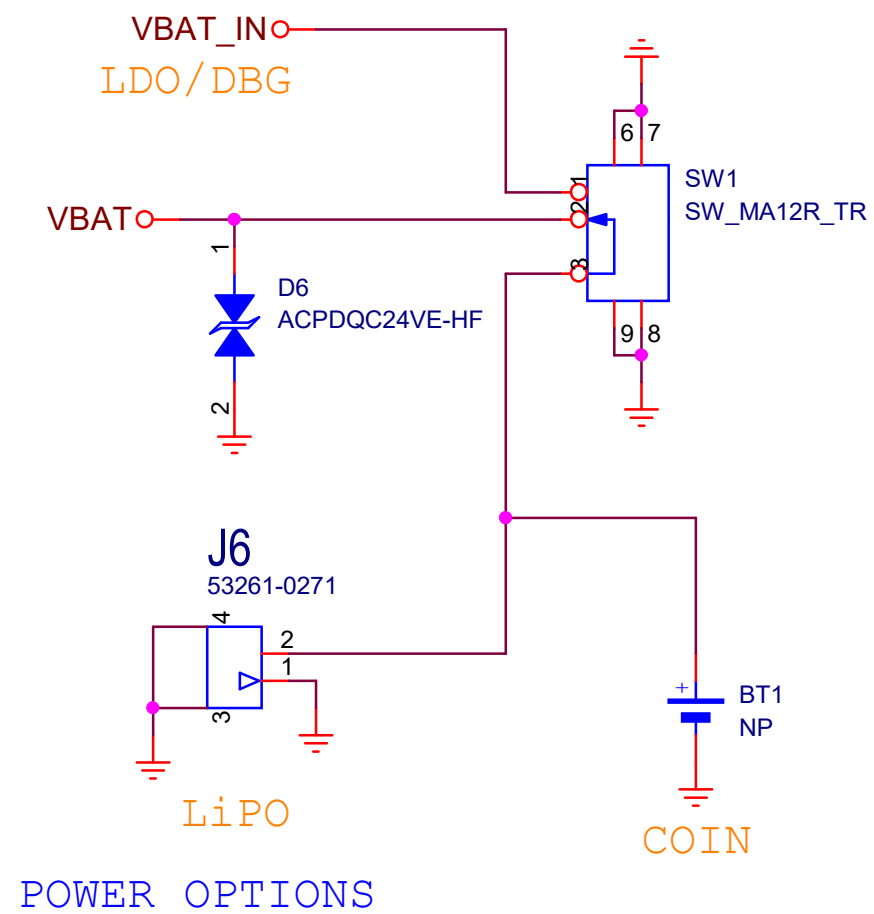
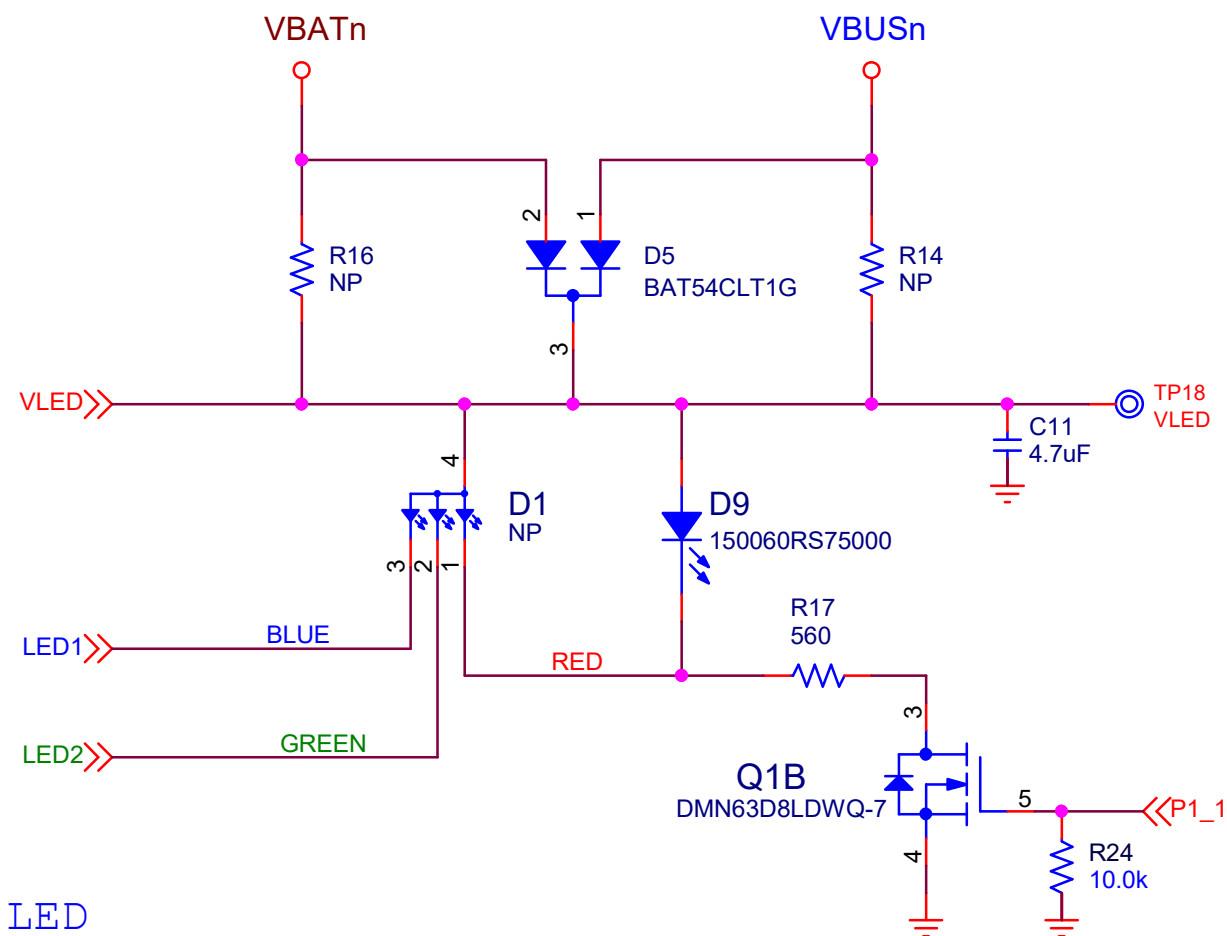
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