

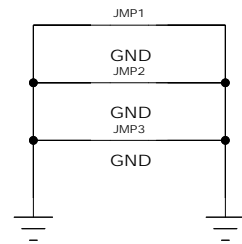
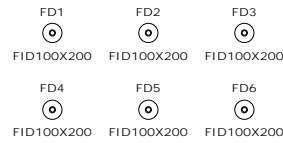
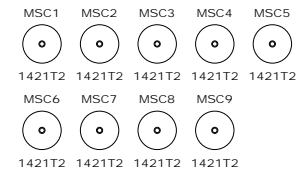
REVISION TABLE

REV.	DATE	ENGINEER	NOTES
A00	25/10/2016	GF/GC	Initial version based on 329-01-A EVB Solder.
A01	09/01/2017	GF	Added a clarifying note on page 1, explaining that C1M/C2M are used interchangeably with C1N/C2N.

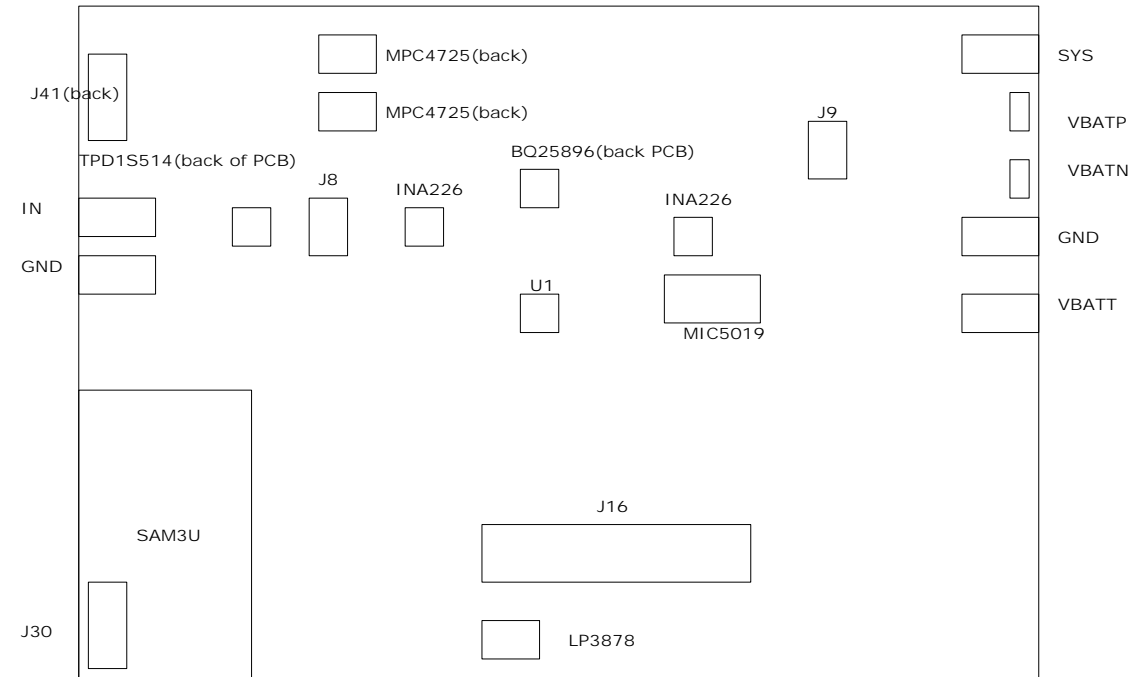
MECHANICAL PARTS

NOTE: C1M = C1N
C2M = C2N

MECHANICAL



LAYOUT NOTE: SPREAD GND LOOPS EVENLY AROUND THE BOARD.



SCHEMATIC TEMPLATE REV.xdxd_v3 (23-10-2015)

DESIGNED BY: Greg Fattig	CONFIDENTIAL	SIZE	TITLE:			
	INFORMATION	A3L	DA9318 System Reference Board			
	SAVED DATE:	25/02/2022	DRAWING NO:	329-03-A		REV:
REVIEWED BY: GF, ES	REVIEWED DATE:	12/20/2016	SHEET NAME:		PAGE:	1 of 8
			REVISION			

A

B

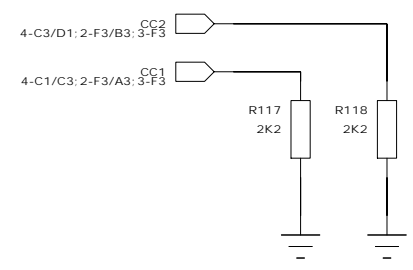
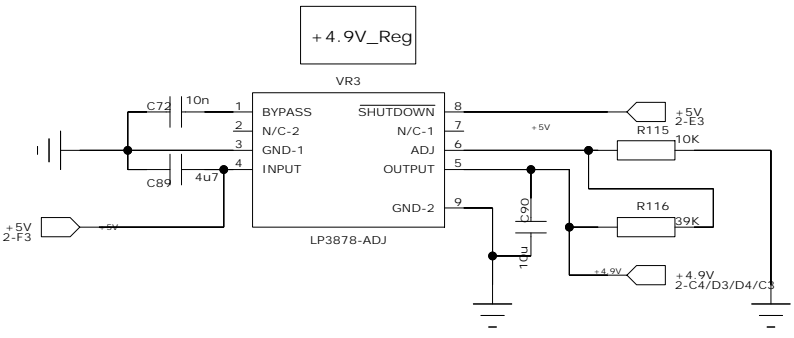
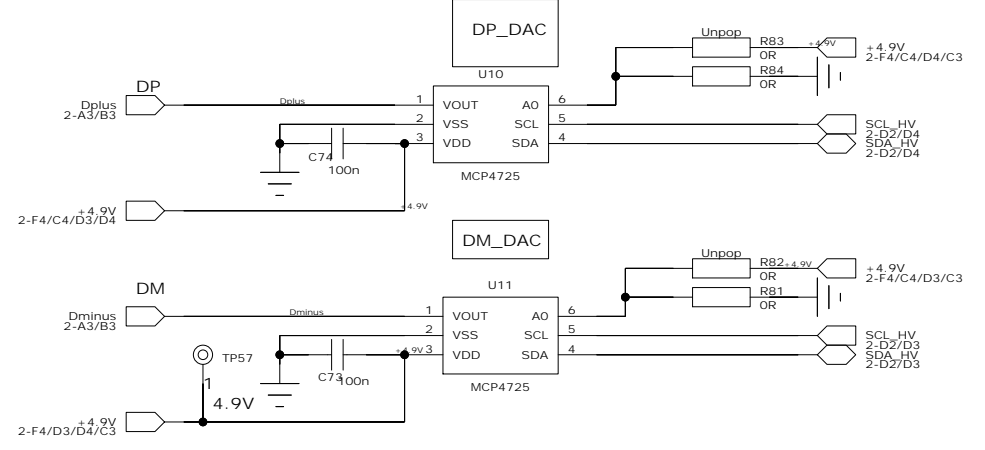
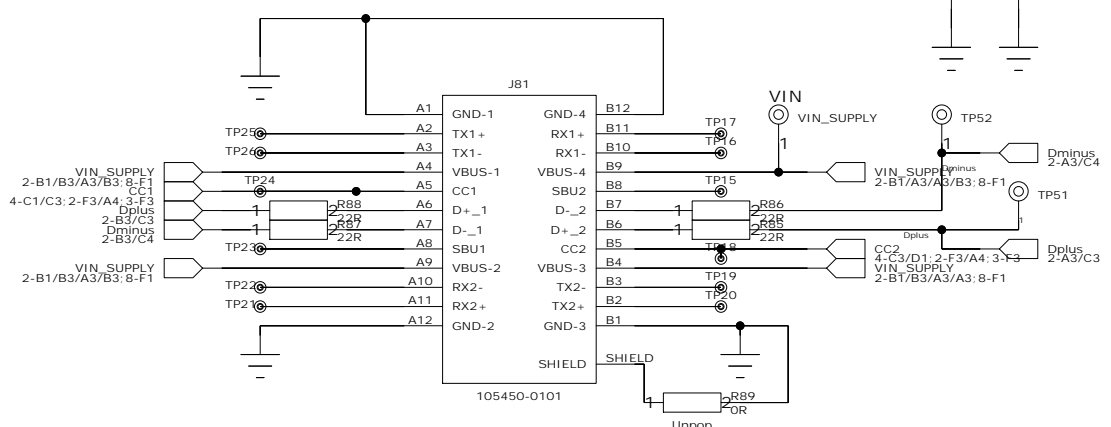
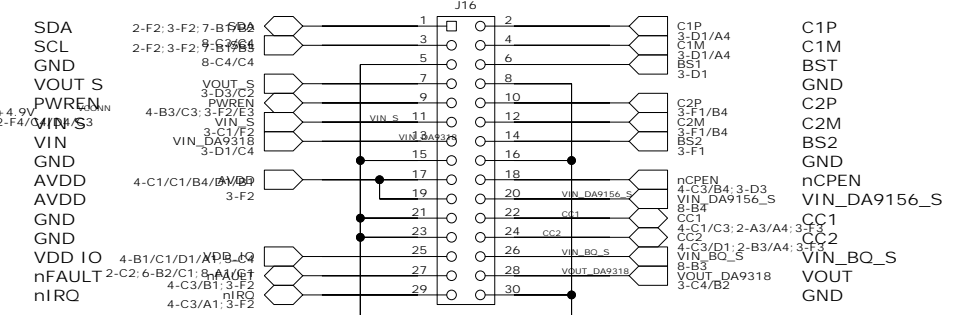
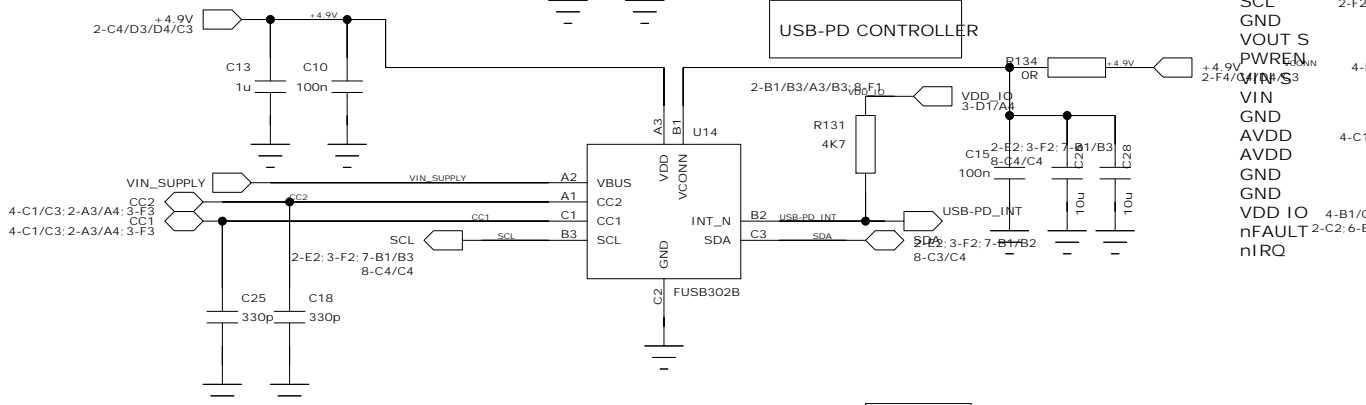
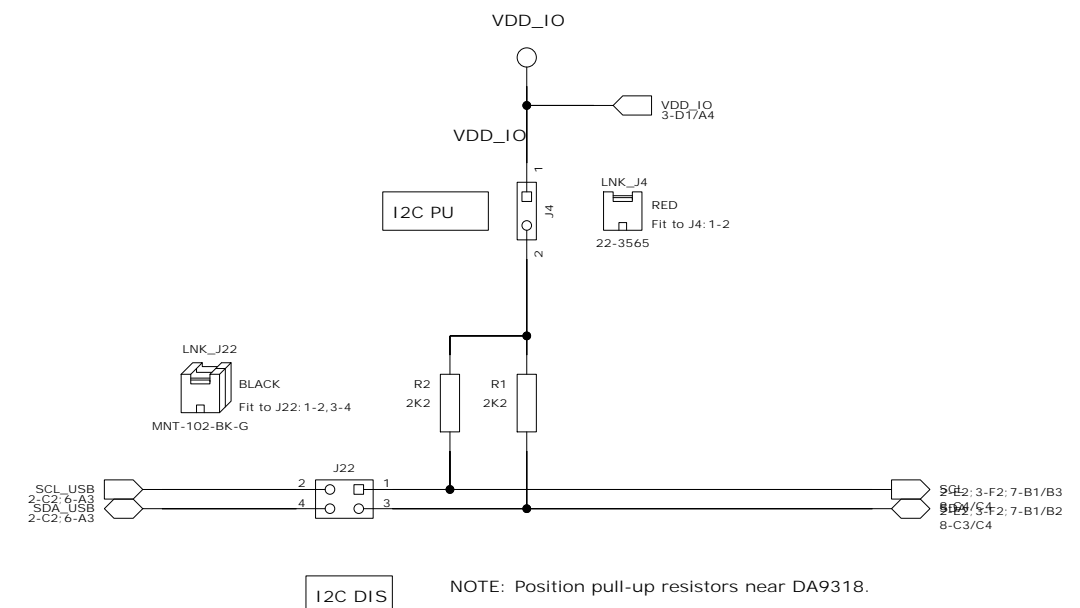
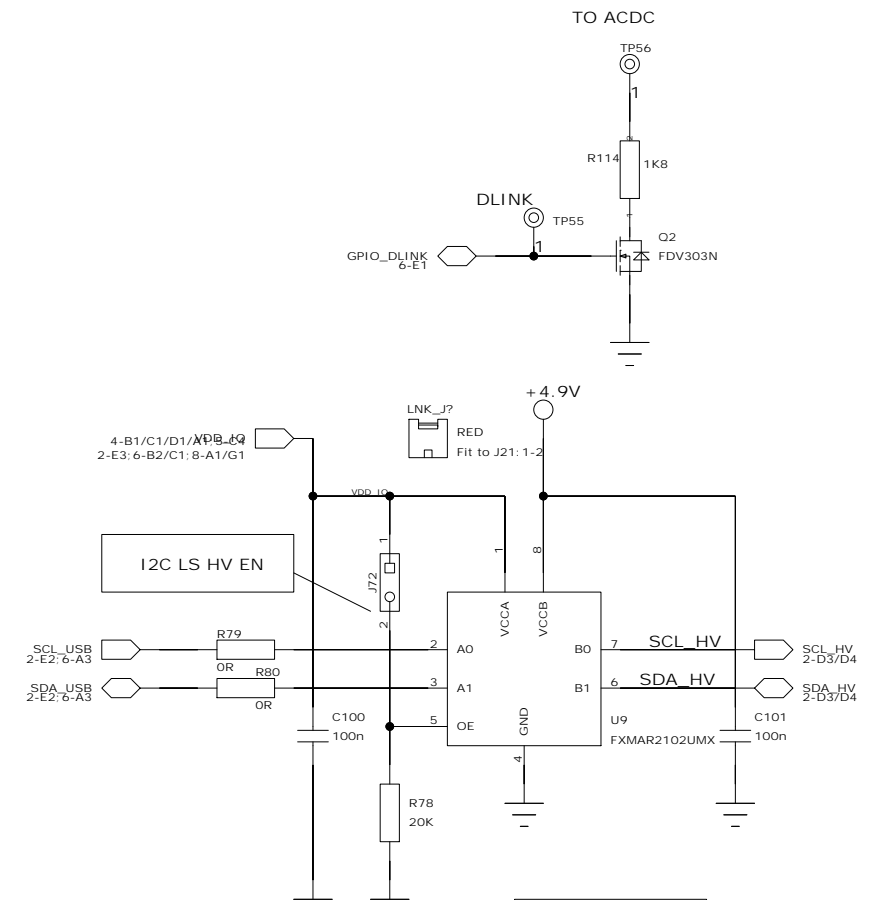
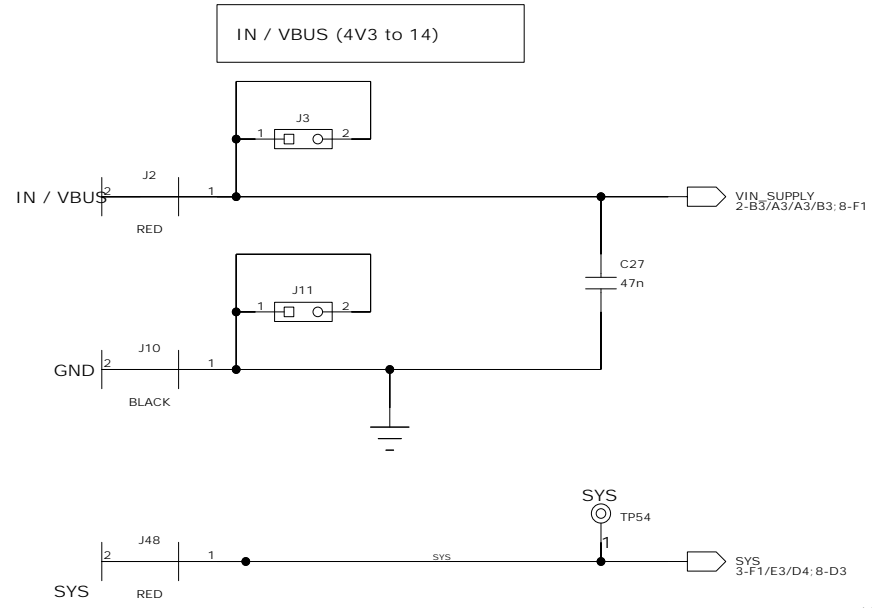
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E

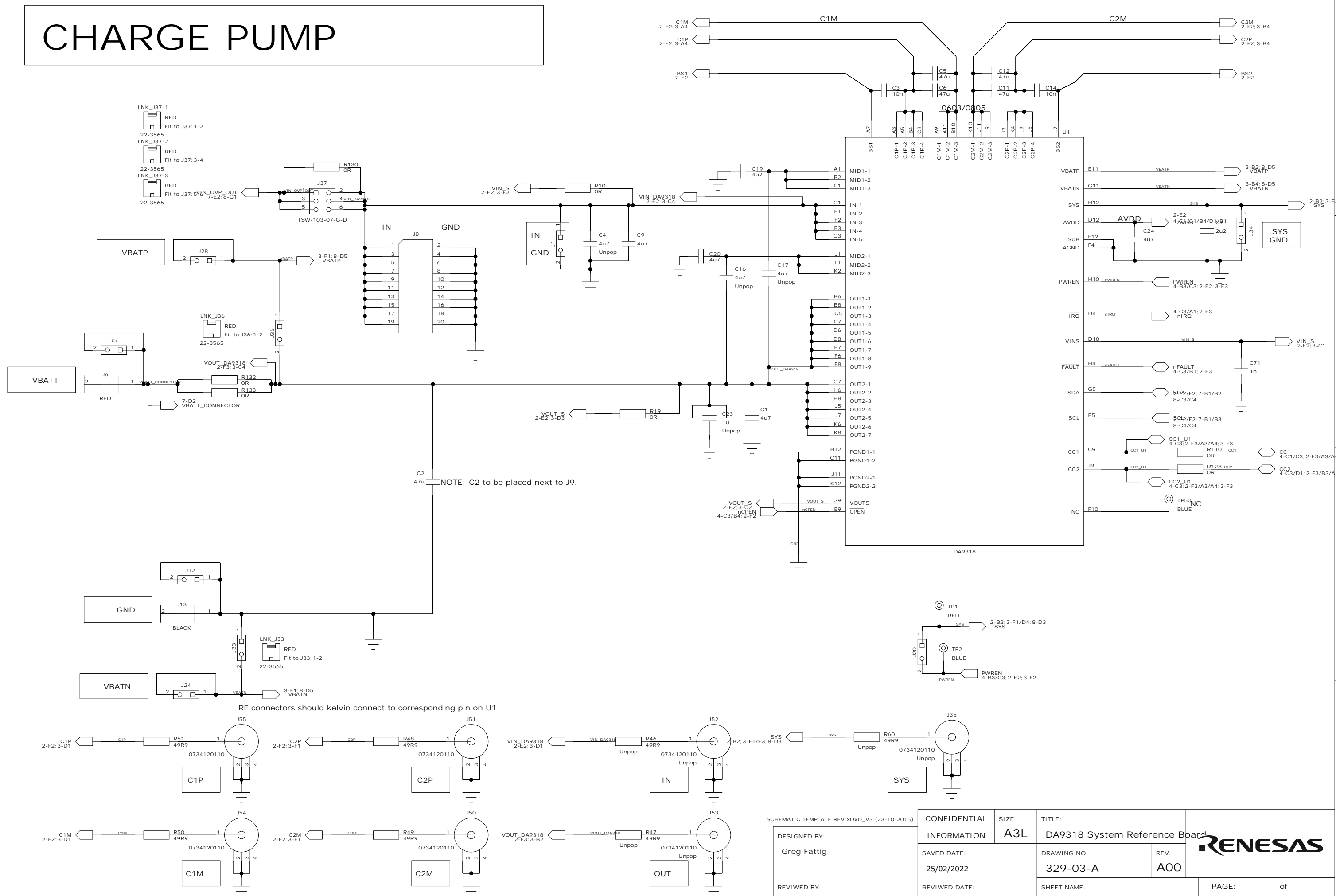
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POWER & IOs



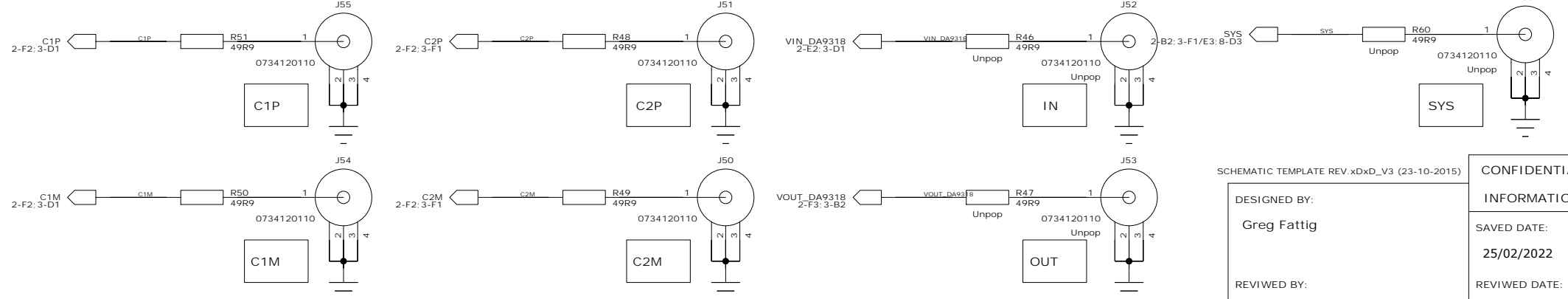
SCHEMATIC TEMPLATE REV. xDxD_V3 (23-10-2015)		CONFIDENTIAL	SIZE	TITLE:	
DESIGNED BY:	INFORMATION	A3L	DA9318 System Reference Board		
Greg Fattig	SAVED DATE:	25/02/2022	DRAWING NO:	329-03-A	
REVIWED BY:	REV:	A00	PAGE: 2 of 8		
GF, ES	REVIWED DATE:	12/20/2016	SHEET NAME:	POWER_AND_IOs	

CHARGE PUMP



NOTE: C2 to be placed next to J9.

RF connectors should kelvin connect to corresponding pin on U1



SCHEMATIC TEMPLATE REV. xDxD_V3 (23-10-2015)

DESIGNED BY:
Greg Fattig

REVIWED BY:
GF, ES

CONFIDENTIAL INFORMATION	SIZE A3L	TITLE: DA9318 System Reference Board		
	SAVED DATE: 25/02/2022	DRAWING NO: 329-03-A	REV: A00	
REVIWED DATE: 12/20/2016	SHEET NAME: CP		PAGE: 3	of 8

A

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1

1

2

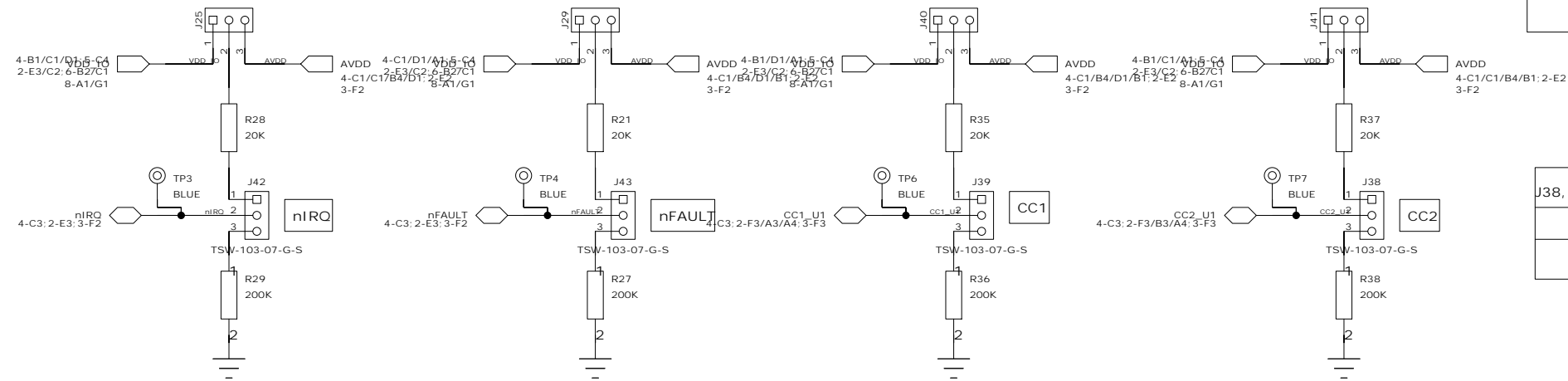
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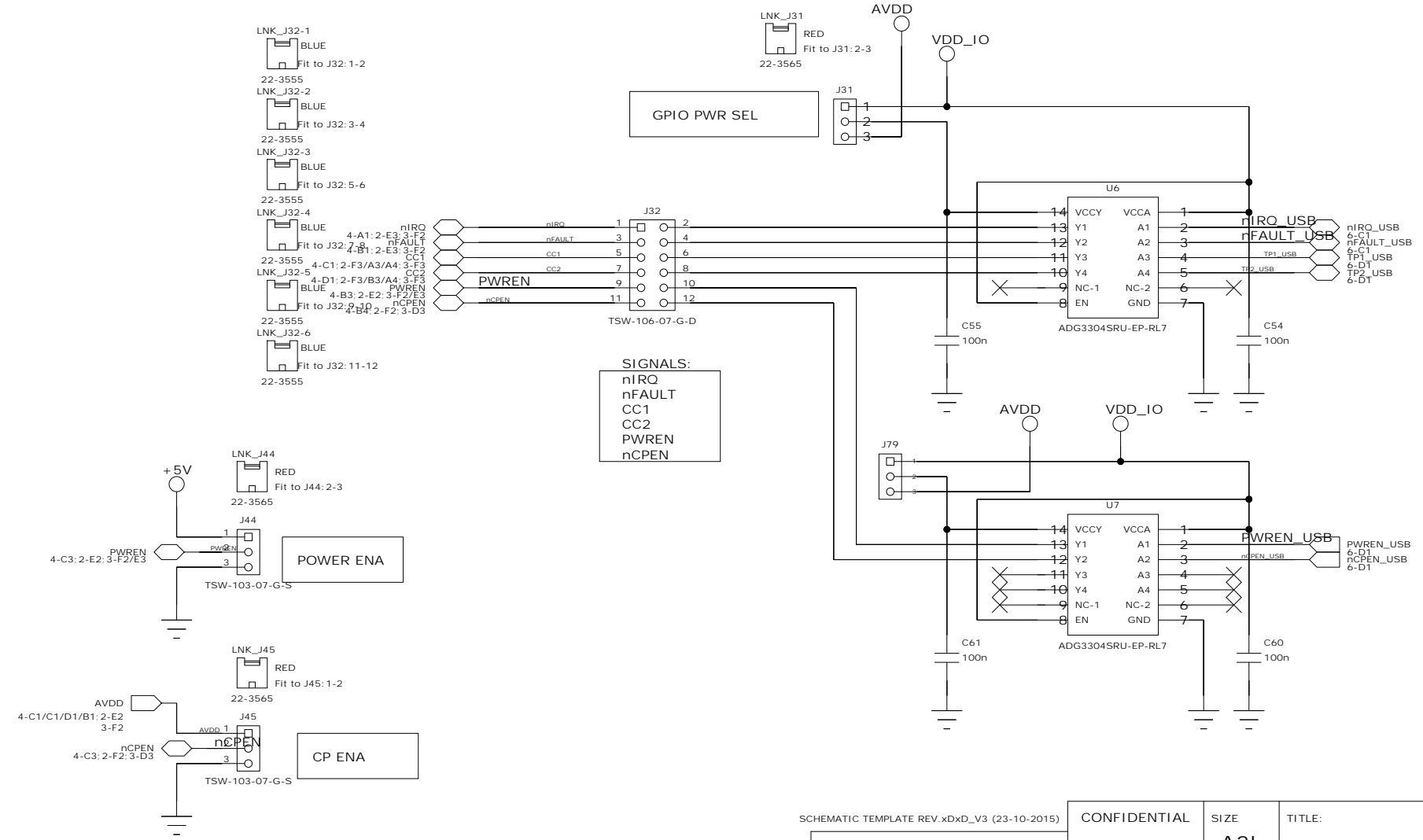
4

4



J25, J29, J40, J41	PU PWR SEL
1-2	VDD IO
2-3	AVDD

J38, J39, J42, J43	PU or PD select
1-2	Pull Up
2-3	Pull Down



SIGNALS:
 nIRQ
 nFAULT
 CC1
 CC2
 PWREN
 nCPEN

GPIOs

SCHEMATIC TEMPLATE REV. xDxD_V3 (23-10-2015)

DESIGNED BY:
 Greg Fattig

REVIEWED BY:
 GF, ES

CONFIDENTIAL INFORMATION	SIZE A3L	TITLE: DA9318 System Reference Board
SAVED DATE: 25/02/2022	DRAWING NO: 329-03-A	REV: A00
REVIEWED DATE: 12/20/2016	SHEET NAME: GPIOs	PAGE: 4 of 8



A

B

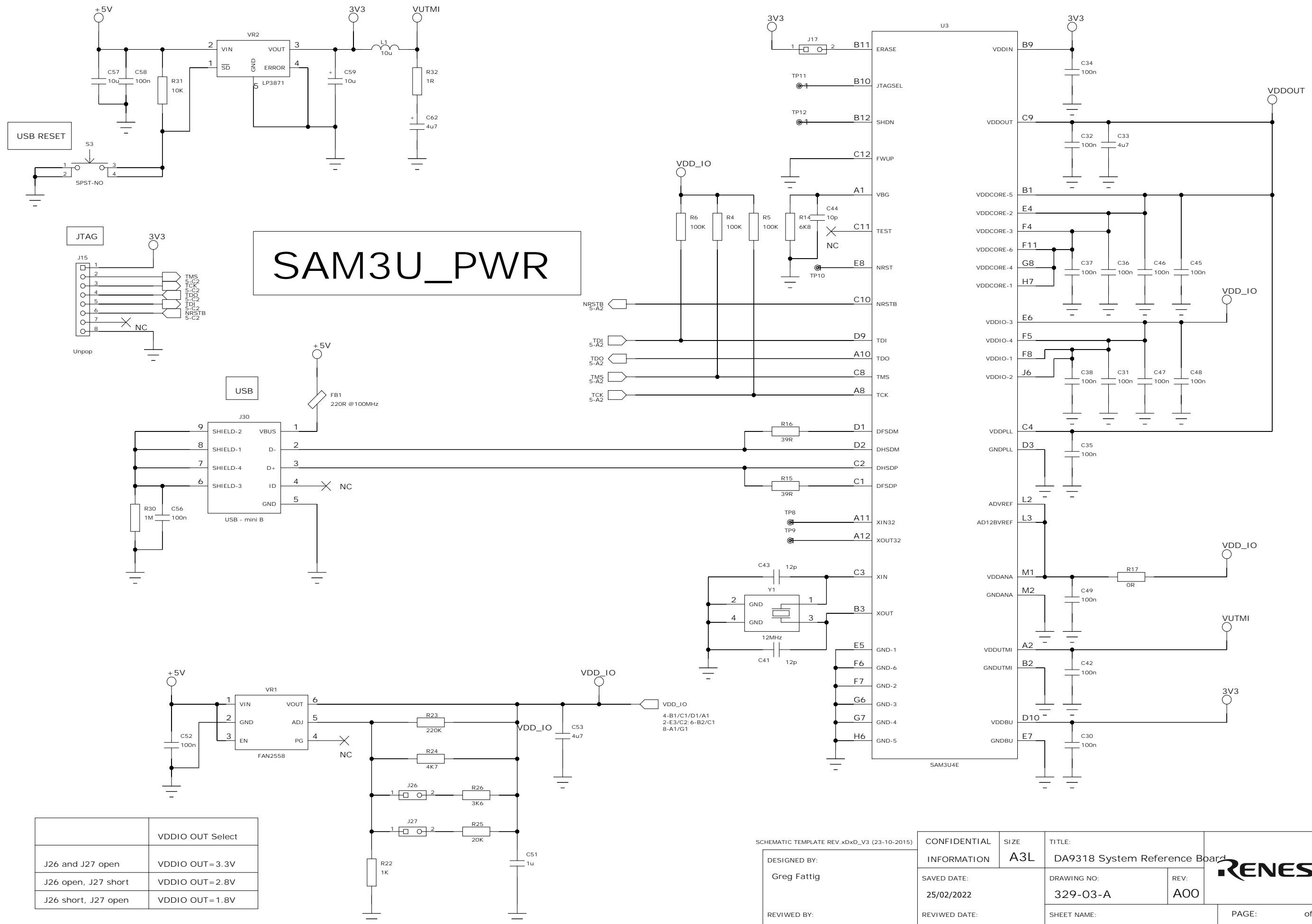
C

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E

F

SAM3U_PWR



	VDDIO OUT Select
J26 and J27 open	VDDIO OUT=3.3V
J26 open, J27 short	VDDIO OUT=2.8V
J26 short, J27 open	VDDIO OUT=1.8V

SCHEMATIC TEMPLATE REV. xDxD_V3 (23-10-2015)

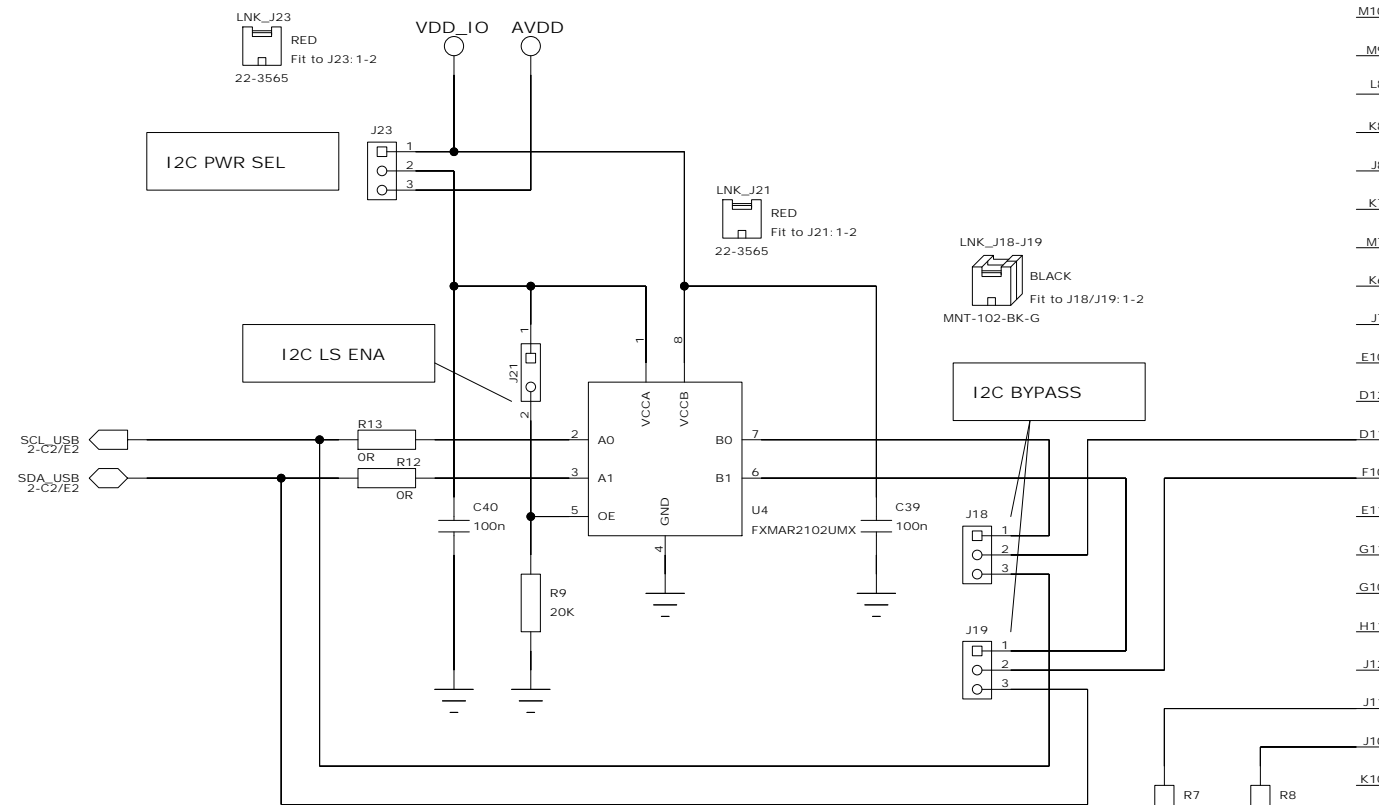
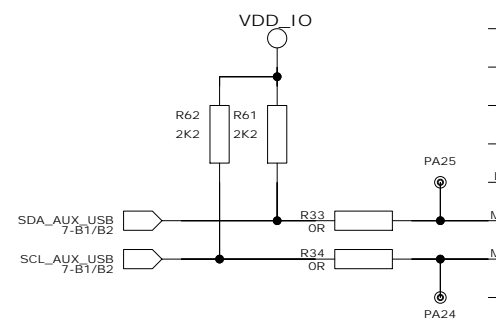
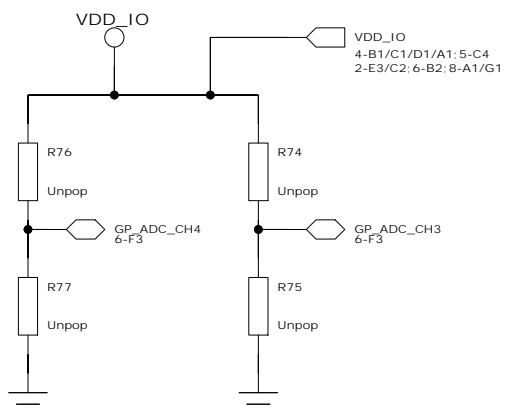
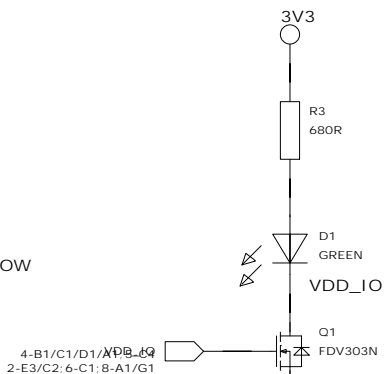
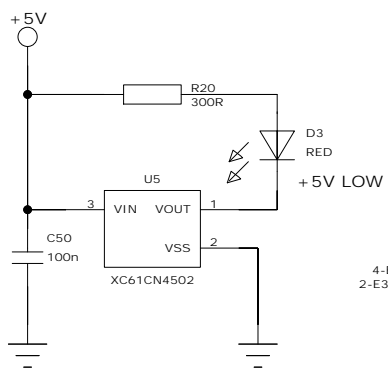
DESIGNED BY:
Greg Fattig

REVIEWED BY:
GF, ES

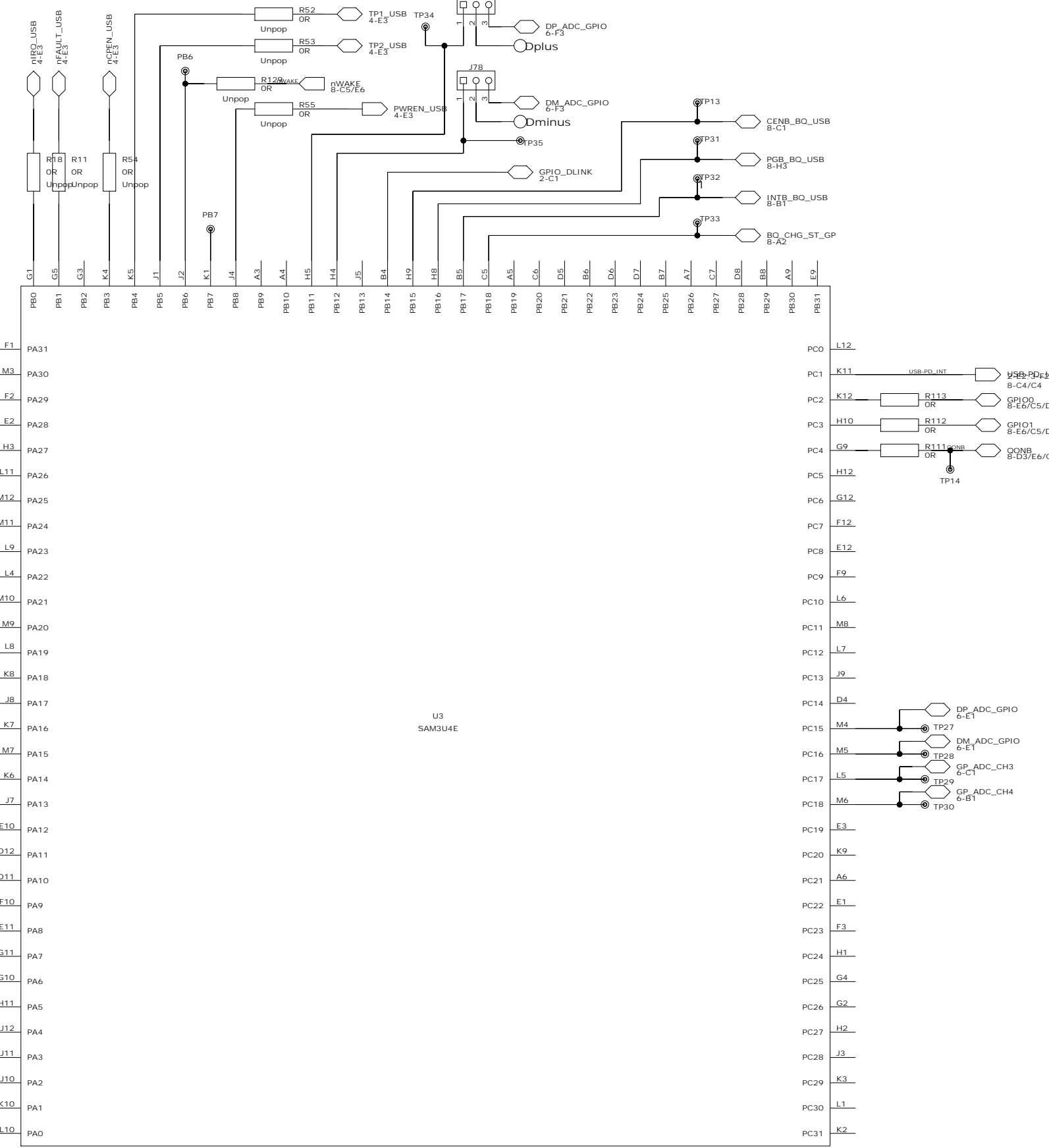
CONFIDENTIAL INFORMATION	SIZE A3L	TITLE: DA9318 System Reference Board
SAVED DATE: 25/02/2022	DRAWING NO: 329-03-A	REV: A00
REVIEWED DATE: 12/20/2016	SHEET NAME: USB_IF	PAGE: 5 of 8



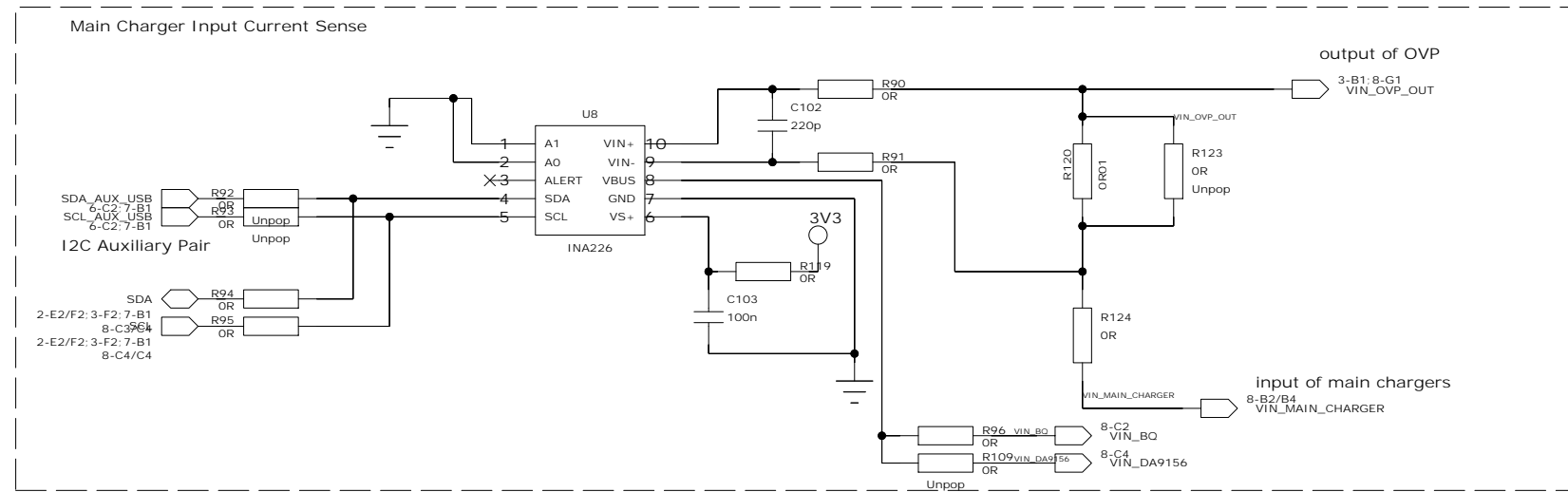
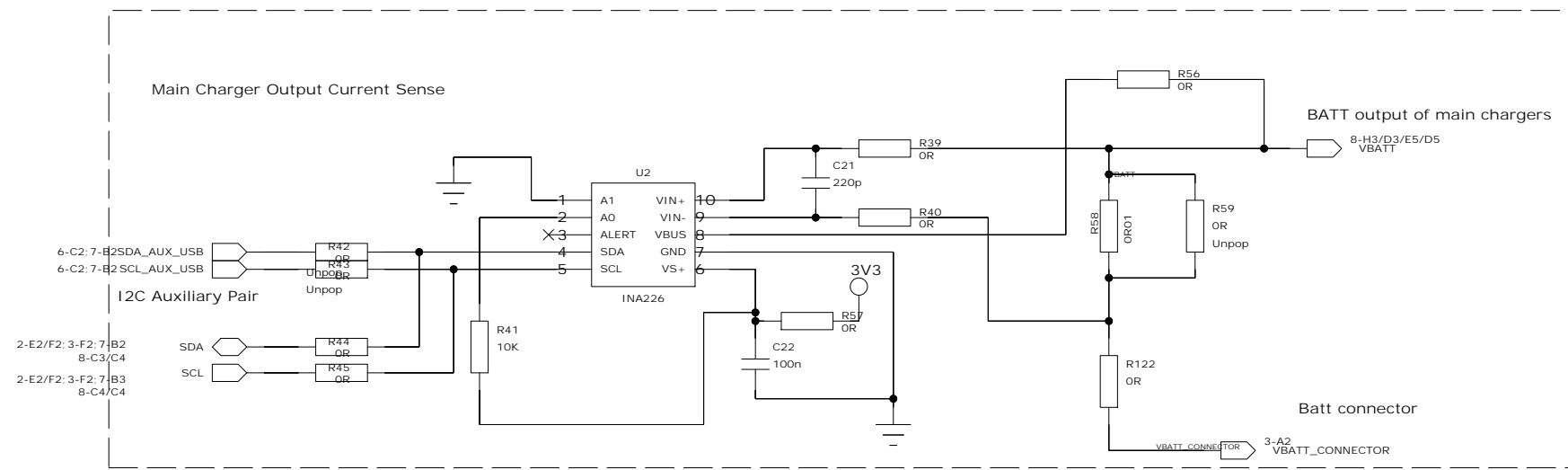
SAM3U_IOs



NOTE: Juxtapose J18 and J19 to allow the use of double link LNK_J18-J19.



SCHEMATIC TEMPLATE REV. xDxD_V3 (23-10-2015)		CONFIDENTIAL INFORMATION	SIZE: A3L	TITLE: DA9318 System Reference Board	
DESIGNED BY: Greg Fattig	SAVED DATE: 25/02/2022	DRAWING NO.: 329-03-A	REV.: A00	PAGE: 6 of 8	
REVIEWED BY: GF, ES	REVIEWED DATE: 12/20/2016	SHEET NAME: USB_LEVEL_SHIFTER			

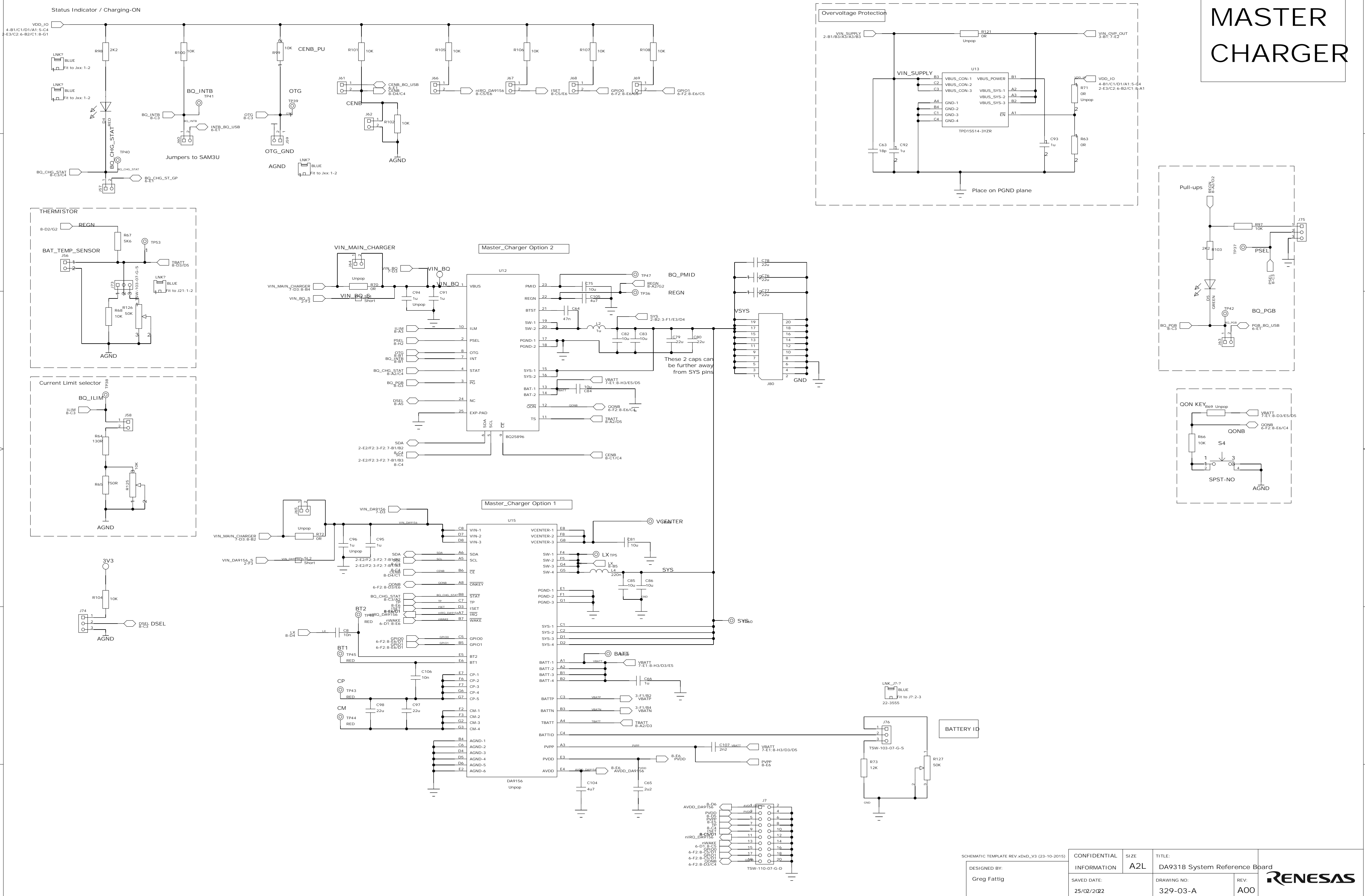


DA9318 has integrated current and voltage reporting

SCHEMATIC TEMPLATE REV. xDxD_V3 (23-10-2015)

DESIGNED BY: Greg Fattig	CONFIDENTIAL	SIZE A3L	TITLE: DA9318 System Reference Board		
	INFORMATION		DRAWING NO: 329-03-A	REV: A00	
REVIEWED BY: GF, ES	SAVED DATE: 25/02/2022	REVIEWED DATE: 12/20/2016	SHEET NAME: ISENSE		PAGE: 7 of 8

MASTER CHARGER



SCHEMATIC TEMPLATE REV.XDxD_V3 (23-10-2015)		CONFIDENTIAL	SIZE	TITLE:	
DESIGNED BY:	INFORMATION	A2L	DA9318 System Reference Board		
Greg Fattig	SAVED DATE:	25/02/2022	DRAWING NO:	REV:	RENESAS
REVIEWED BY:	12/20/2016	329-03-A	A00		
GF, ES	REVIEWED DATE:	12/20/2016	SHEET NAME:	PAGE:	of
			DA9156	8	8