

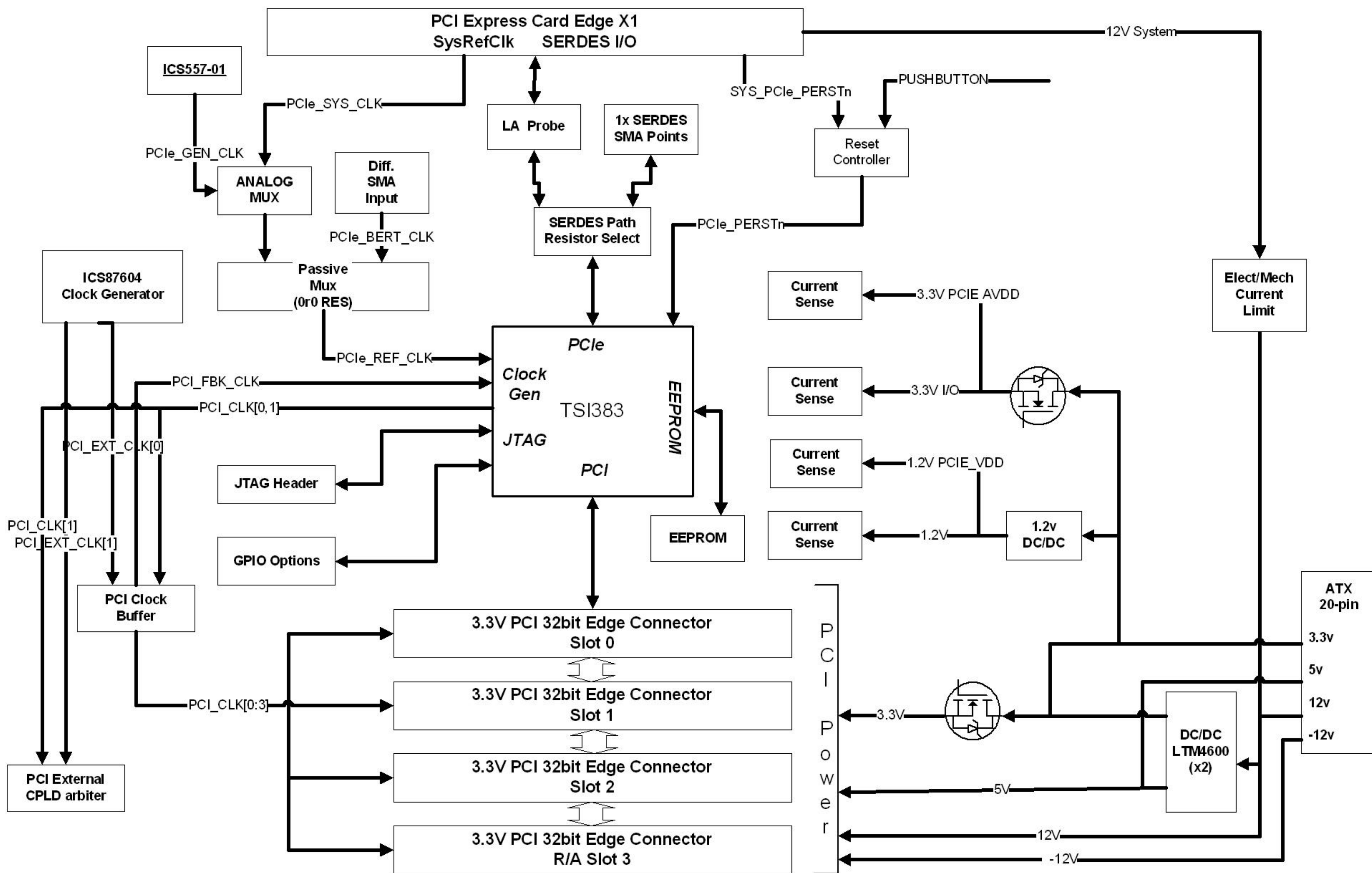
Tsi383 (QFN) Evaluation Board Schematics

TABLE OF CONTENTS

- PAGE 01 - Table of Contents
- PAGE 02 - Block Diagram
- PAGE 03 - Tsi383 PCIe/Misc
- PAGE 04 - PCIe Connectors
- PAGE 05 - Tsi383 PCI Interface
- PAGE 06 - PCI Slot 0 (R/A Top)
- PAGE 07 - PCI Slot 1 (Vertical)
- PAGE 08 - PCI Slot 3 (Vertical)
- PAGE 09 - PCI Slot 2 (Vertical)
- PAGE 10 - Clock Distribution
- PAGE 11 - Power Sources
- PAGE 12 - Tsi383 Power/Regulators
- PAGE 13 - PCI Regulators
- PAGE 14 - Test Devices
- PAGE 15 - Test Devices Cont'd

TITLE :			
TABLE OF CONTENTS			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	TBD	1.0	
LAST MODIFIED DATE :			SHEET
12-17-2009_15:26			1 OF 15

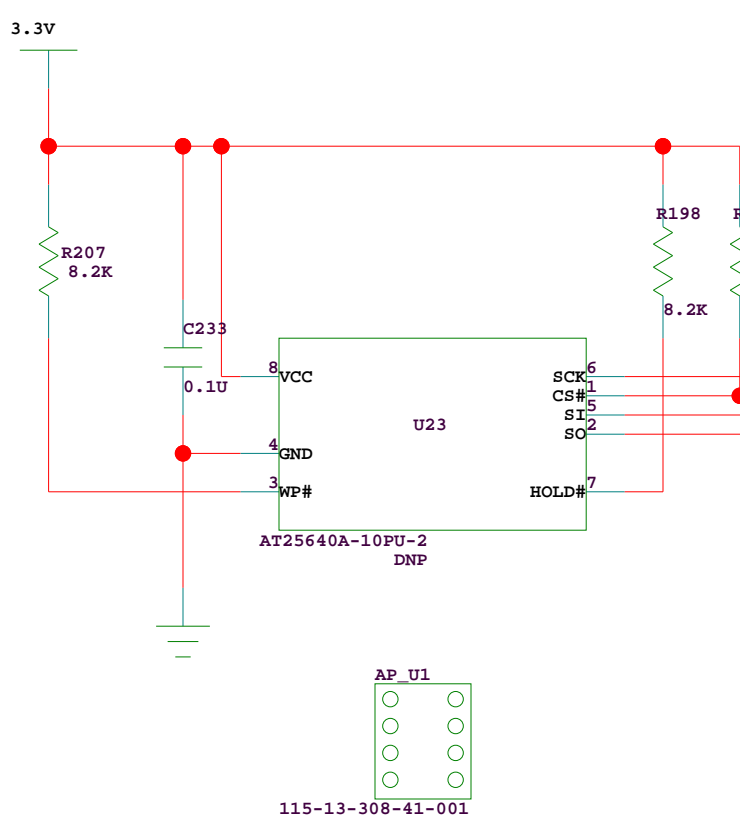
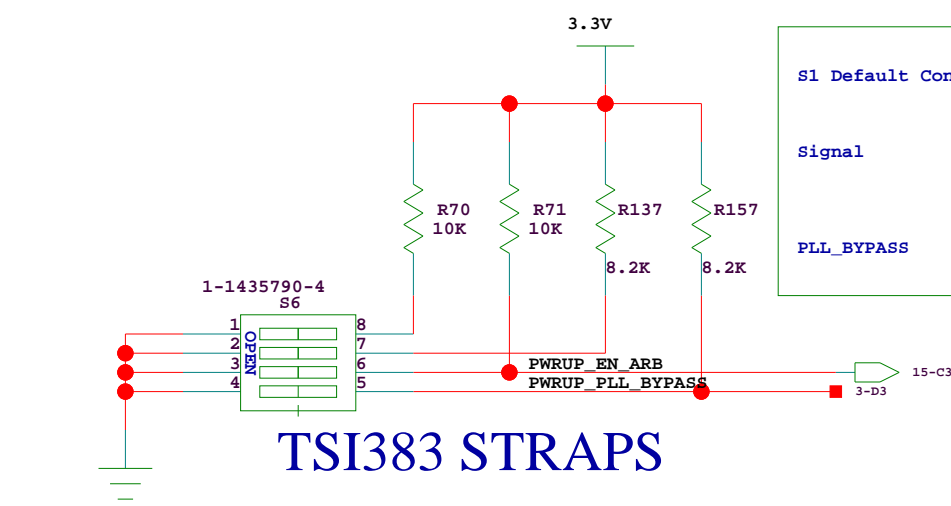
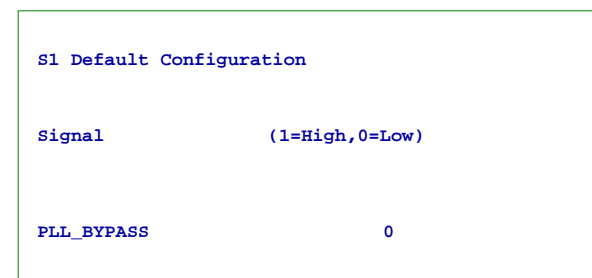
BLOCK DIAGRAM



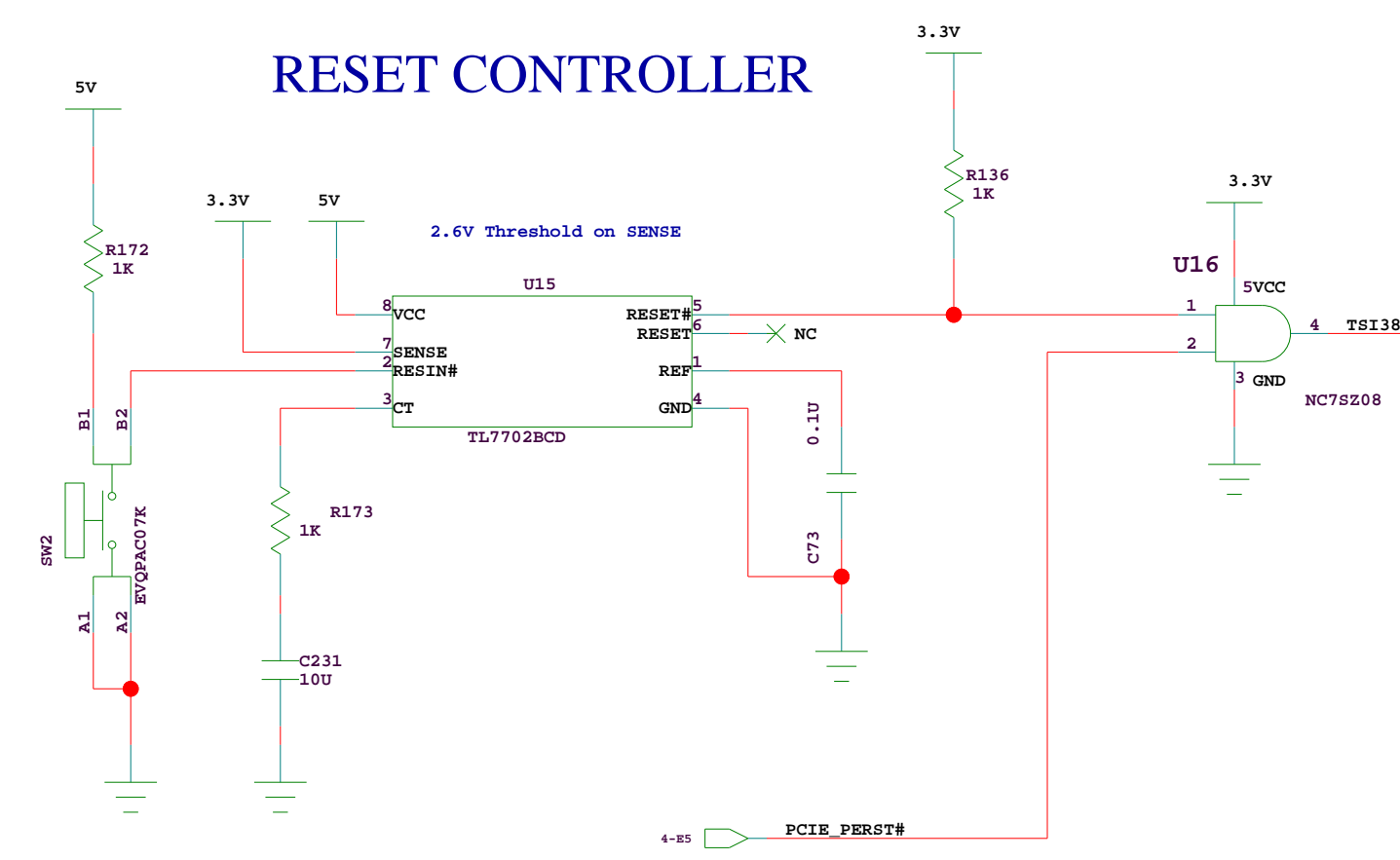
TITLE : BLOCK DIAGRAM			
SIZE C	DRAWING NUMBER : TBD	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 12-17-2009_15:26		SHEET 2 OF 15	

TSI383 PCIE/MISC INTERFACE

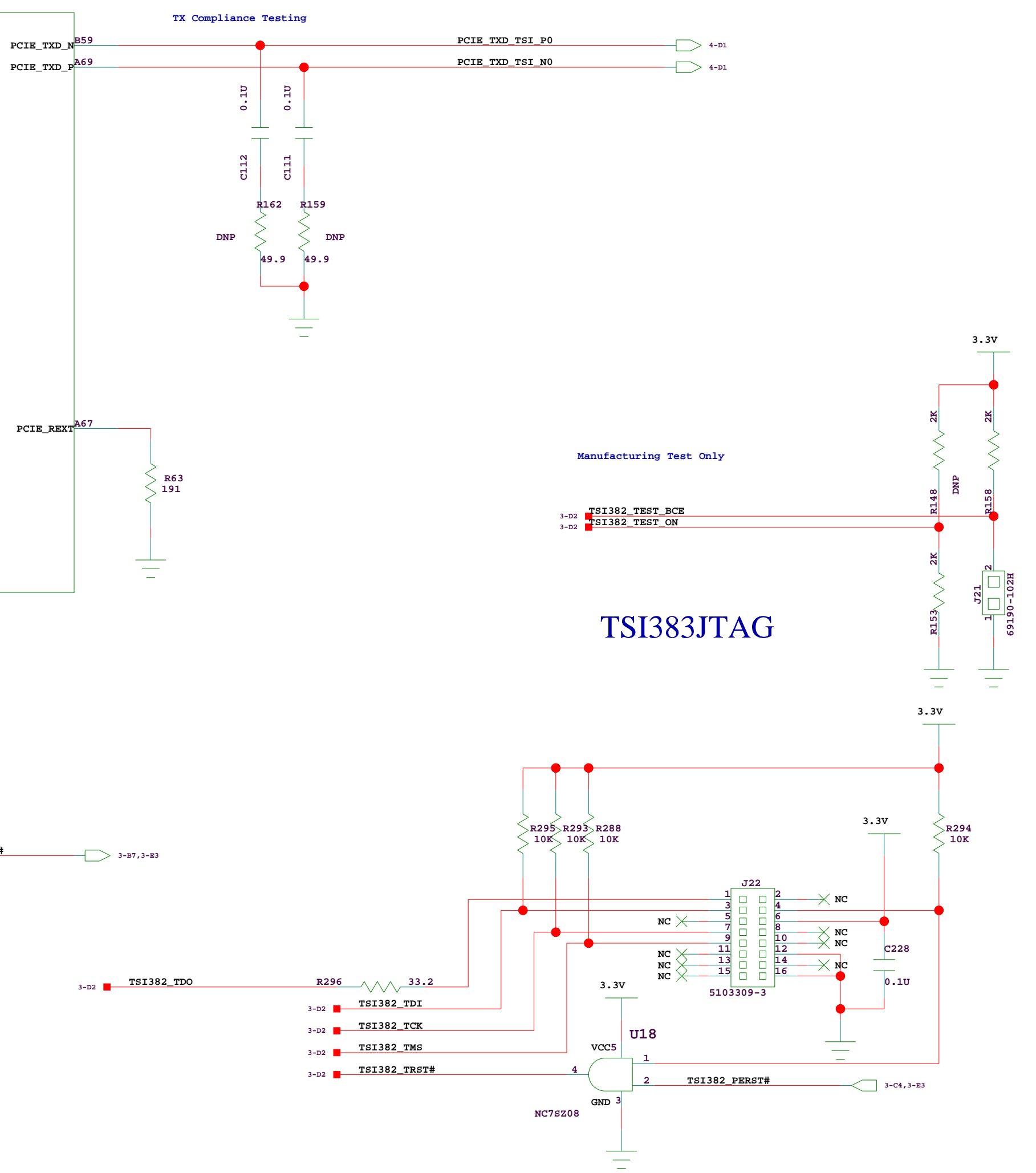
TSI383 STRAPS



RESET CONTROLLER

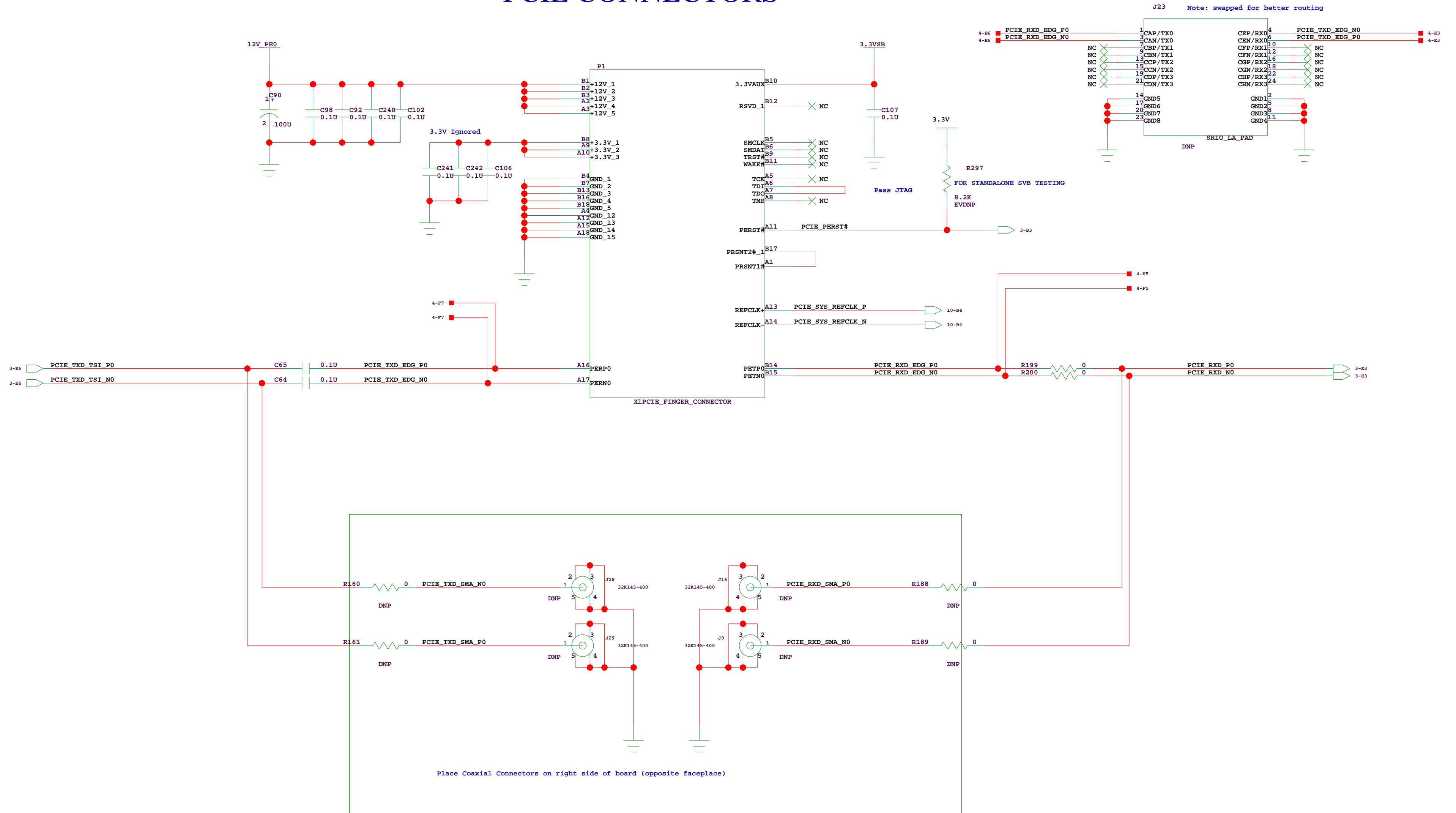


TSI383JTAG



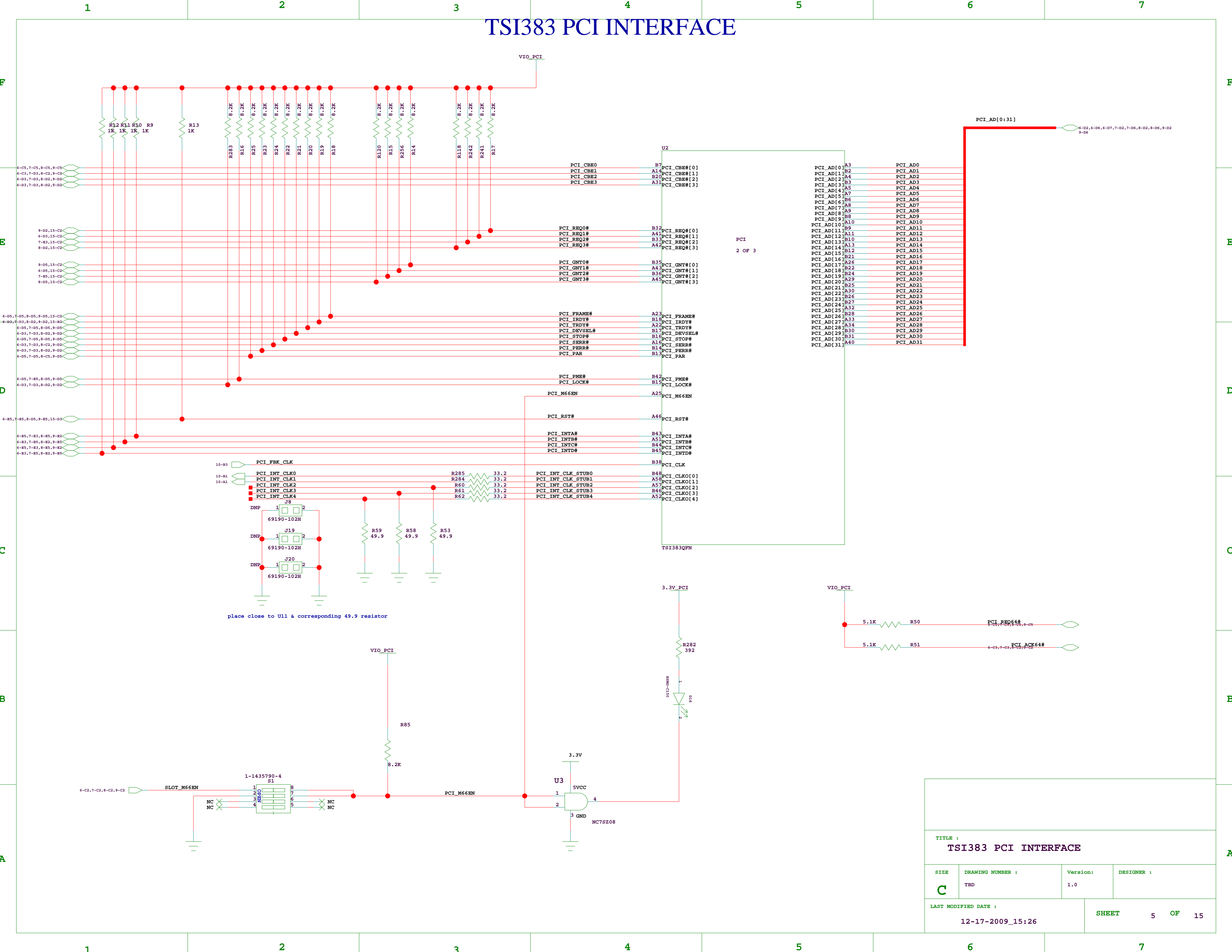
TITLE : TSI383 PCIE/MISC			
SIZE C	DRAWING NUMBER : TBD	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 12-17-2009_15:26		SHEET 3 OF 15	

PCIE CONNECTORS



TITLE :			
PCIE CONNECTORS			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	TBD	1.0	
LAST MODIFIED DATE :			SHEET
12-17-2009_15:26			4 OF 15

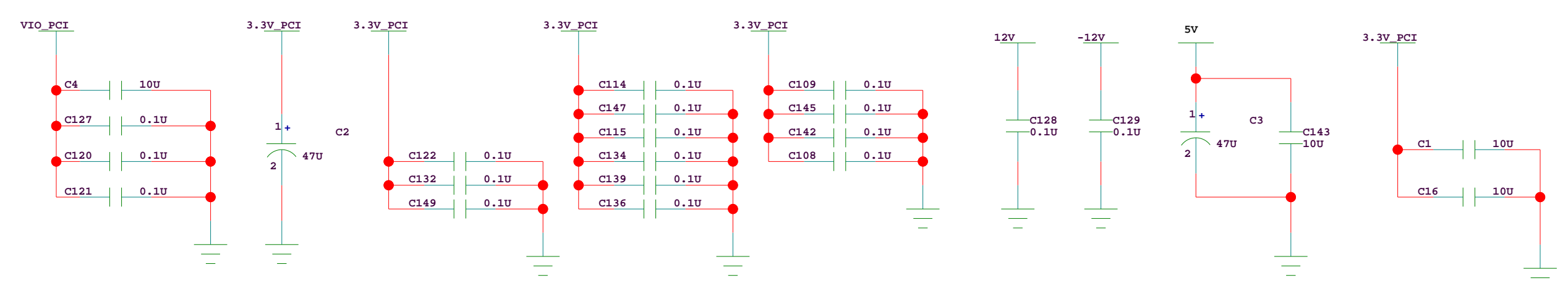
TSI383 PCI INTERFACE



TITLE :			
TSI383 PCI INTERFACE			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	TBD	1.0	
LAST MODIFIED DATE :			SHEET
12-17-2009_15:26			5 OF 15

PCI SLOT 0 (R/A)

IDSEL AD16
 - Required Interrupt Routing
 SLOT : BRIDGE
 INTA -> INTA
 INTB -> INTB
 INTC -> INTC
 INTD -> INTD
 - PCI Clock PCI_CLK0
 - PCI Arbitration PCI_GNT#1/PCI_REQ#1

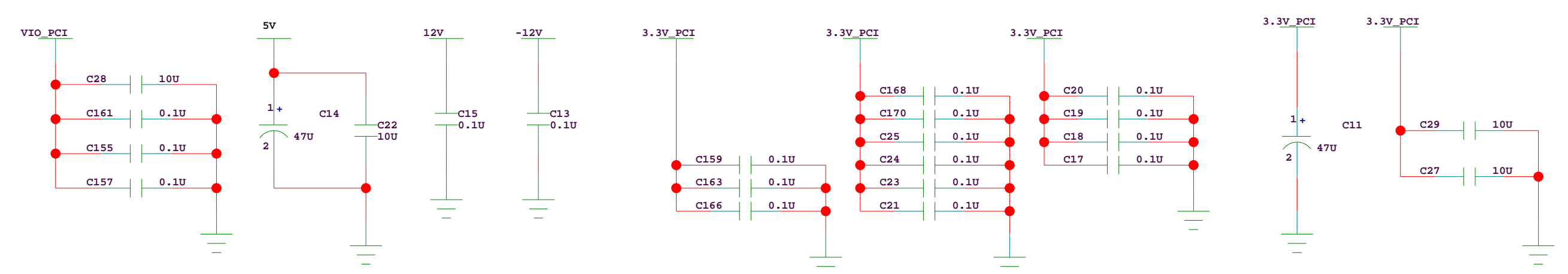
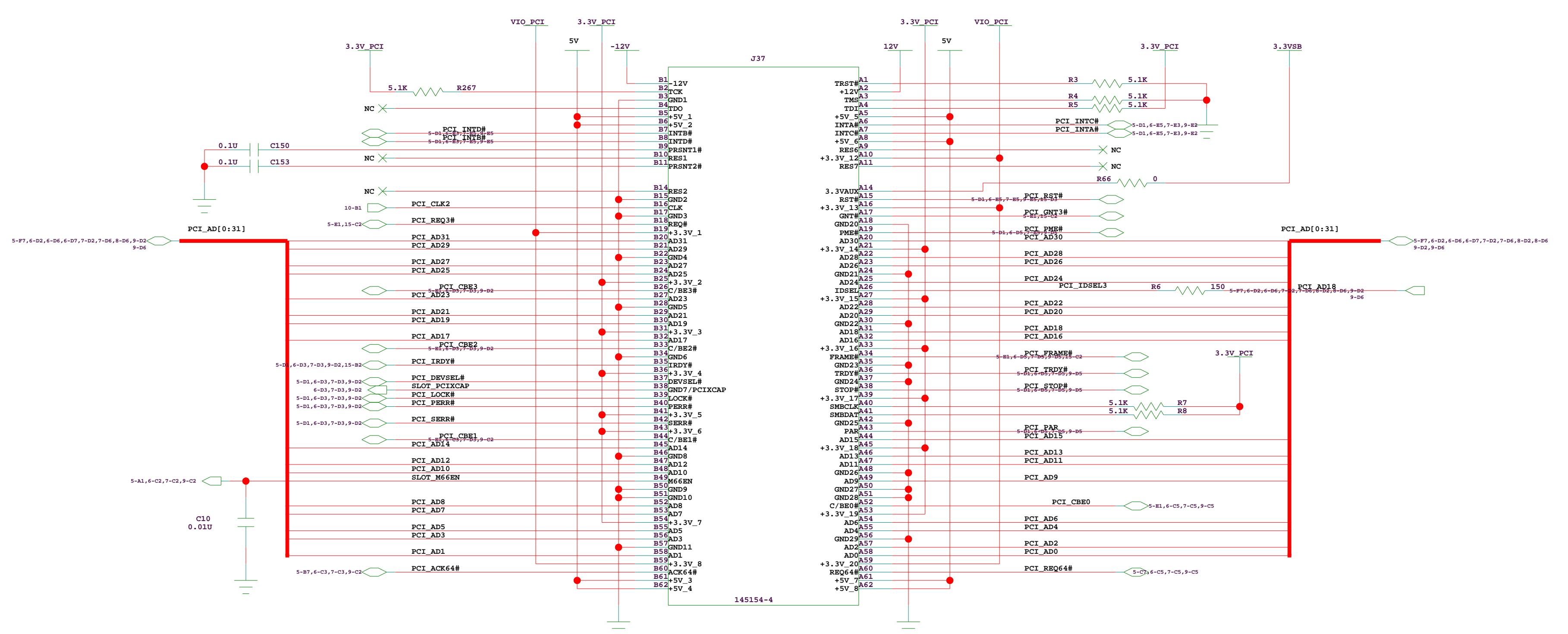


TITLE :			
PCI SLOT 0			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	TBD	1.0	
LAST MODIFIED DATE :			SHEET
12-17-2009_15:26			6 OF 15

PCI SLOT 3 (Vertical)

IDSEL AD18

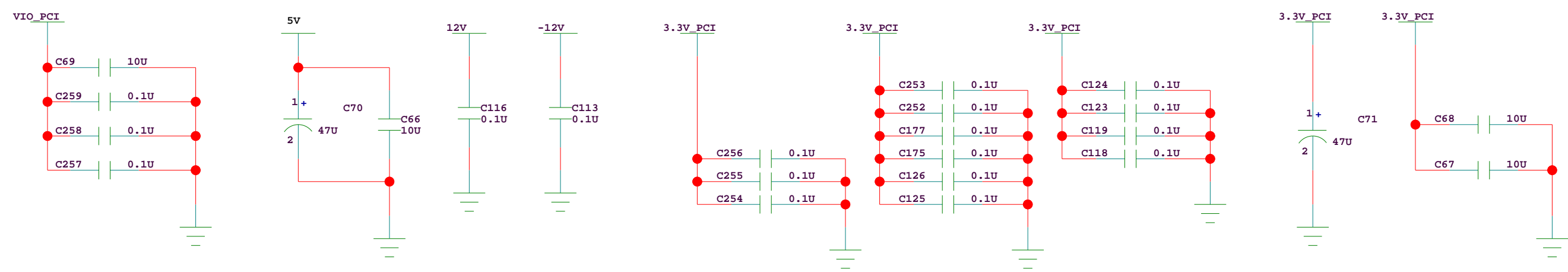
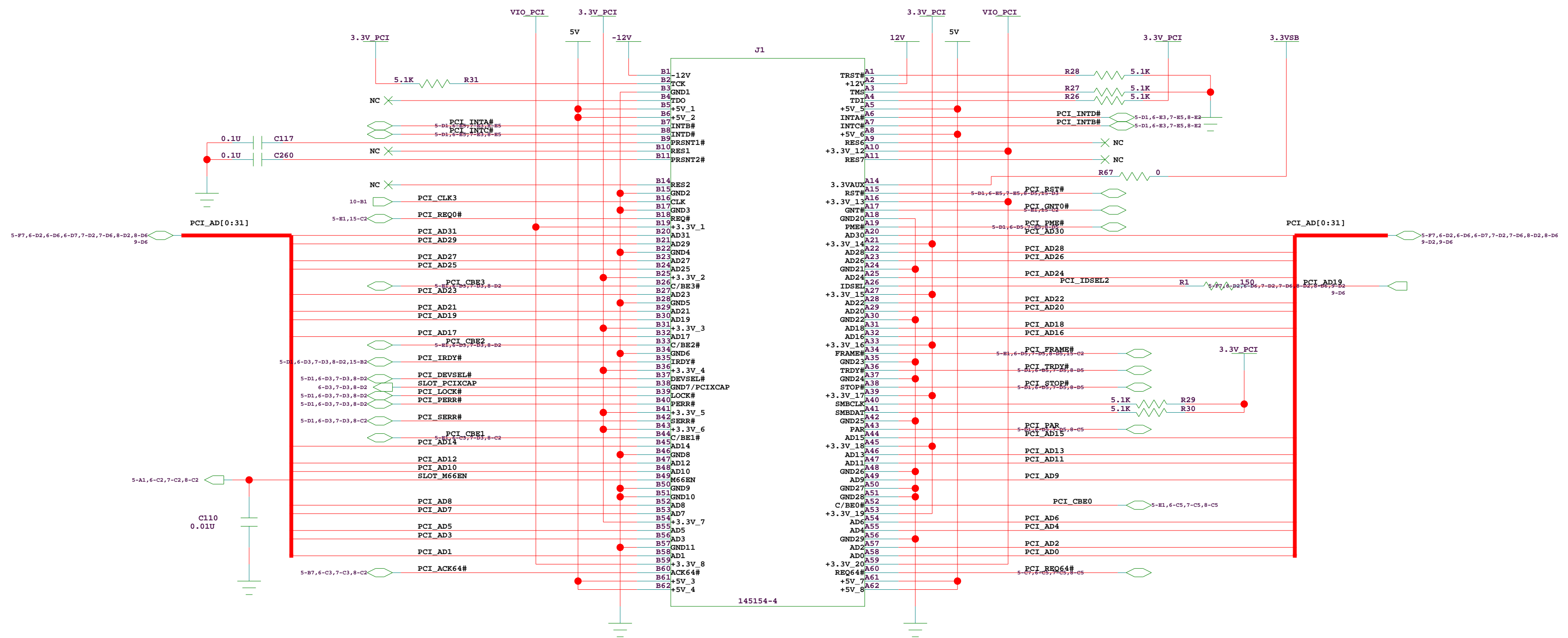
- Required Interrupt Routing
- SLOT : BRIDGE
- INTA -> INTC
- INTB -> INTD
- INTC -> INTA
- INTD -> INTB
- PCI Clock PCI_CLK2
- PCI Arbitration PCI_GNT3#/PCI_REQ#3



TITLE :			
PCI SLOT 3			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	TBD	1.0	
LAST MODIFIED DATE :			SHEET
12-17-2009_15:26			8 OF 15

PCI SLOT 2 (Vertical)

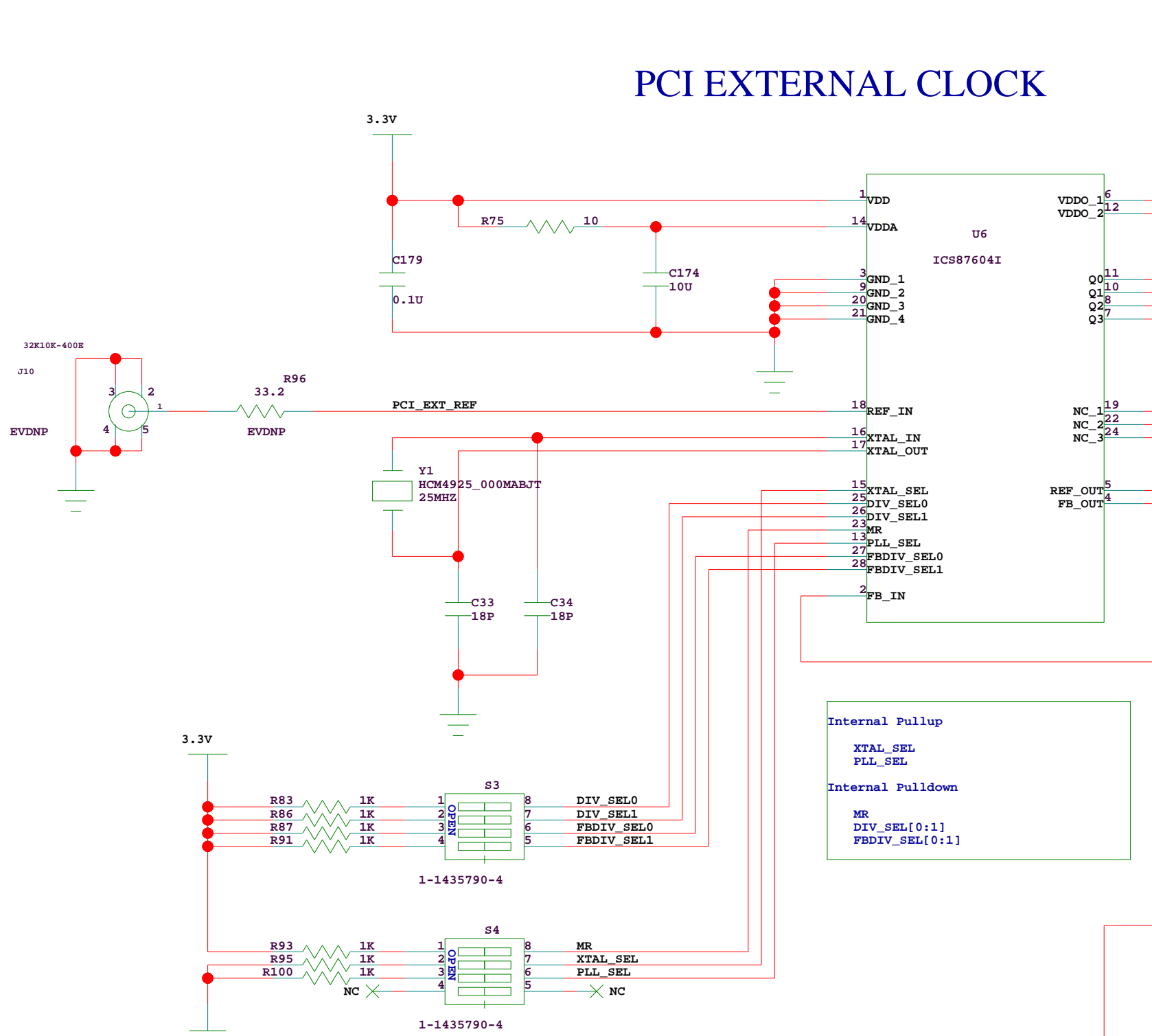
IDSEL AD19
 - Required Interrupt Routing
 SLOT : BRIDGE
 INTA -> INTD
 INTB -> INTA
 INTC -> INTB
 INTD -> INTC
 - PCI Clock PCI_CLK3
 - PCI Arbitration PCI_GNT0#/PCI_REQ#0



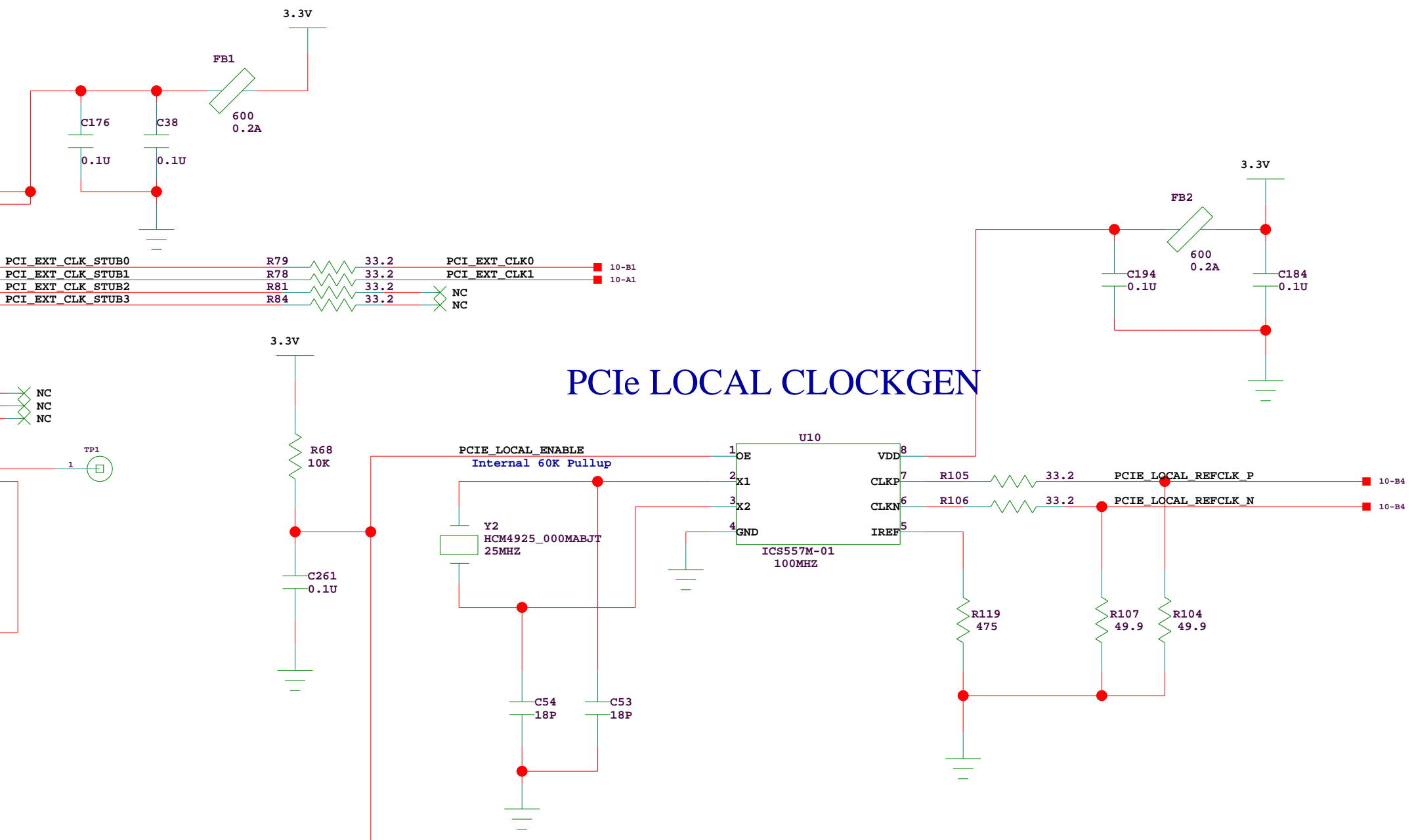
TITLE :			
PCI SLOT 2			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	TBD	1.0	
LAST MODIFIED DATE :			SHEET
12-17-2009_15:26			9 OF 15

CLOCK DISTRIBUTION

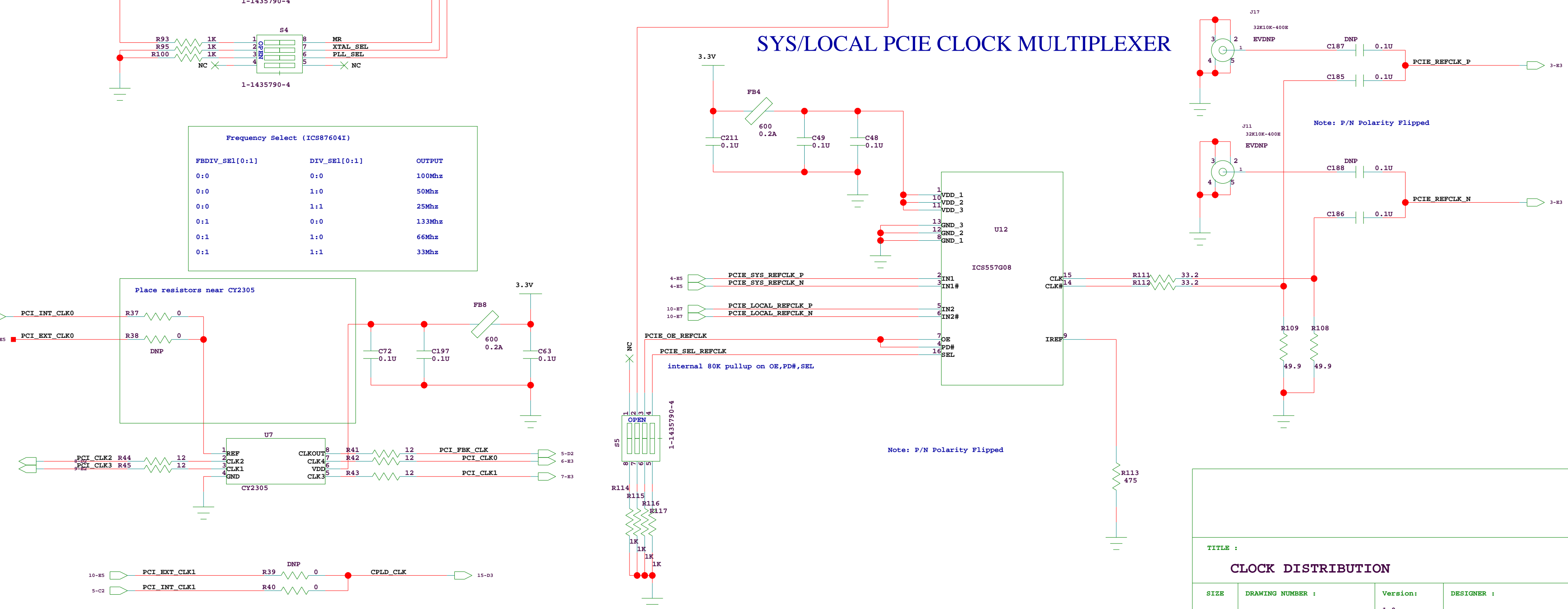
PCI EXTERNAL CLOCK



PCIe LOCAL CLOCKGEN



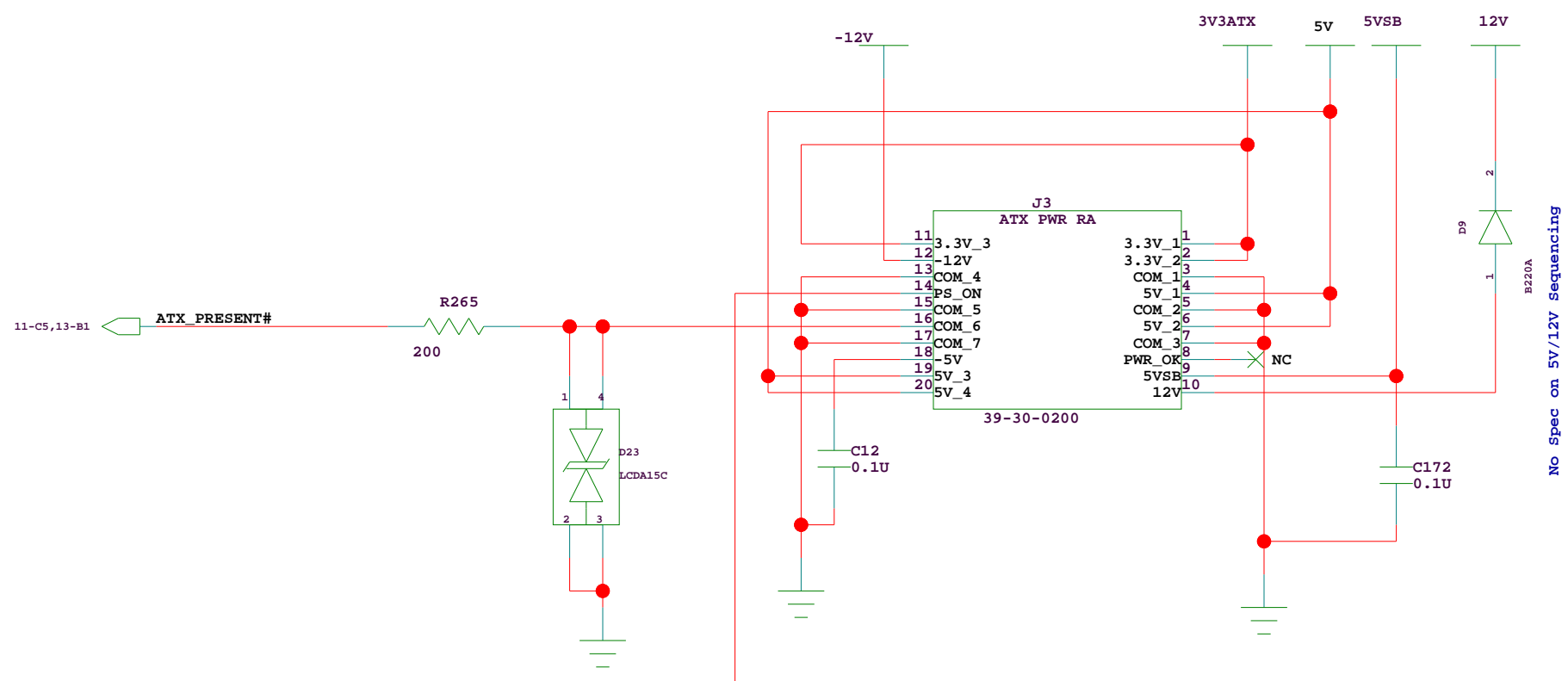
SYS/LOCAL PCIe CLOCK MULTIPLEXER



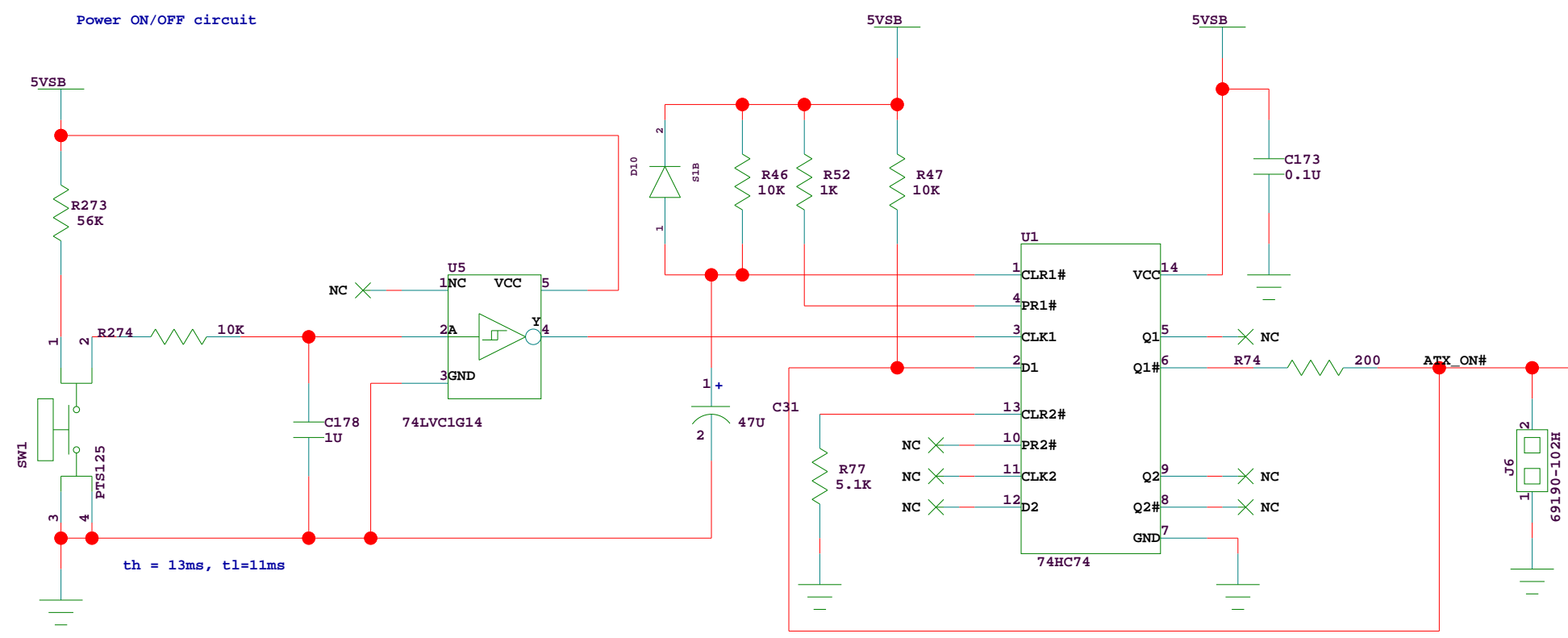
TITLE :			
CLOCK DISTRIBUTION			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C		1.0	
LAST MODIFIED DATE :			SHEET
12-17-2009_15:26			10 OF 15

POWER SOURCES

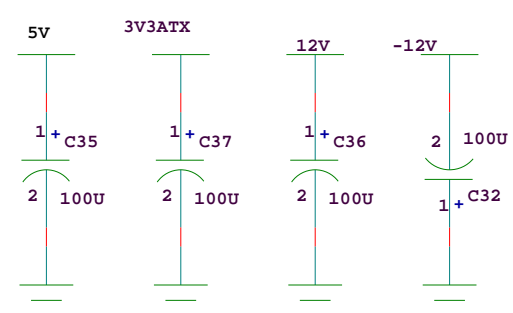
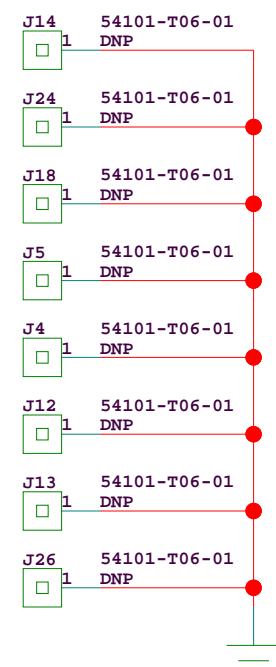
ATX



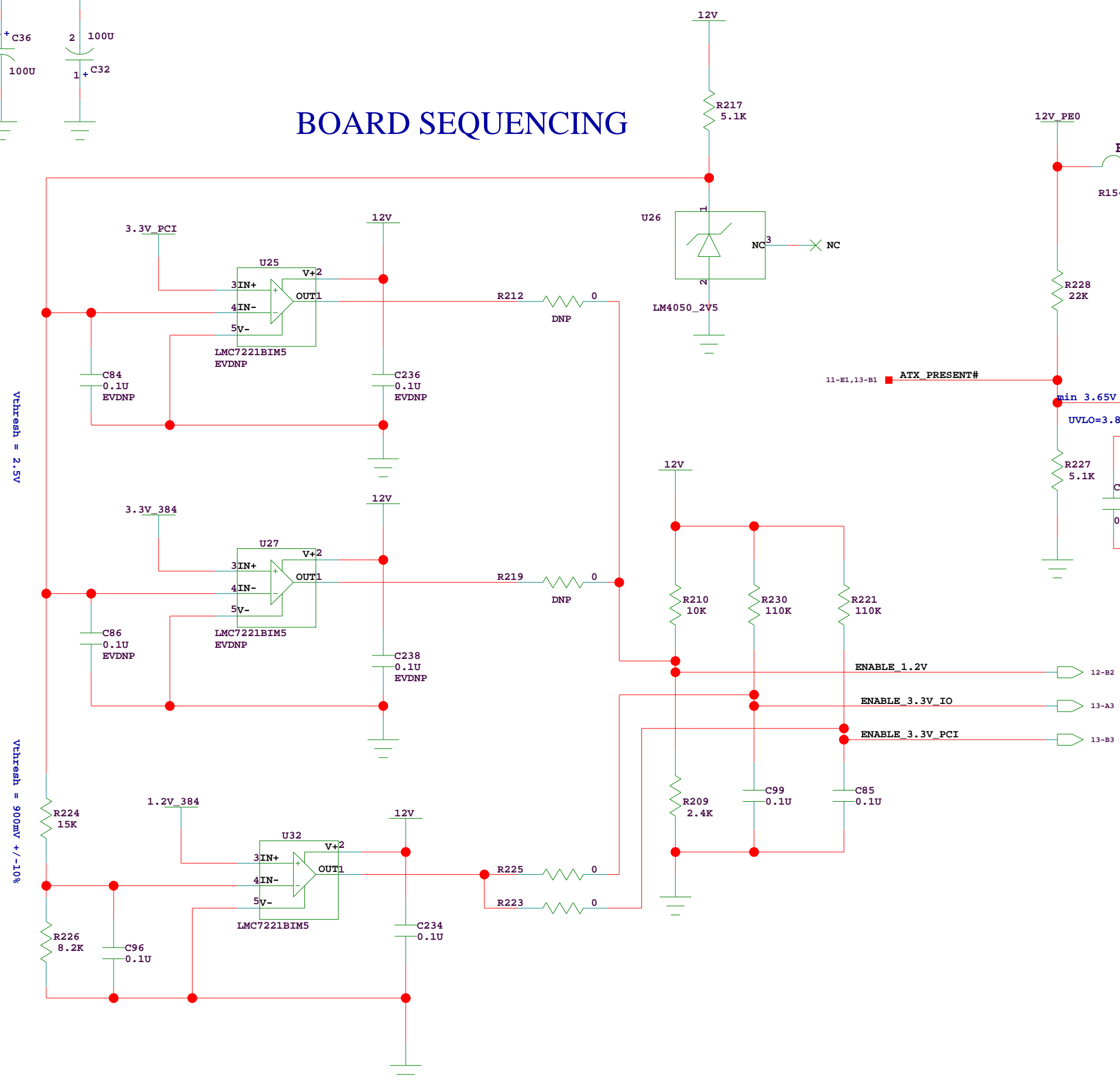
ATX SUPPLY TOGGLE



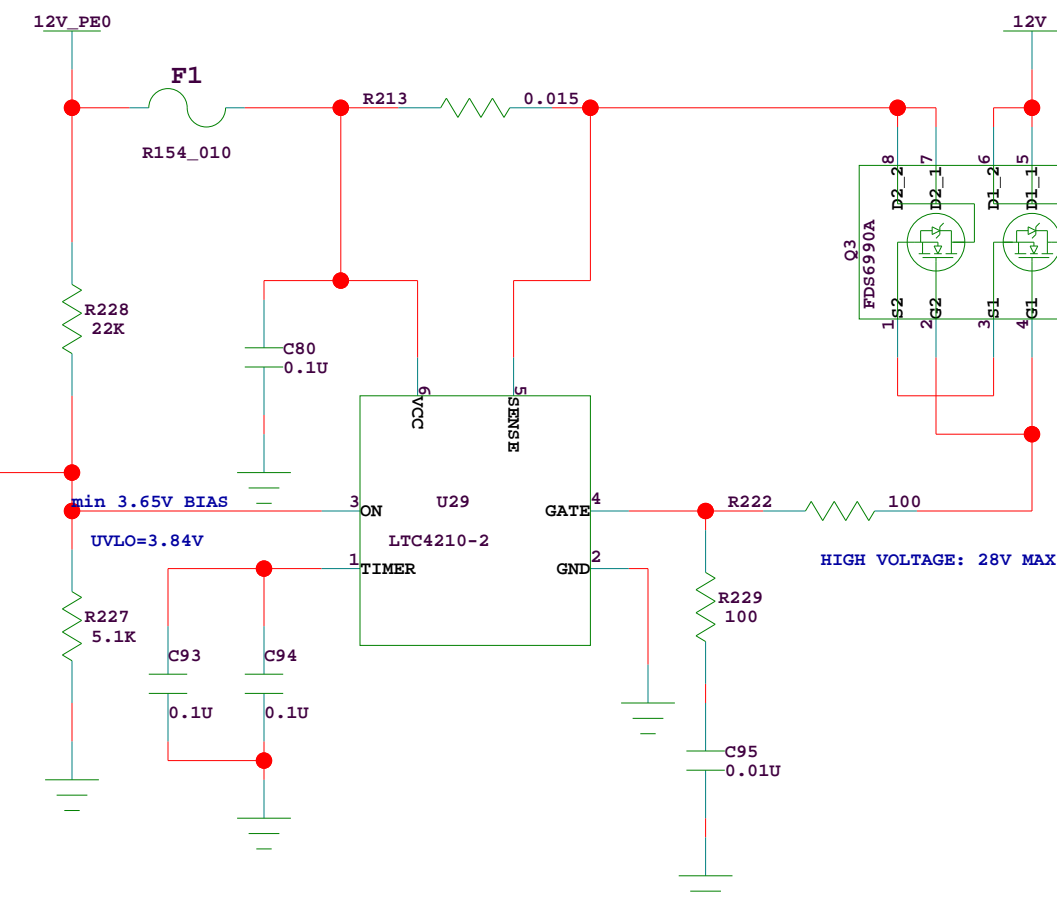
GND TESTPOINTS



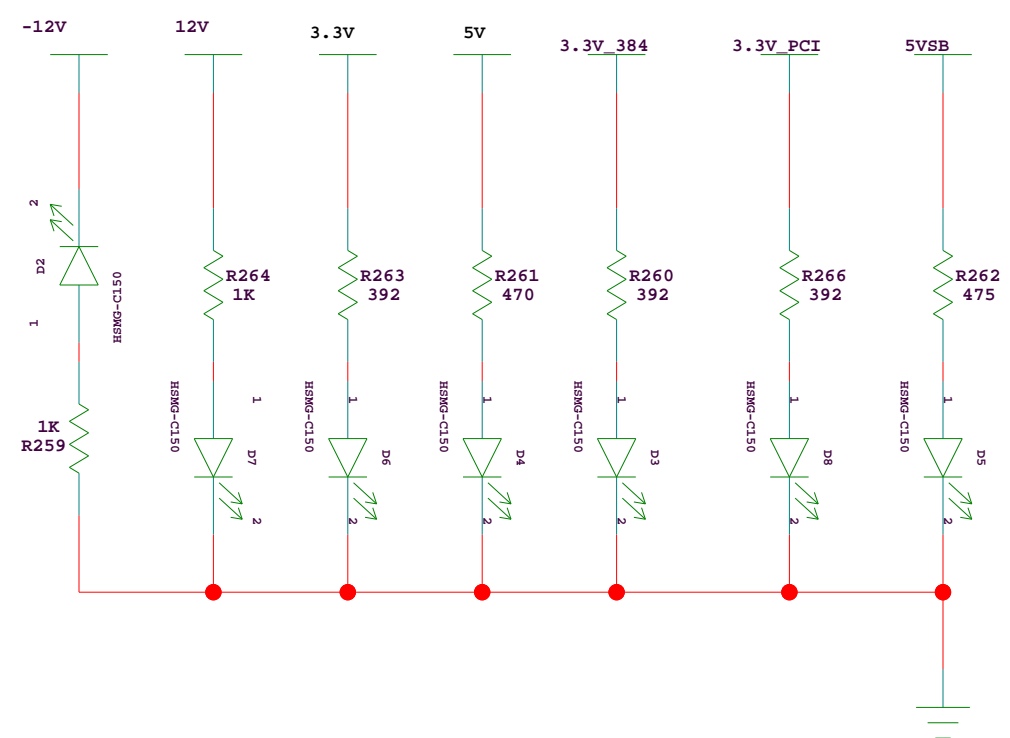
BOARD SEQUENCING



SYS SUPPLY SWITCH

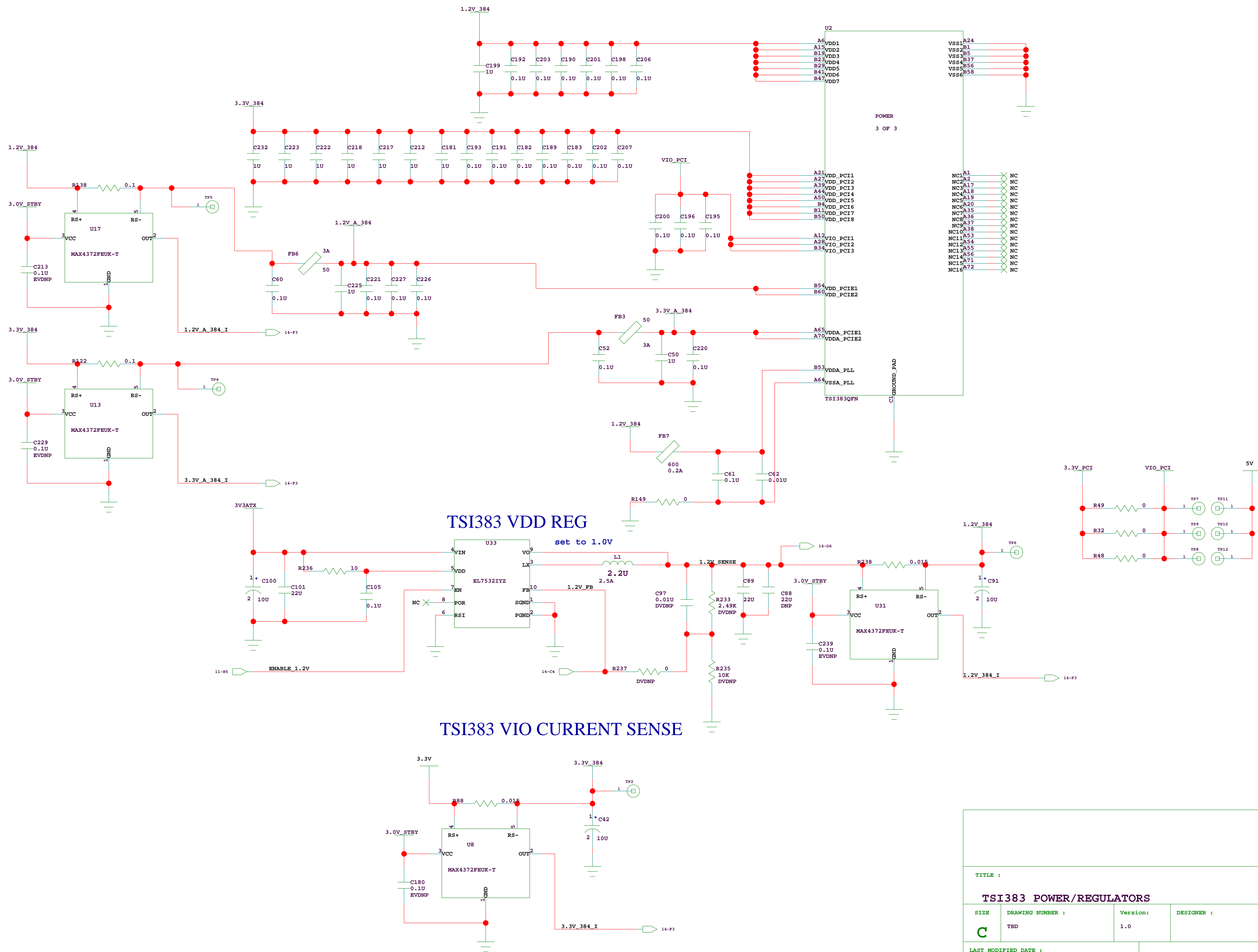


POWER STATUS



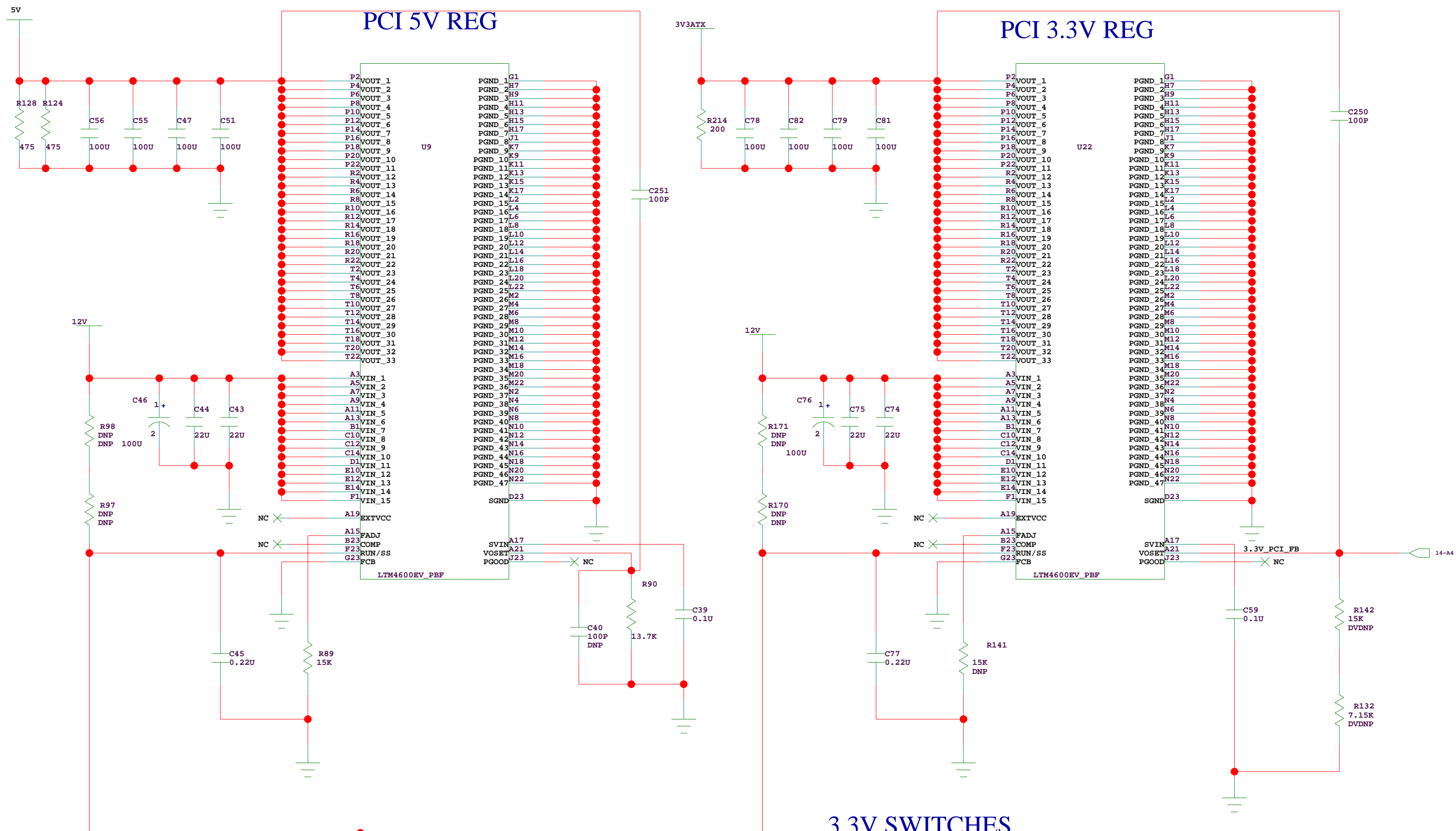
TITLE : POWER SOURCES			
SIZE : TBD	DRAWING NUMBER : TBD	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 12-17-2009_15:26		SHEET 11	OF 15

TSI383 POWER/REGULATORS

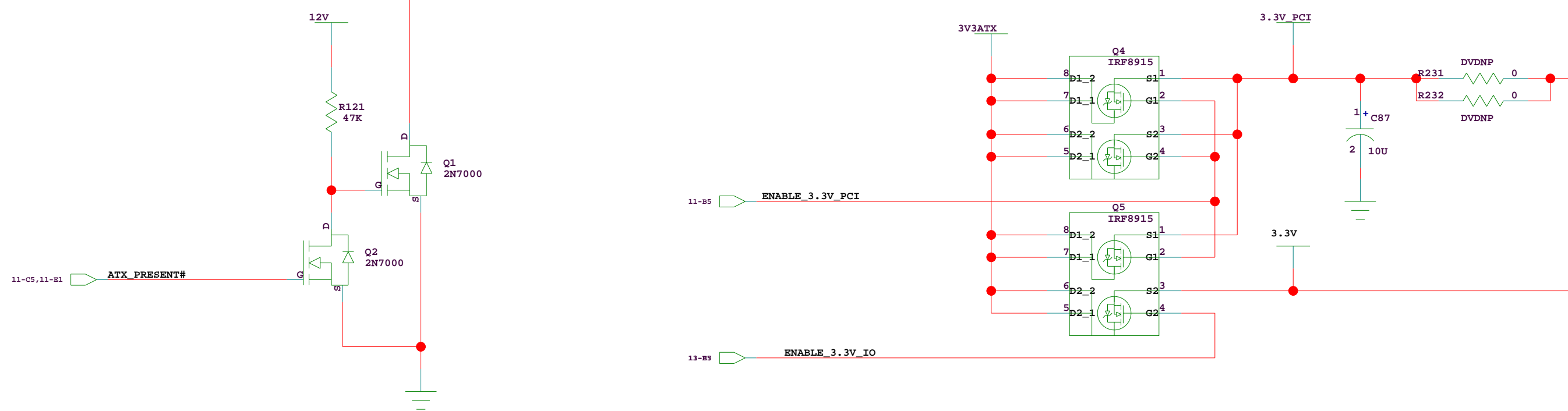


TITLE :			
TSI383 POWER/REGULATORS			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	TBD	1.0	
LAST MODIFIED DATE :			SHEET
12-17-2009_15:26			12 OF 15

PCI POWER REGULATORS



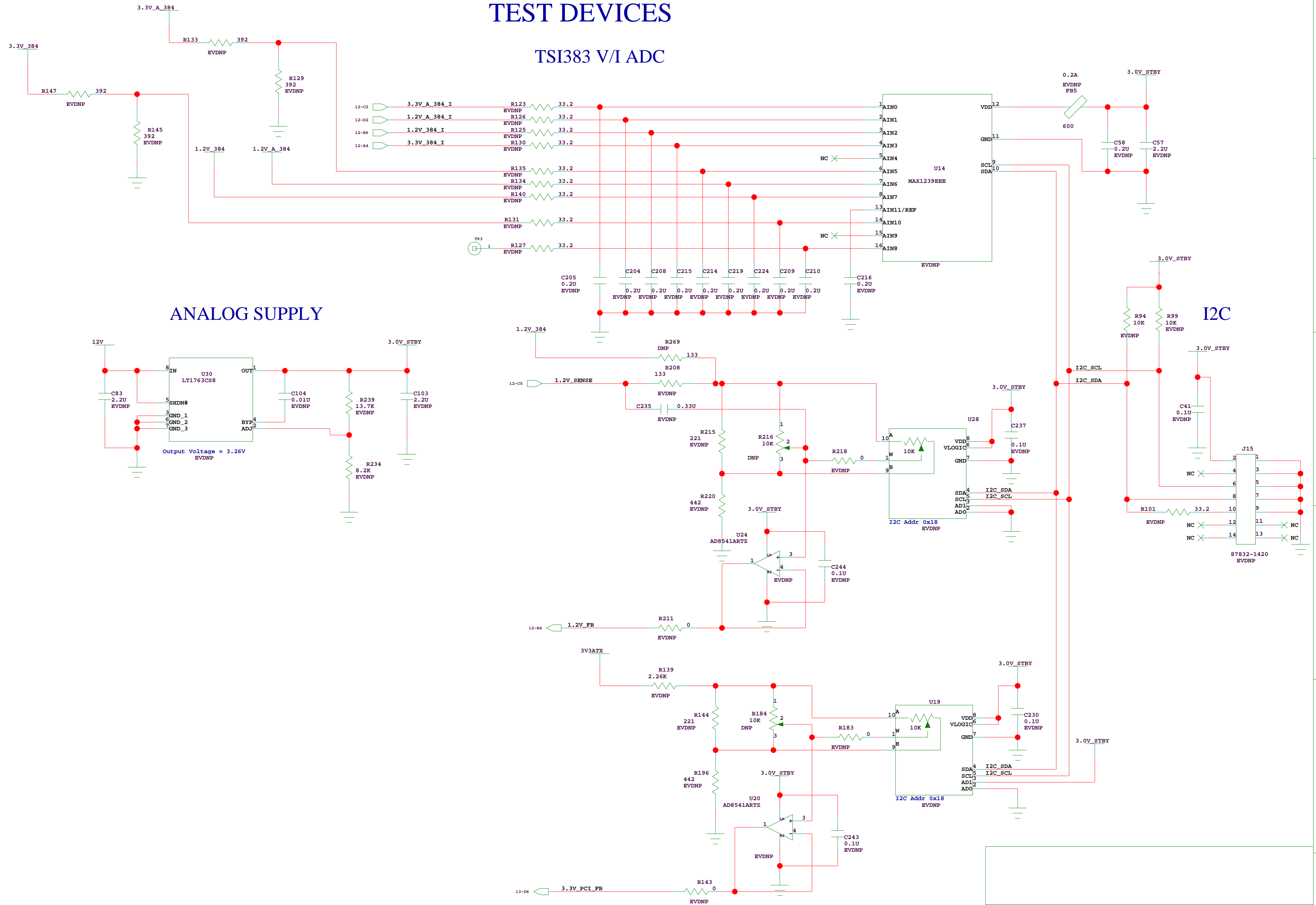
3.3V SWITCHES



TITLE :			
PCI POWER REGULATORS			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	TBD	1.0	
LAST MODIFIED DATE :			SHEET
12-17-2009_15:26			13 OF 15

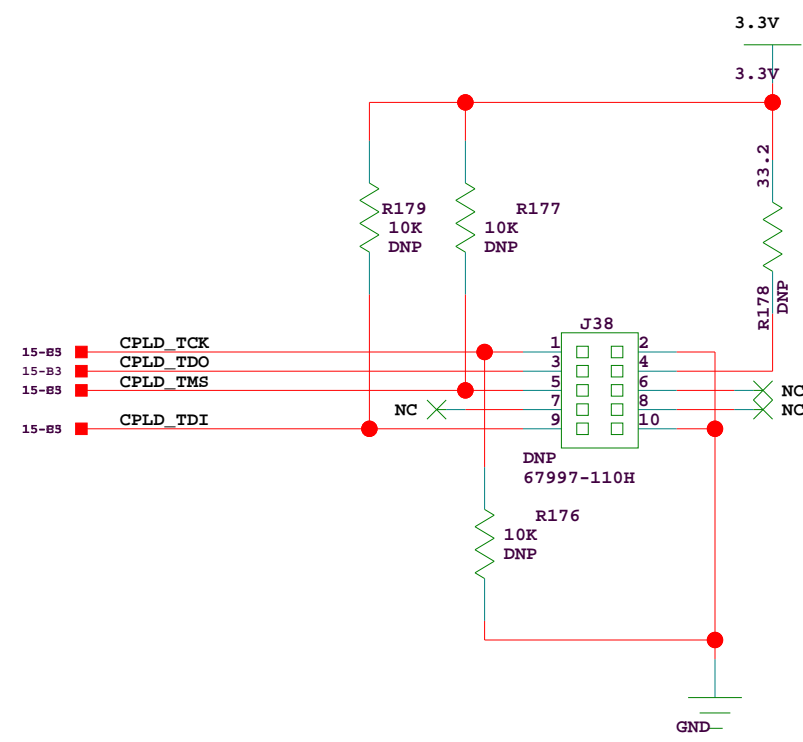
TEST DEVICES

TSI383 V/I ADC

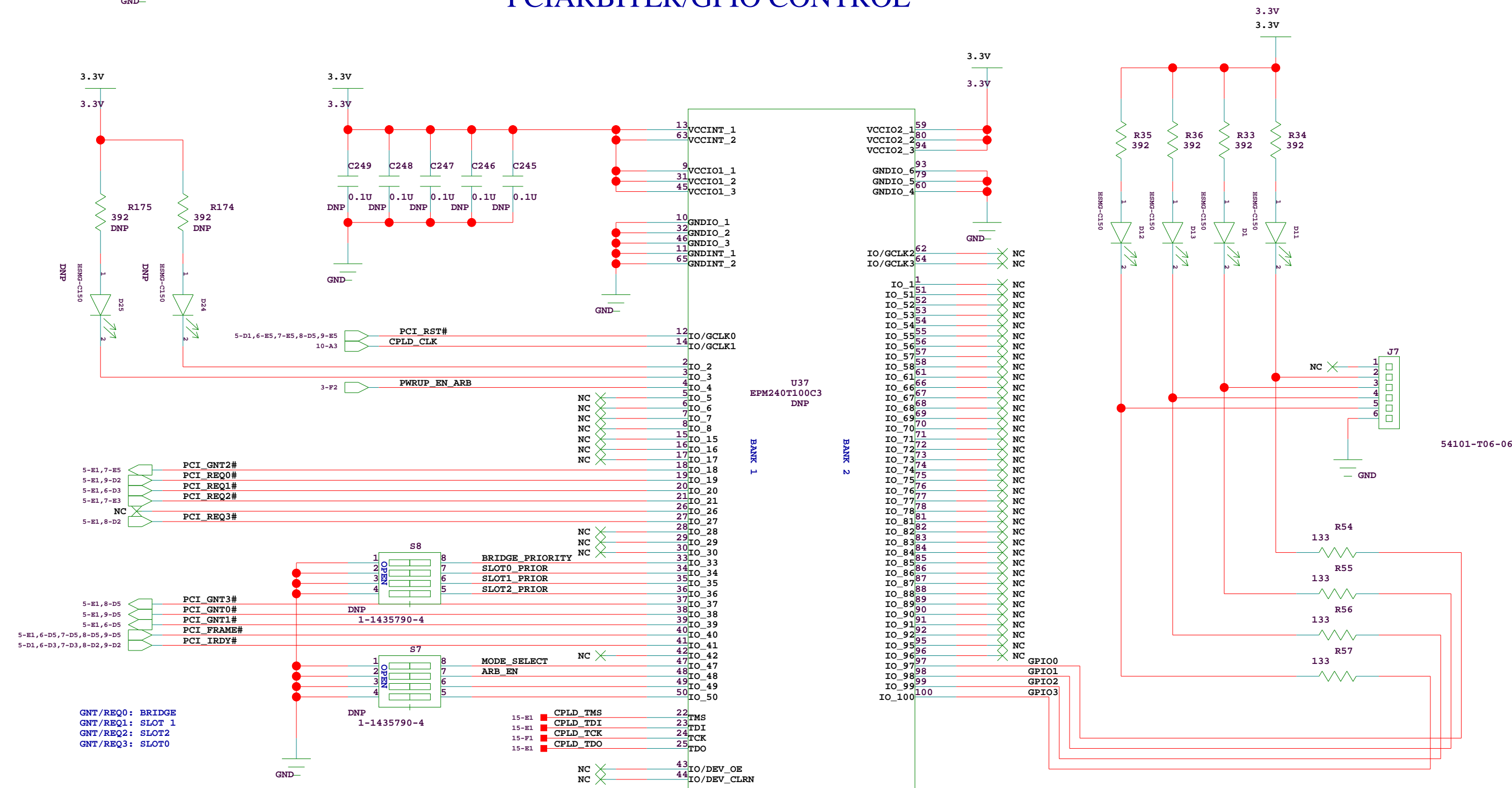


TITLE :			
TEST DEVICES			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	TBD	1.0	
LAST MODIFIED DATE :			SHEET
12-17-2009_15:26			14 OF 15

TEST DEVICES CONT'D



PCIARBITER/GPIO CONTROL



TITLE :			
TEST DEVICES CONT'D			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	TBD	1.0	
LAST MODIFIED DATE :			SHEET
12-17-2009_15:26			15 OF 15