Engineering Change Notice

The following table contains a list of engineering changes that are not reflected in the Tsi382 (BGA) Evaluation Board Schematics.

Table 1: ECN for E2010_AS001_02 (Board order number Tsi382-RDK1 V2.0)

No.	Item(s)	Original	Change To
1	Tsi382 Device	Tsi382-66ILVZ1	Tsi382-66ILVZ2
2	JTAG signals pull-ups	2K pull-up on R288, R293, R294, and R295	10K pull-up on resistors
3	EEPROM socket	No EEPROM installed in DIP-8 socket U23	Installed AT25604A-10PU-2.7 Atmel EEPROM in DIP-8 socket U23.
4	PCI reset time too short	C231	10uF, ECJ-1VB0J106M

Tsi382 Evaluation Board Schematics

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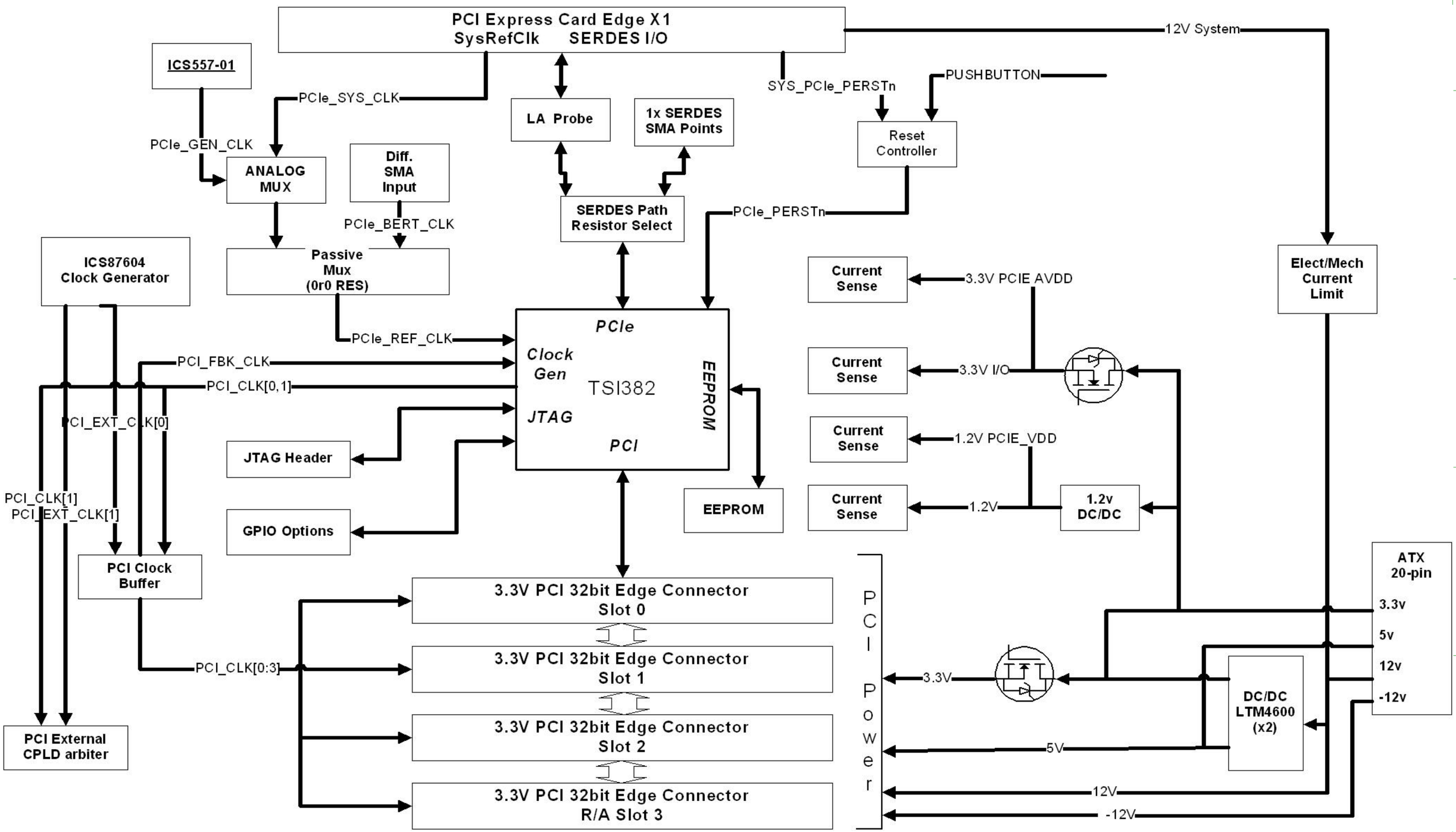
BLOCK DIAGRAM



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SIZE C	DRAWING NUMBER : 60E2010_SC001	Version: 1.0	DESIGNER : PHILIP LAUZON	
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TSI382 PCIE/MISCELLANEOUS

TSI382 STRAPS

S1 Default Configuration

Signal	(1=High,0=Low)
N/C	
PWRUP_EN_ARB	0
N/C	
PLL_BYPASS	0

3.3V
R137 8.2K
R157 8.2K
1-1435790-4
S6
OPEN
NC
NC
PWRUP_EN_ARB
PWRUP_PLL_BYPASS
3-E3,15-C3
3-D3

TSI382 JTAG

Test for IDT Only

3.3V
2K DNP R150
2K DNP R148
2K R158
2K R156
2K R153
J21
69130-102LF
3-D2 TSI382_TEST_BCE
3-D2 TSI382_TEST_ON
3-D2 TSI382_TEST_BIDR_CTRL

RESET CONTROLLER

2.6V Threshold on SENSE

5V
R172 1K
B1 B2 SW2 EVQPAC07K A1 A2
R173 1K
C231 1U
3.3V 5V
U15
TL7702BCD
VCC SENSE RESIN# CT RESET# RESET GND REF NC
0.1U C73
3.3V
R136 1K
U16
NC7SZ08
VCC GND
TSI382_PERST#
3-B7,3-E3
4-E5 PCIE_PERST#

TX Compliance Testing

PCIE_TXD_P A4
PCIE_TXD_N B4
0.1U C112
0.1U C111
R162 DNP 49.9
R159 DNP 49.9
PCIE_TXD_TSI_P0 4-D1
PCIE_TXD_TSI_N0 4-D1

TSI382

U11

4-D7 PCIE_RXD_P0	A6	PCIE_RXD_P
4-D7 PCIE_RXD_N0	B6	PCIE_RXD_N
10-C7 PCIE_REFCLK_P	B8	PCIE_REFCLK_P
10-C7 PCIE_REFCLK_N	A8	PCIE_REFCLK_N
3-B7,3-C4 TSI382_PERST#	B9	PCIE_PERSTN
3-F2,15-C3 PWRUP_EN_ARB	K11	PWRUP_EN_ARB
3-F2 PWRUP_PLL_BYPASS	L1	PWRUP_PLL_BYPASS
TSI382_SR_CLK	A2	SR_CLK
TSI382_SR_CSN	D4	SR_CSN
TSI382_SR_DIN	A3	SR_DIN
TSI382_SR_DOUT	E4	SR_DOUT
3-B5 TSI382_TCK	K4	JTAG_TCK
3-B5 TSI382_TDI	M3	JTAG_TDI
3-B4 TSI382_TDO	K3	JTAG_TDO
3-B5 TSI382_TMS	M12	JTAG_TMS
3-B5 TSI382_TRST#	K9	JTAG_TRSTN
3-D6 TSI382_TEST_BCE	D7	TEST_BCE
3-D6 TSI382_TEST_BIDR_CTRL	C3	TEST_BIDR_CTL
3-D6 TSI382_TEST_ON	B3	TEST_ON
PCIE_REXT	A11	

1 OF 3
PCIE, MISC

R63 191

U23

3.3V
R207 8.2K
C233 0.1U
R198 8.2K
R187 8.2K
VCC GND WP# HOLD# SCK CS# SI SO
AT25640A-10PU-2
DNP
AR_U1
115-13-308-41-001

3.3V / 5V

3.3V
2K R295
2K R293
2K R288
2K R294
J22
5103309-3
NC
C228 0.1U
U18
NC7SZ08
VCC GND
TSI382_PERST# 3-C4,3-E3
3-D2 TSI382_TDO
R296 33.2
3-D2 TSI382_TDI
3-D2 TSI382_TCK
3-D2 TSI382_TMS
3-D2 TSI382_TRST#

TITLE : TSI382 PCIE/MISC

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60E2010_SC001	1.0	PHILIP LAUZON

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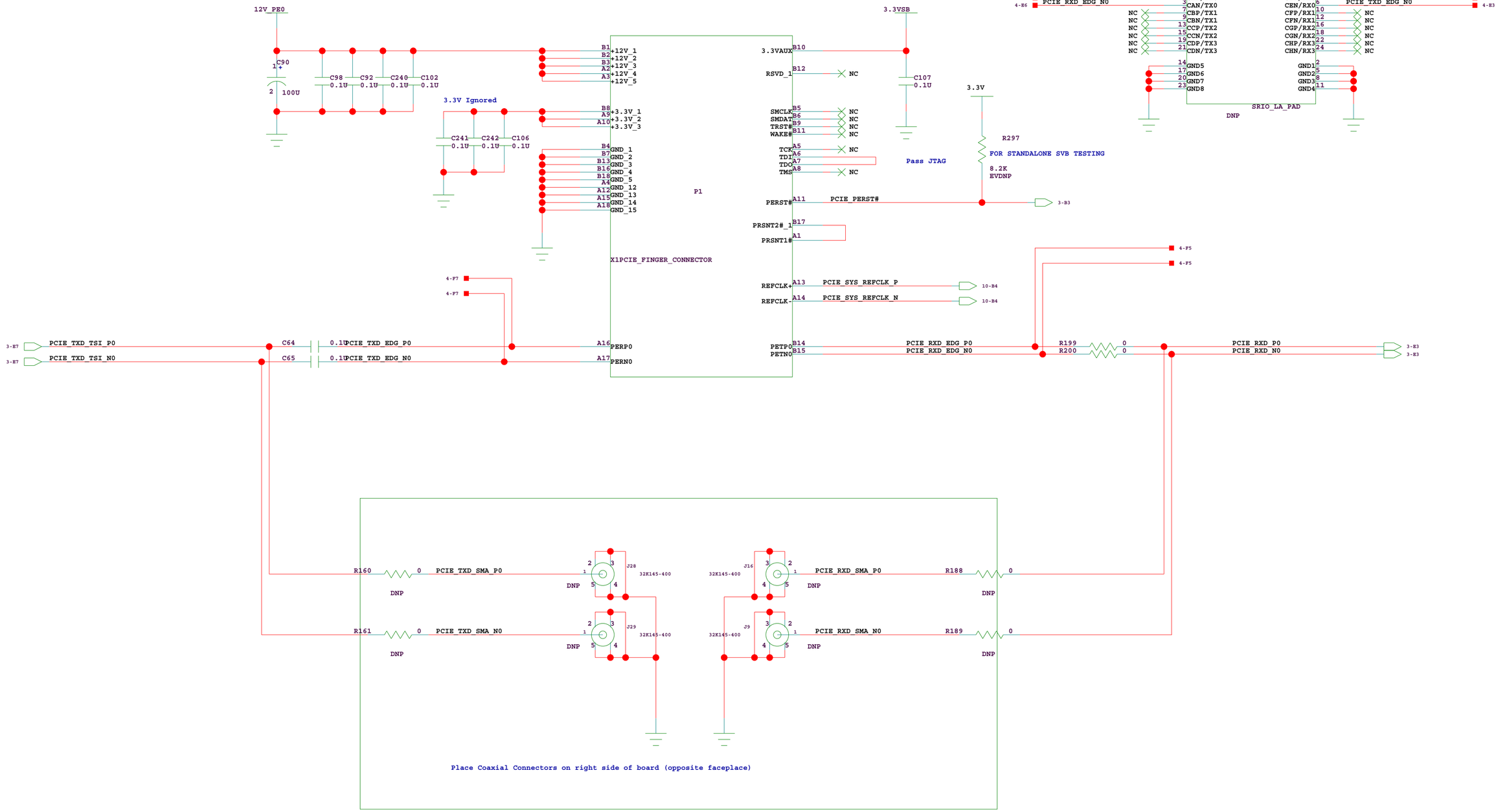
PCIE CONNECTORS



TITLE : PCIE CONNECTORS			
SIZE C	DRAWING NUMBER : 60E2010_SC001	Version: 1.0	DESIGNER : PHILIP LAUZON
LAST MODIFIED DATE : 1-9-2008_14:18	SHEET 4 OF 15		

TSI382 PCI INTERFACE

VIO_PCI

R12 2.4K
R11 2.4K
R10 2.4K
R9 2.4K
R13 1K
R283 8.2K
R16 8.2K
R25 8.2K
R23 8.2K
R24 8.2K
R22 8.2K
R21 8.2K
R20 8.2K
R19 8.2K
R18 8.2K
R120 8.2K
R15 8.2K
R256 8.2K
R14 8.2K
R118 8.2K
R242 8.2K
R241 8.2K
R17 8.2K

U11

PCI_AD[0:31] → 6-D2,6-D6,6-D7,7-D2,7-D6,8-D2,8-D6,9-D2 9-D6

6-C5,7-C5,8-C5,9-C5	PCI_CBE0	F3	PCI_CBEN[0]
6-C3,7-D3,8-C2,9-C2	PCI_CBE1	J3	PCI_CBEN[1]
6-D3,7-D3,8-D2,9-D2	PCI_CBE2	M4	PCI_CBEN[2]
6-D3,7-D3,8-D2,9-D2	PCI_CBE3	L9	PCI_CBEN[3]
9-D2,15-C2	PCI_REQ0#	F10	PCI_REQN[0]
6-D3,15-C2	PCI_REQ1#	J10	PCI_REQN[1]
7-B3,15-C2	PCI_REQ2#	G10	PCI_REQN[2]
8-D2,15-C2	PCI_REQ3#	H11	PCI_REQN[3]
9-D5,15-C2	PCI_GNT0#	G9	PCI_GNTN[0]
6-D5,15-C2	PCI_GNT1#	F12	PCI_GNTN[1]
7-B5,15-C2	PCI_GNT2#	F11	PCI_GNTN[2]
8-D5,15-C2	PCI_GNT3#	E10	PCI_GNTN[3]
6-D5,7-D5,8-D5,9-D5,15-C2	PCI_FRAME#	M5	PCI_FRAMEN
6-D3,7-D3,8-D2,9-D2,15-B2	PCI_IRDY#	L5	PCI_IRDYN
6-D5,7-D5,8-D5,9-D5	PCI_TRDY#	K5	PCI_TRDYN
6-D3,7-D3,8-D2,9-D2	PCI_DEVSEL#	M2	PCI_DEVSELN
6-D5,7-D5,8-D5,9-D5	PCI_STOP#	J6	PCI_STOPN
6-D3,7-D3,8-C2,9-D2	PCI_SERR#	J2	PCI_SERRN
6-D3,7-D3,8-D2,9-D2	PCI_PERR#	J4	PCI_PERRN
6-D5,7-D5,8-C5,9-D5	PCI_PAR	K1	PCI_PAR
6-D5,7-E5,8-D5,9-D5	PCI_PME#	H12	PCI_PMEN
6-D3,7-D3,8-D2,9-D2	PCI_LOCK#	L3	PCI_LOCKN
	PCI_M66EN	B11	PCI_M66EN
6-E5,7-E5,8-D5,9-E5,15-D3	PCI_RST#	E12	PCI_RSTN
6-E5,7-E3,8-E5,9-E2	PCI_INTA#	D12	PCI_INTAN
6-E3,7-E5,8-E2,9-E5	PCI_INTB#	F9	PCI_INTBN
6-E5,7-E3,8-E5,9-E2	PCI_INTC#	C10	PCI_INTCN
6-E3,7-E5,8-E2,9-E5	PCI_INTD#	C12	PCI_INTDN
10-B3	PCI_FBK_CLK	B12	PCI_CLK
10-B1	PCI_INT_CLK0	H10	PCI_CLKO[0]
10-B1	PCI_INT_CLK1	B2	PCI_CLKO[1]
10-A1	PCI_INT_CLK2	J9	PCI_CLKO[2]
	PCI_INT_CLK3	J8	PCI_CLKO[3]
	PCI_INT_CLK4	A12	PCI_CLKO[4]
15-B7	GPIO0	E9	GPIO[0]
15-B7	GPIO1	D8	GPIO[1]
15-B7	GPIO2	C9	GPIO[2]
15-B7	GPIO3	D9	GPIO[3]

PCI_AD[0:31] → B1 C2 F4 E3 E2 F2 D1 D3 F1 G4 E1 G1 H3 H1 H4 J1 J5 J7 L6 M6 K6 K7 M8 K8 M10 L10 L8 M11 H9 K12 J12 L12

PCI_AD[0]	PCI_AD0
PCI_AD[1]	PCI_AD1
PCI_AD[2]	PCI_AD2
PCI_AD[3]	PCI_AD3
PCI_AD[4]	PCI_AD4
PCI_AD[5]	PCI_AD5
PCI_AD[6]	PCI_AD6
PCI_AD[7]	PCI_AD7
PCI_AD[8]	PCI_AD8
PCI_AD[9]	PCI_AD9
PCI_AD[10]	PCI_AD10
PCI_AD[11]	PCI_AD11
PCI_AD[12]	PCI_AD12
PCI_AD[13]	PCI_AD13
PCI_AD[14]	PCI_AD14
PCI_AD[15]	PCI_AD15
PCI_AD[16]	PCI_AD16
PCI_AD[17]	PCI_AD17
PCI_AD[18]	PCI_AD18
PCI_AD[19]	PCI_AD19
PCI_AD[20]	PCI_AD20
PCI_AD[21]	PCI_AD21
PCI_AD[22]	PCI_AD22
PCI_AD[23]	PCI_AD23
PCI_AD[24]	PCI_AD24
PCI_AD[25]	PCI_AD25
PCI_AD[26]	PCI_AD26
PCI_AD[27]	PCI_AD27
PCI_AD[28]	PCI_AD28
PCI_AD[29]	PCI_AD29
PCI_AD[30]	PCI_AD30
PCI_AD[31]	PCI_AD31

PCI
2 OF 3

R285 33.2
R284 33.2
R60 33.2
R61 33.2
R62 33.2

J8 DNP 69190-102H
J19 DNP 69190-102H
J20 DNP 69190-102H

R59 49.9
R58 49.9
R53 49.9

place close to U11 & corresponding 49.9 resistor

PLX has L11 PU to indicate forward bridge TSI382

3.3V_PCI
R282 392
RBM0-C150 D18

VIO_PCI
5.1K R50 PCI_REQ64# → 6-C5,7-C5,8-C5,9-C5
5.1K R51 PCI_ACK64# → 6-C3,7-C3,8-C2,9-C2

VIO_PCI
R85 8.2K
SLOT_M66EN → 6-C2,7-C2,8-C2,9-C2
S1 1-1435790-4 OPEN
NC NC NC NC
PCI_M66EN

3.3V
U3 NC7SZ08
1 5VCC
2
3 GND
4

TITLE :	TSI382 PCI INTERFACE		
SIZE: C	DRAWING NUMBER : 60E2010_SC001	Version: 1.0	DESIGNER : PHILIP LAUZON
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PCI SLOT 0 (R/A)

IDSEL AD16

- Required Interrupt Routing

  SLOT : BRIDGE

  INTA -> INTA

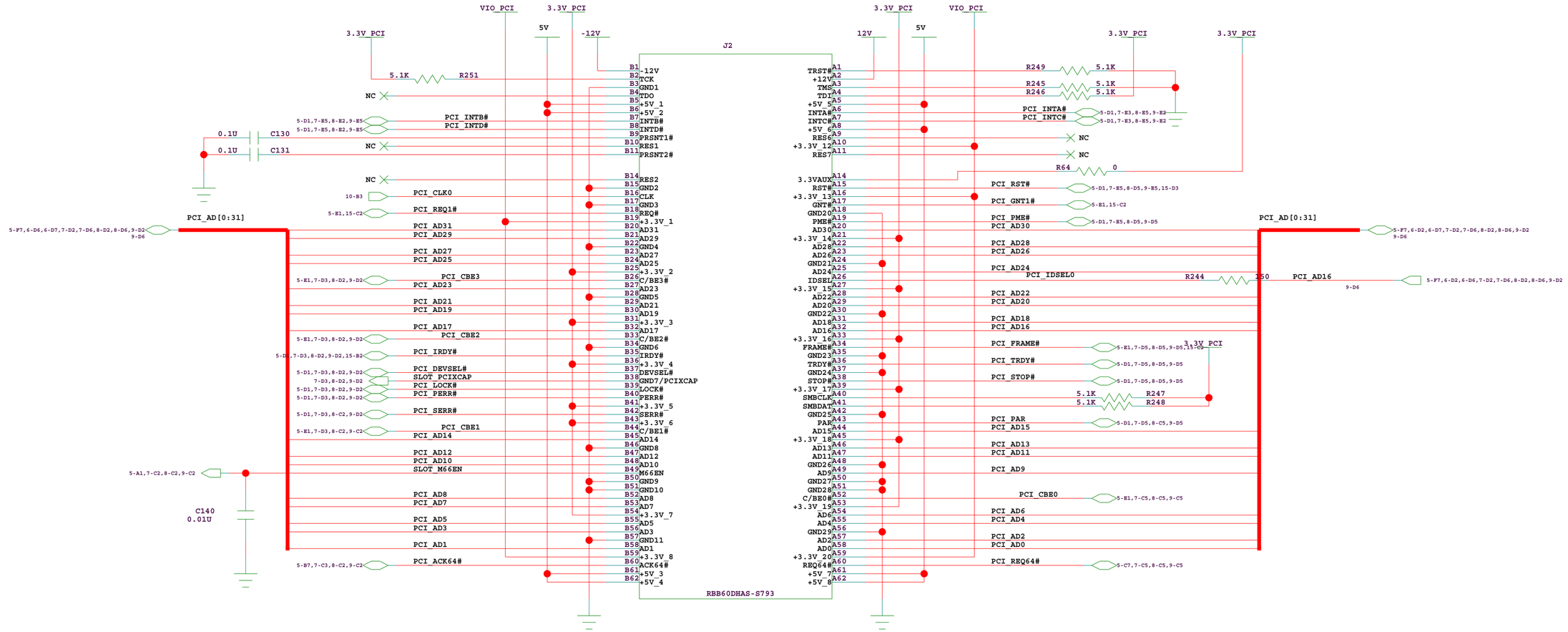
  INTB -> INTB

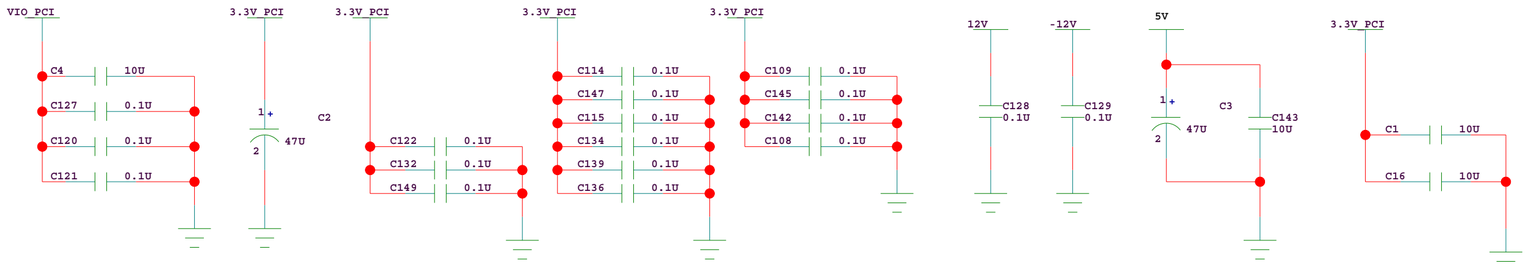
  INTC -> INTC

  INTD -> INTD

- PCI Clock PCI_CLK0

- PCI Arbitration PCI_GNT#1/PCI_REQ#1





TITLE : PCI SLOT 0

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60E2010_SC001	1.0	PHILIP LAUZON

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PCI SLOT 1 (Vertical)

IDSEL AD17

- Required Interrupt Routing

  SLOT : BRIDGE

  INTA -> INTB

  INTB -> INTC

  INTC -> INTD

  INTD -> INTA

- PCI Clock PCI_CLK1

- PCI Arbitration PCI_GNT#2/PCI_REQ#2

TITLE : PCI SLOT 1			
SIZE: C	DRAWING NUMBER : 60E2010_SC001	Version: 1.0	DESIGNER : PHILIP LAUZON
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PCI SLOT 3 (Vertical)

IDSEL AD18

- Required Interrupt Routing

  SLOT : BRIDGE

  INTA -> INTC

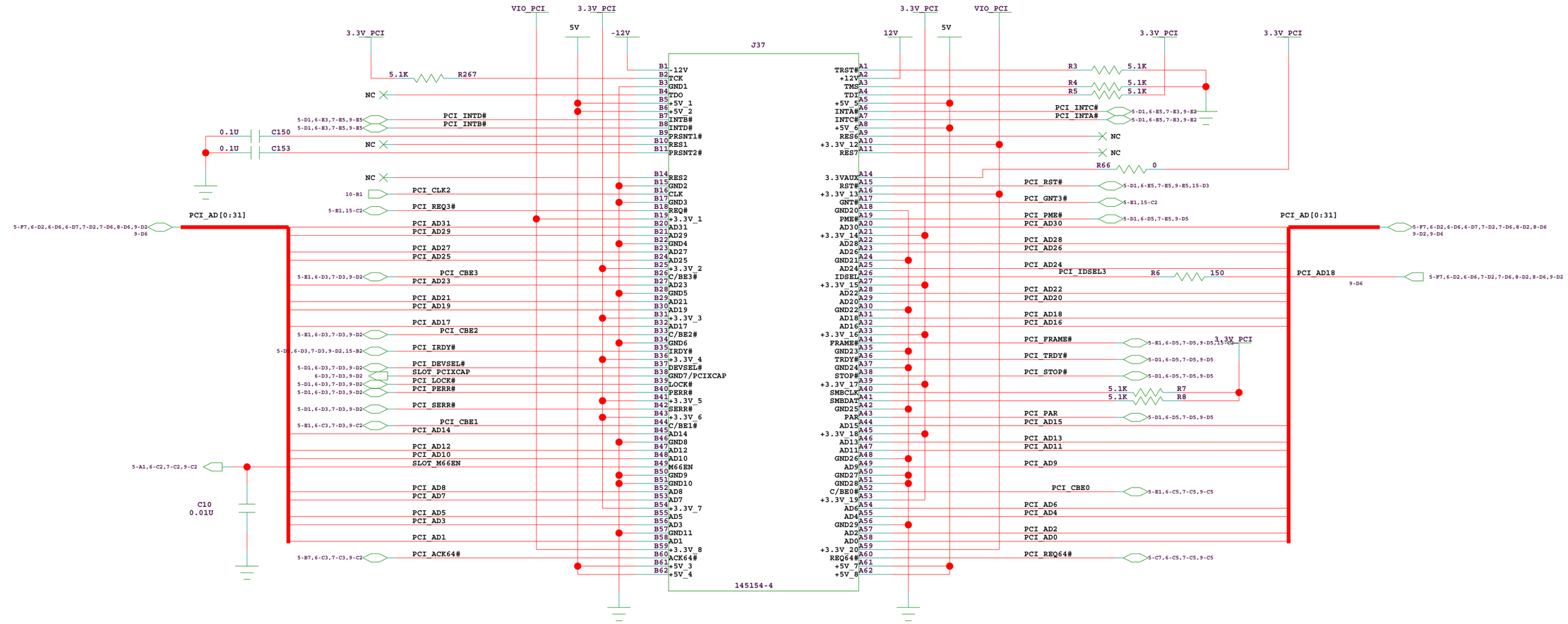
  INTB -> INTD

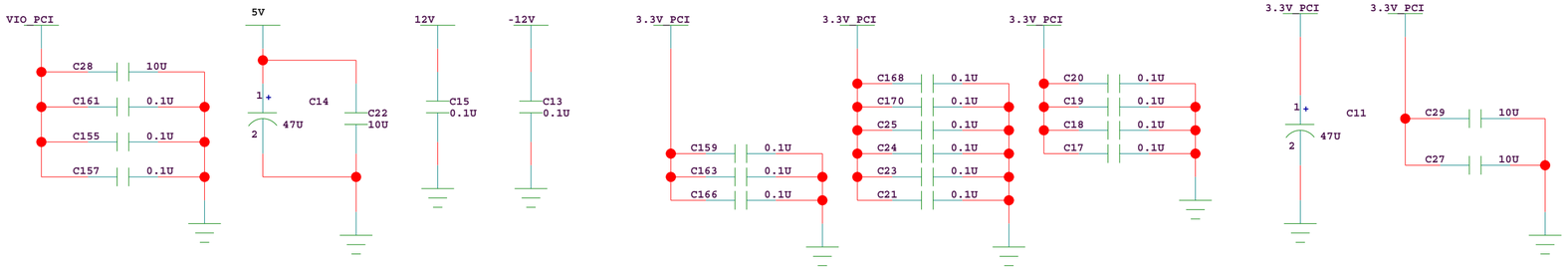
  INTC -> INTA

  INTD -> INTB

- PCI Clock PCI_CLK2

- PCI Arbitration PCI_GNT#3/PCI_REQ#3





TITLE : PCI SLOT 3			
SIZE: C	DRAWING NUMBER : 60E2010_SC001	Version: 1.0	DESIGNER : PHILIP LAUZON
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PCI SLOT 2 (Vertical)

IDSEL AD19

- Required Interrupt Routing

  SLOT : BRIDGE

  INTA -> INTD

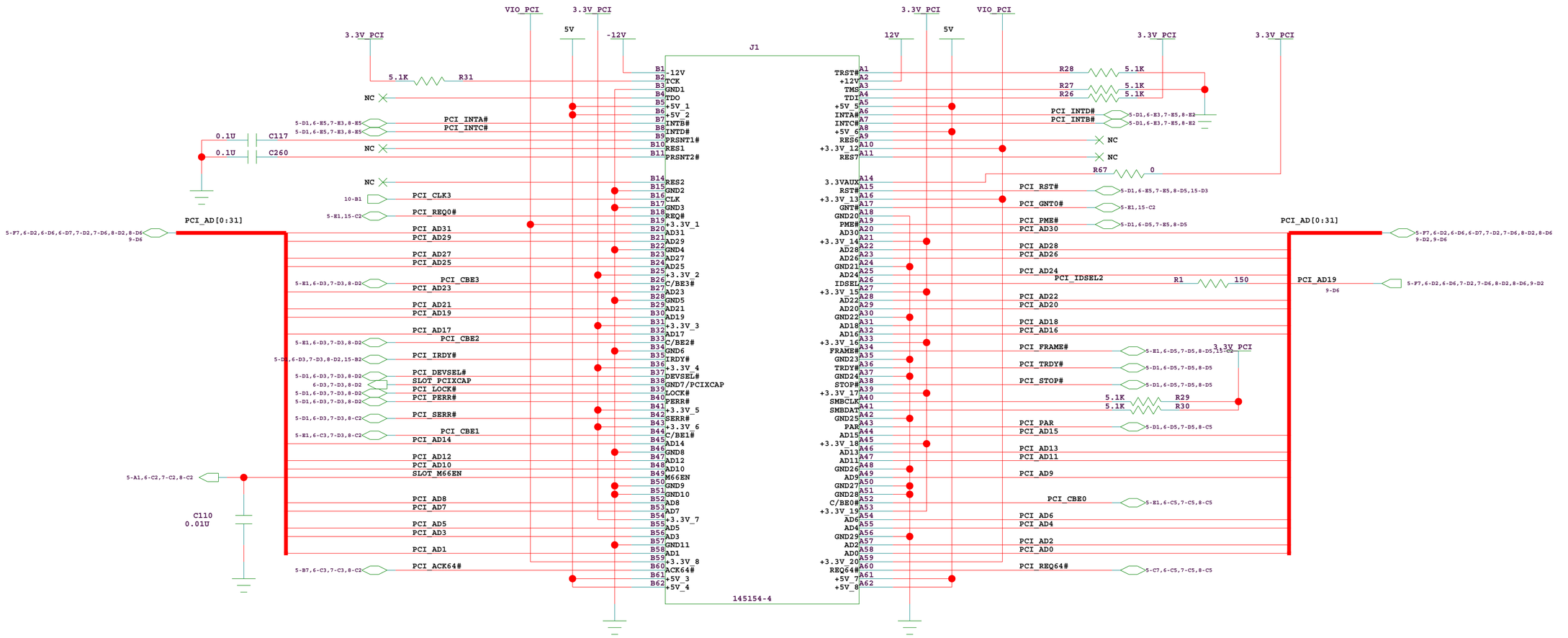
  INTB -> INTA

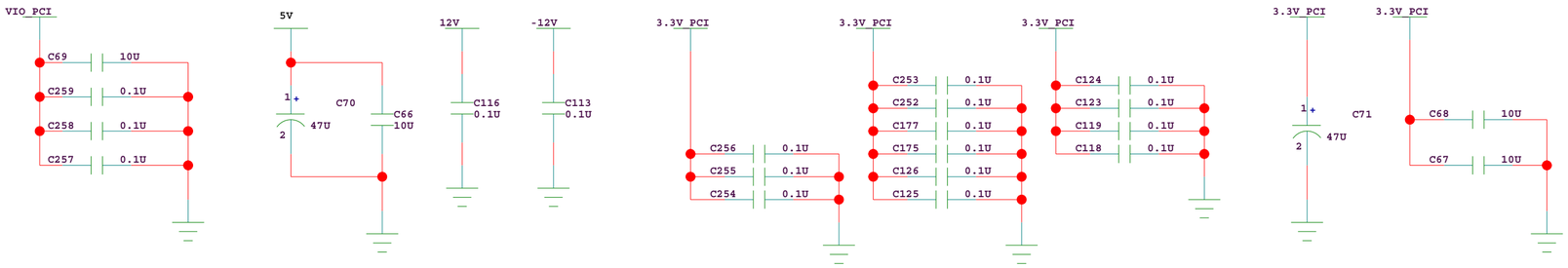
  INTC -> INTB

  INTD -> INTC

- PCI Clock PCI_CLK3

- PCI Arbitration PCI_GNT#0/PCI_REQ#0





TITLE : PCI SLOT 2			
SIZE C	DRAWING NUMBER : 60E2010_SC001	Version: 1.0	DESIGNER : PHILIP LAUZON
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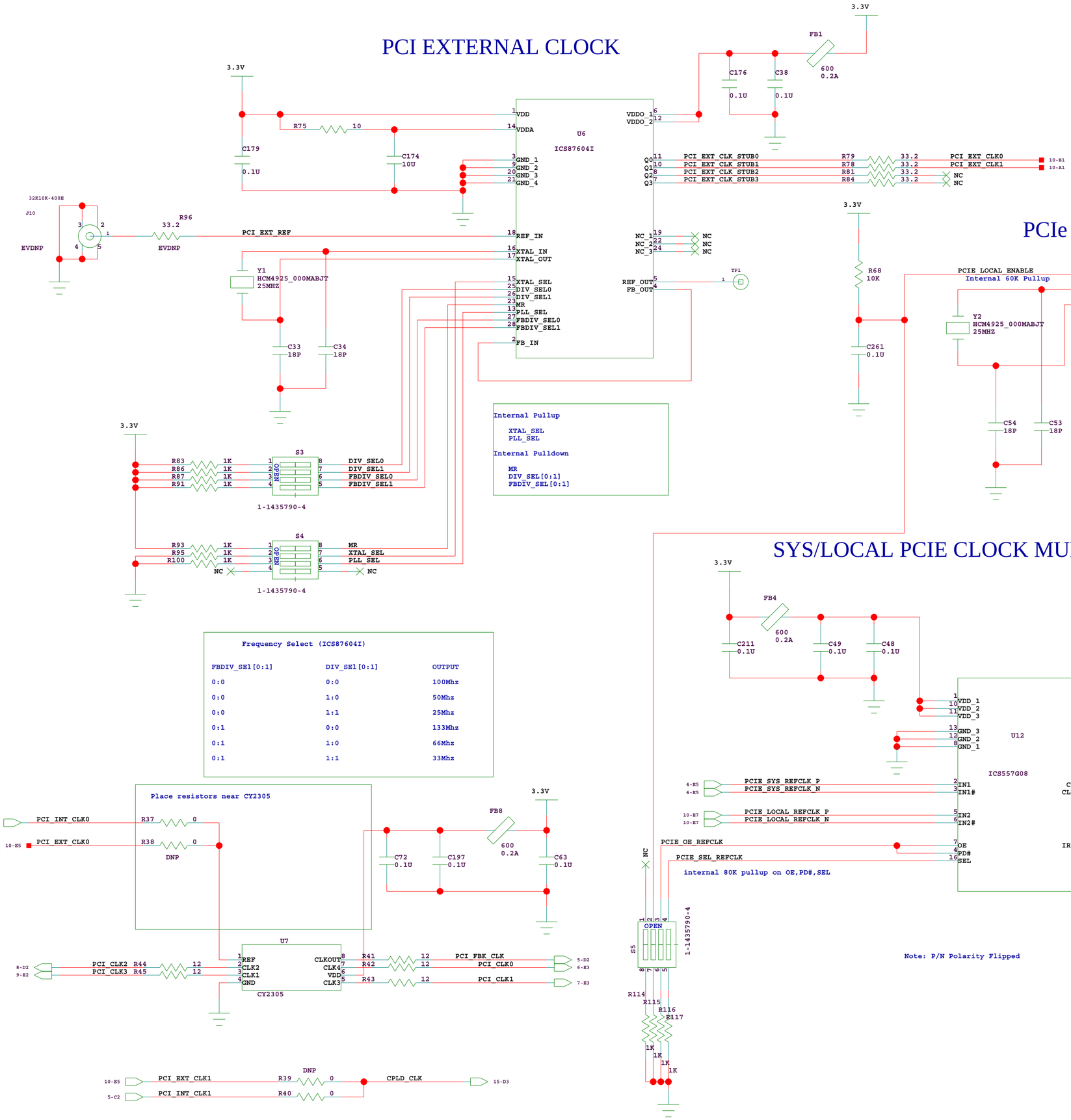
CLOCK DISTRIBUTION

PCI EXTERNAL CLOCK

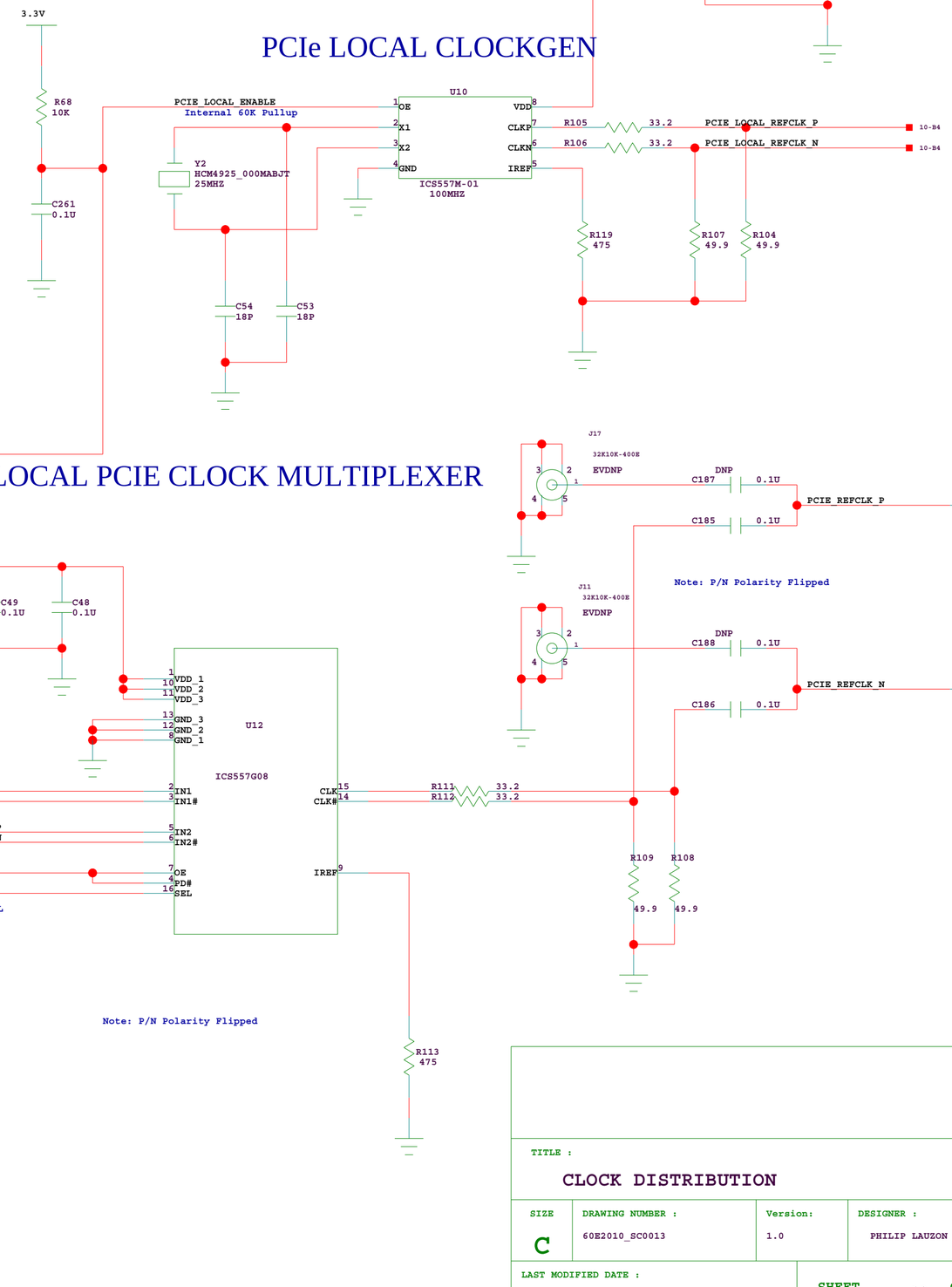


Frequency Select (ICS87604I)

FBDIV_SEl[0:1]	DIV_SEl[0:1]	OUTPUT
0:0	0:0	100Mhz
0:0	1:0	50Mhz
0:0	1:1	25Mhz
0:1	0:0	133Mhz
0:1	1:0	66Mhz
0:1	1:1	33Mhz

Place resistors near CY2305

PCIe LOCAL CLOCKGEN



SYS/LOCAL PCIE CLOCK MULTIPLEXER

TITLE : CLOCK DISTRIBUTION			
SIZE: C	DRAWING NUMBER : 60E2010_SC0013	Version: 1.0	DESIGNER : PHILIP LAUZON
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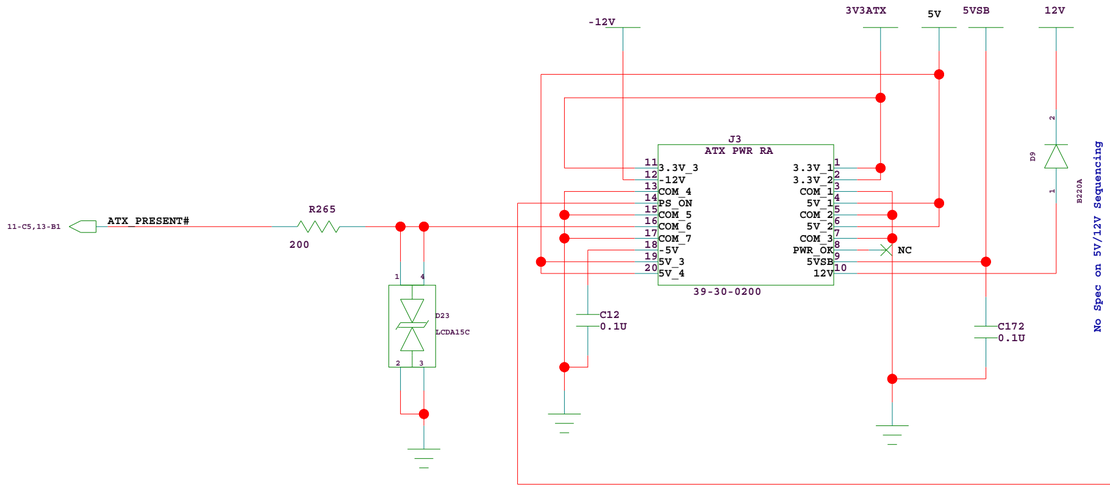
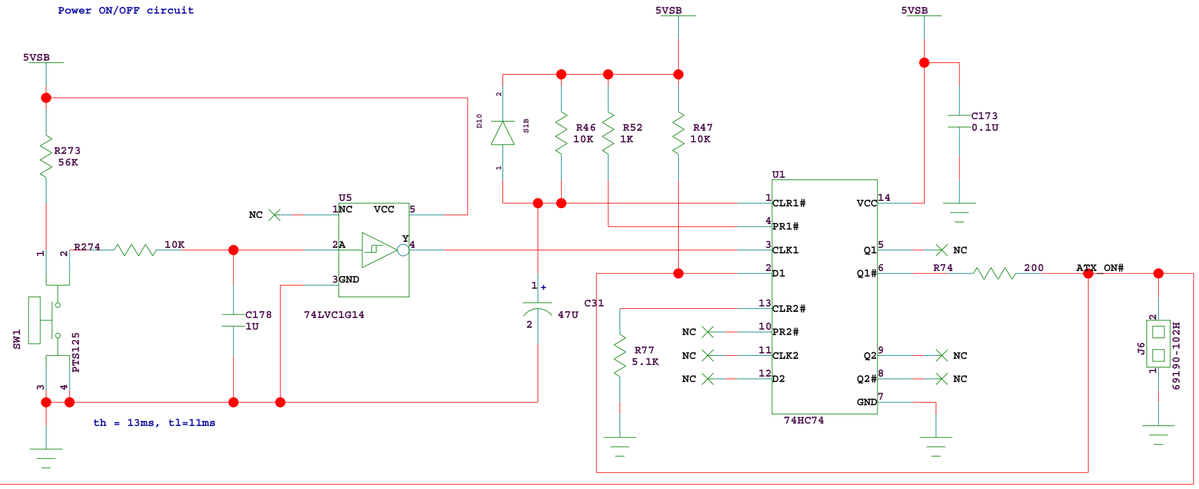
POWER SOURCES

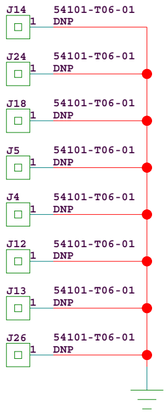
ATX

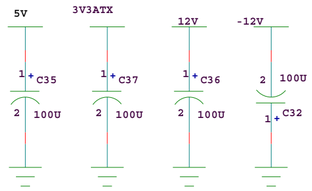


ATX SUPPLY TOGGLE

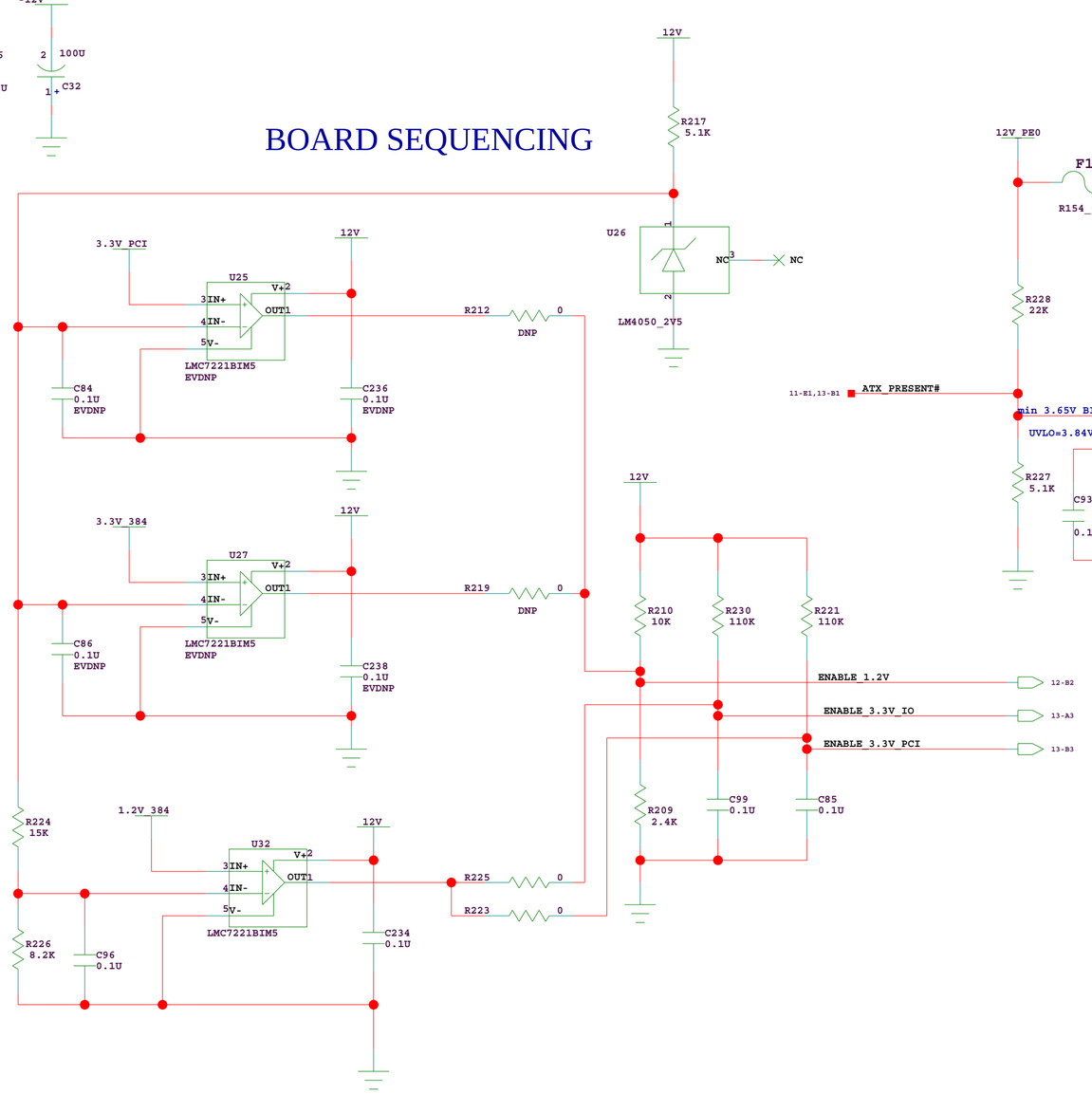


GND TESTPOINTS

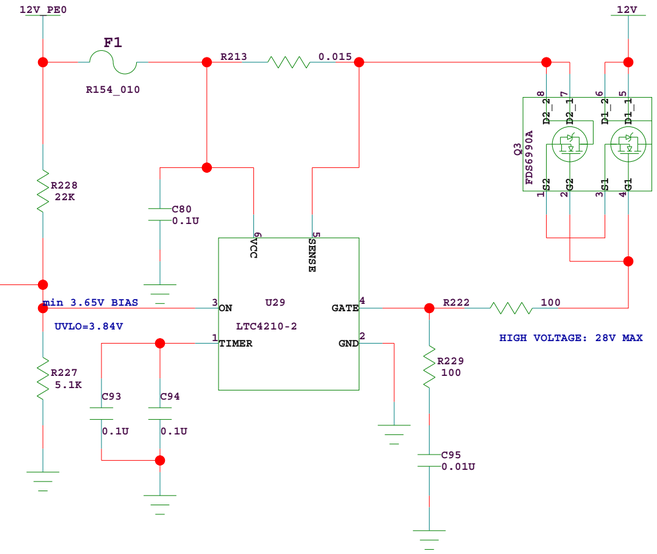




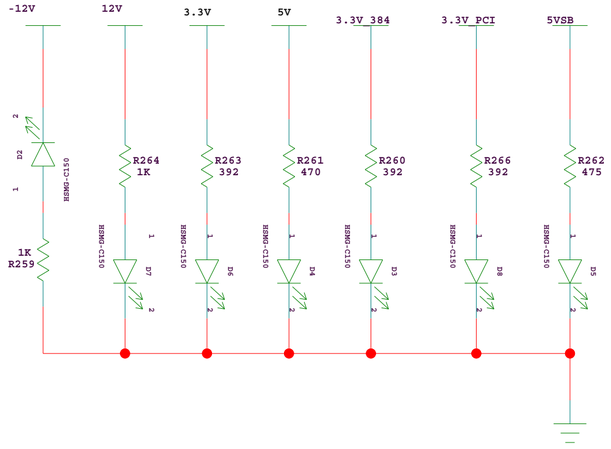
BOARD SEQUENCING



SYS SUPPLY SWITCH



POWER STATUS



TITLE : POWER SOURCES			
SIZE C	DRAWING NUMBER : 60E2010_SC001	Version: 1.0	DESIGNER : PHILIP LAUZON
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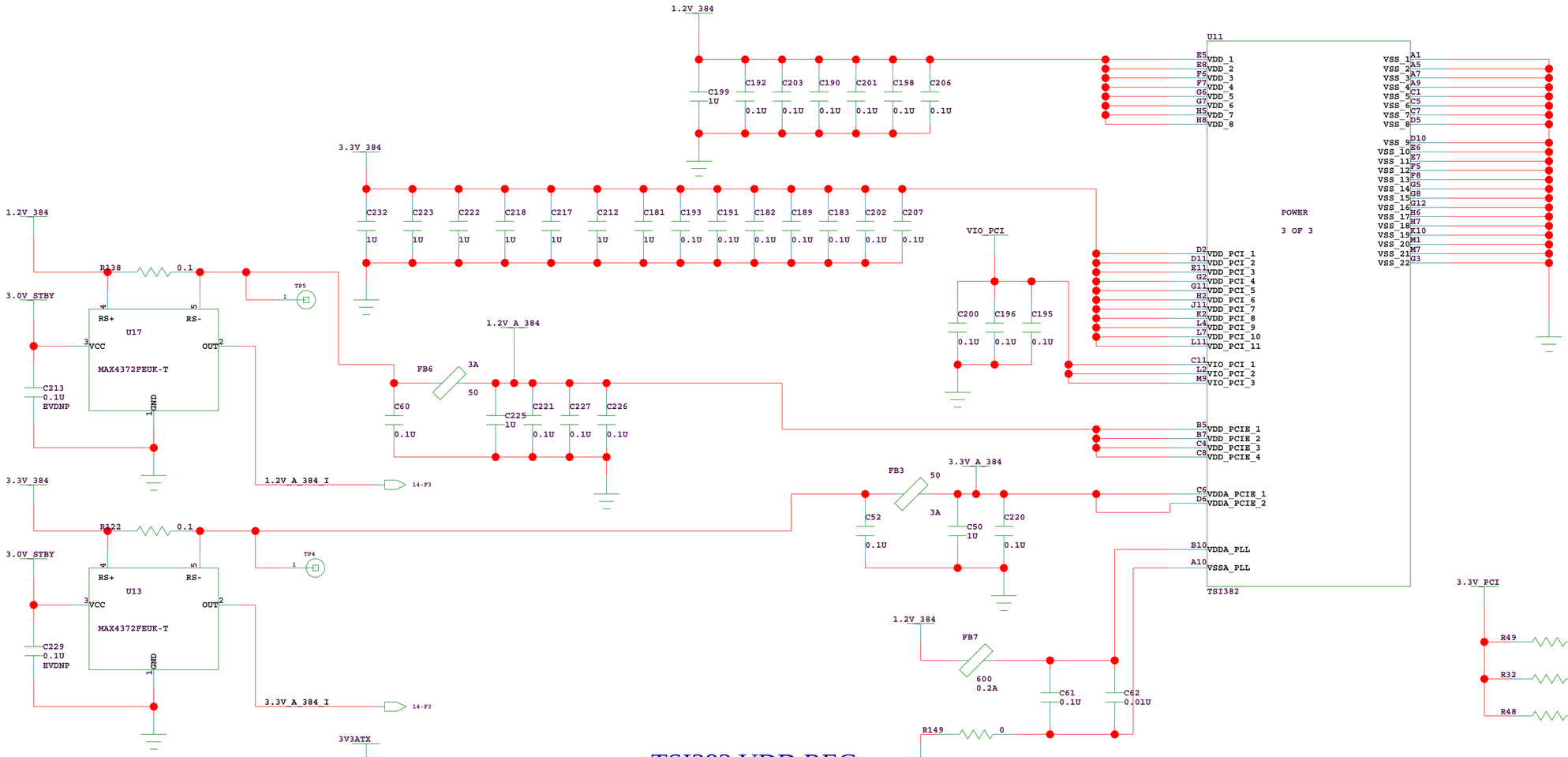
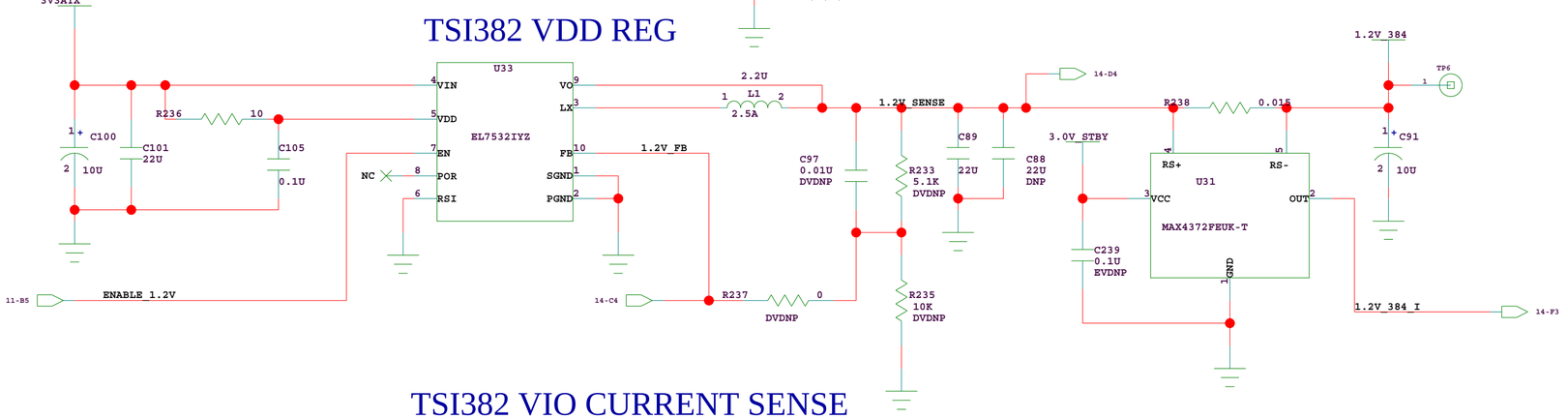
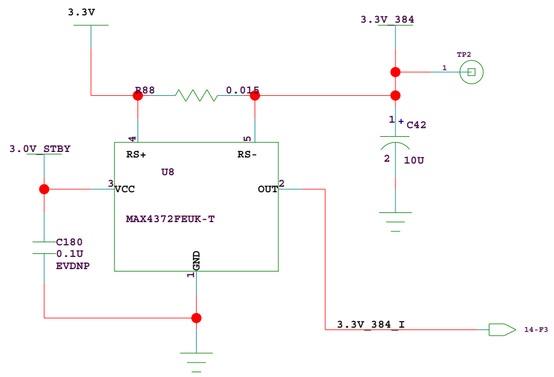
TSI382 POWER/REGULATORS



TSI382 VDD REG



TSI382 VIO CURRENT SENSE



TITLE :

TSI382 POWER/REGULATORS

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60E2010_SC001	1.0	PHILIP LAUZON

LAST MODIFIED DATE :

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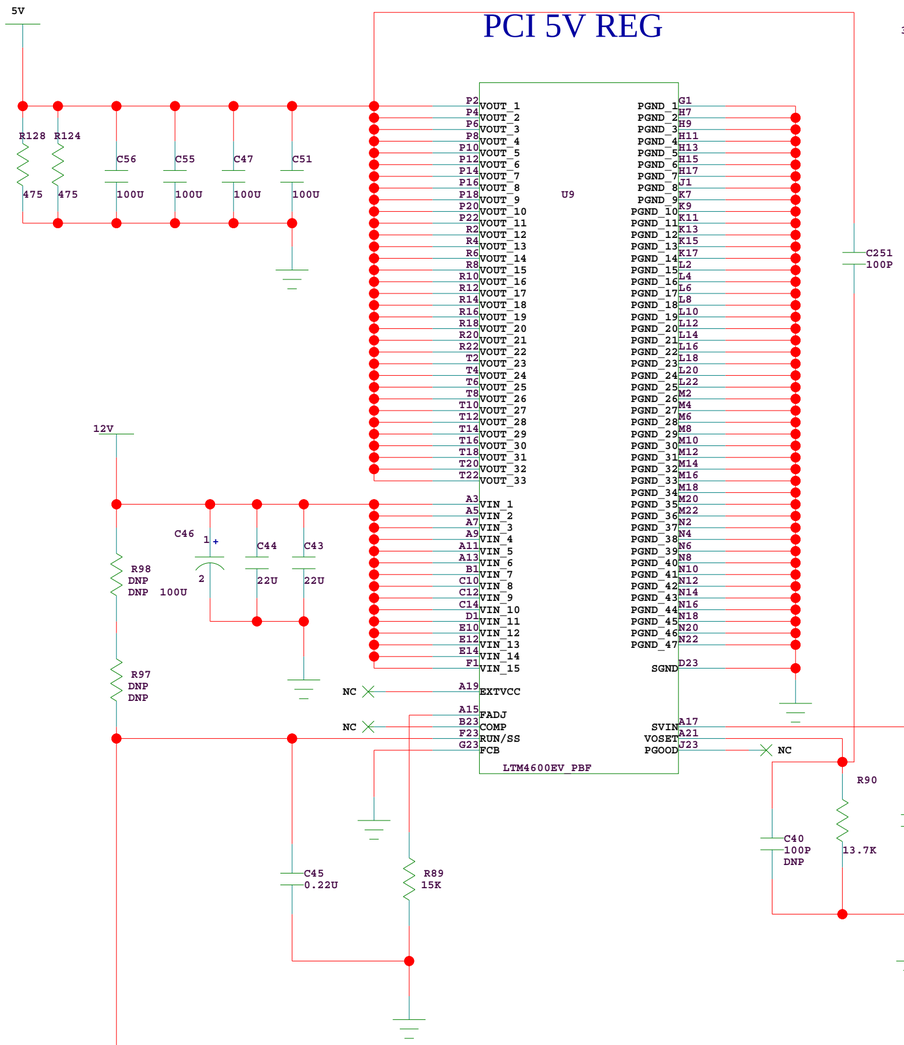
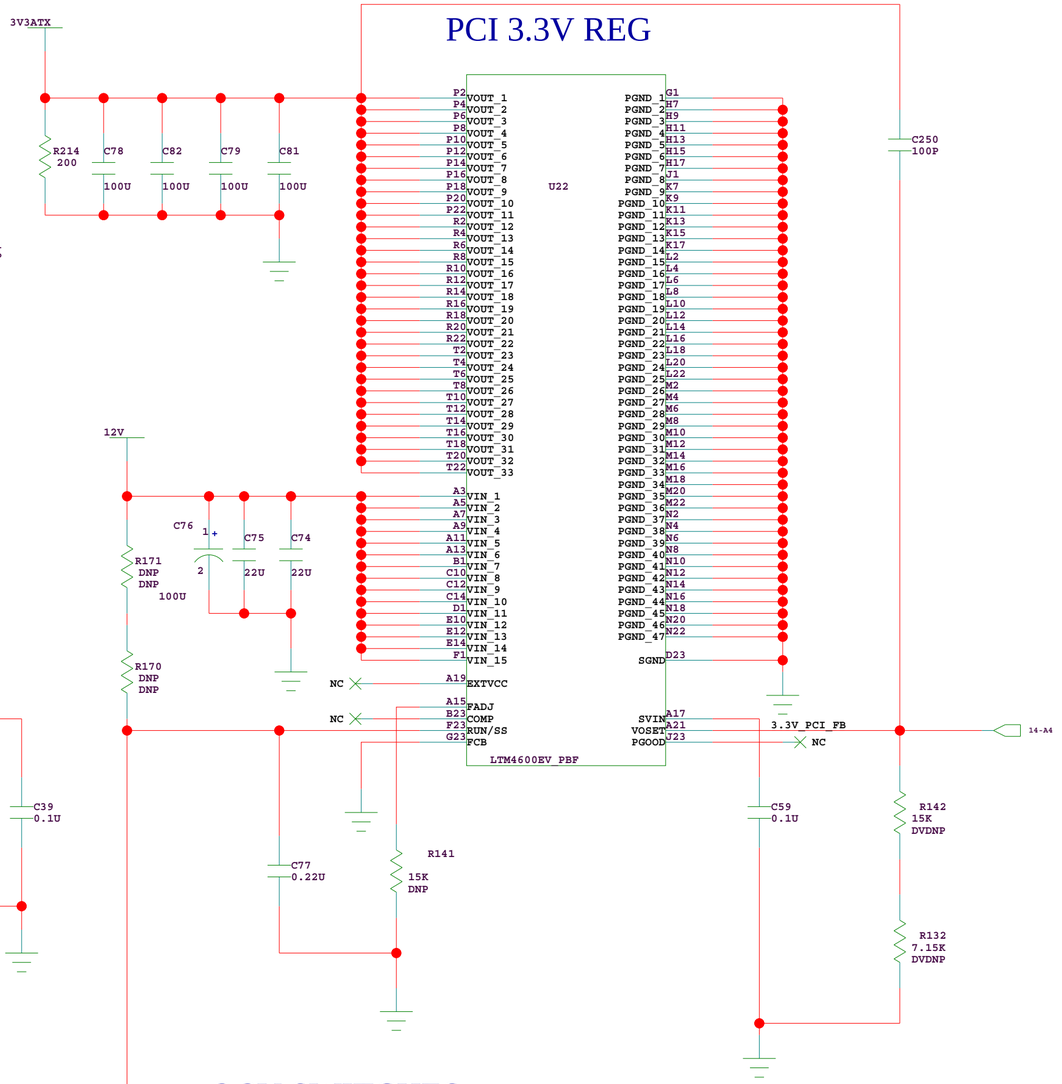
PCI POWER REGULATORS

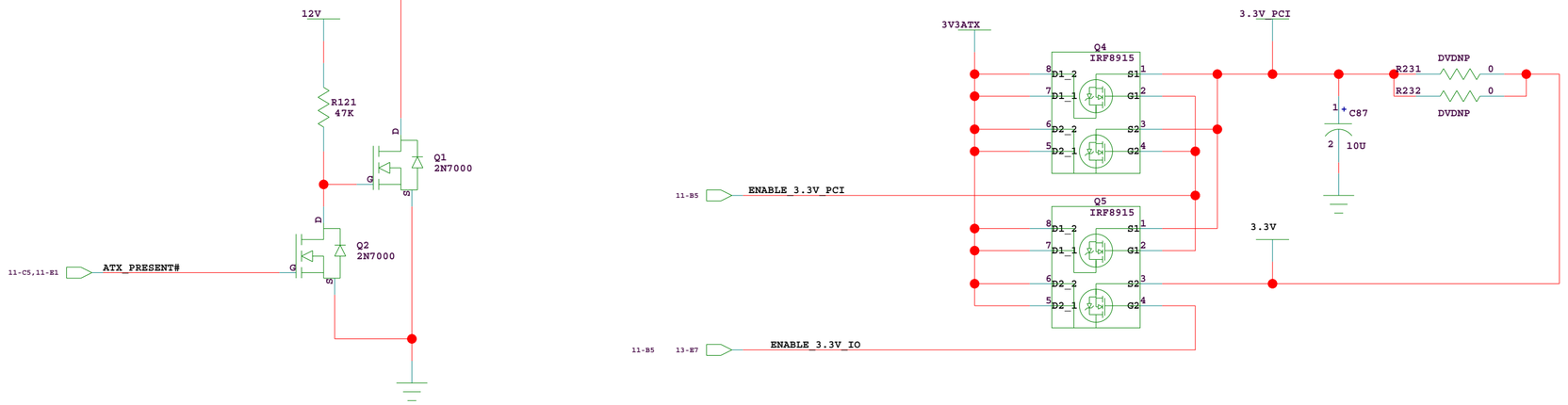
PCI 5V REG



PCI 3.3V REG



3.3V SWITCHES



TITLE :

PCI POWER REGULATORS

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60E2010_SC001	1.0	PHILIP LAUZON

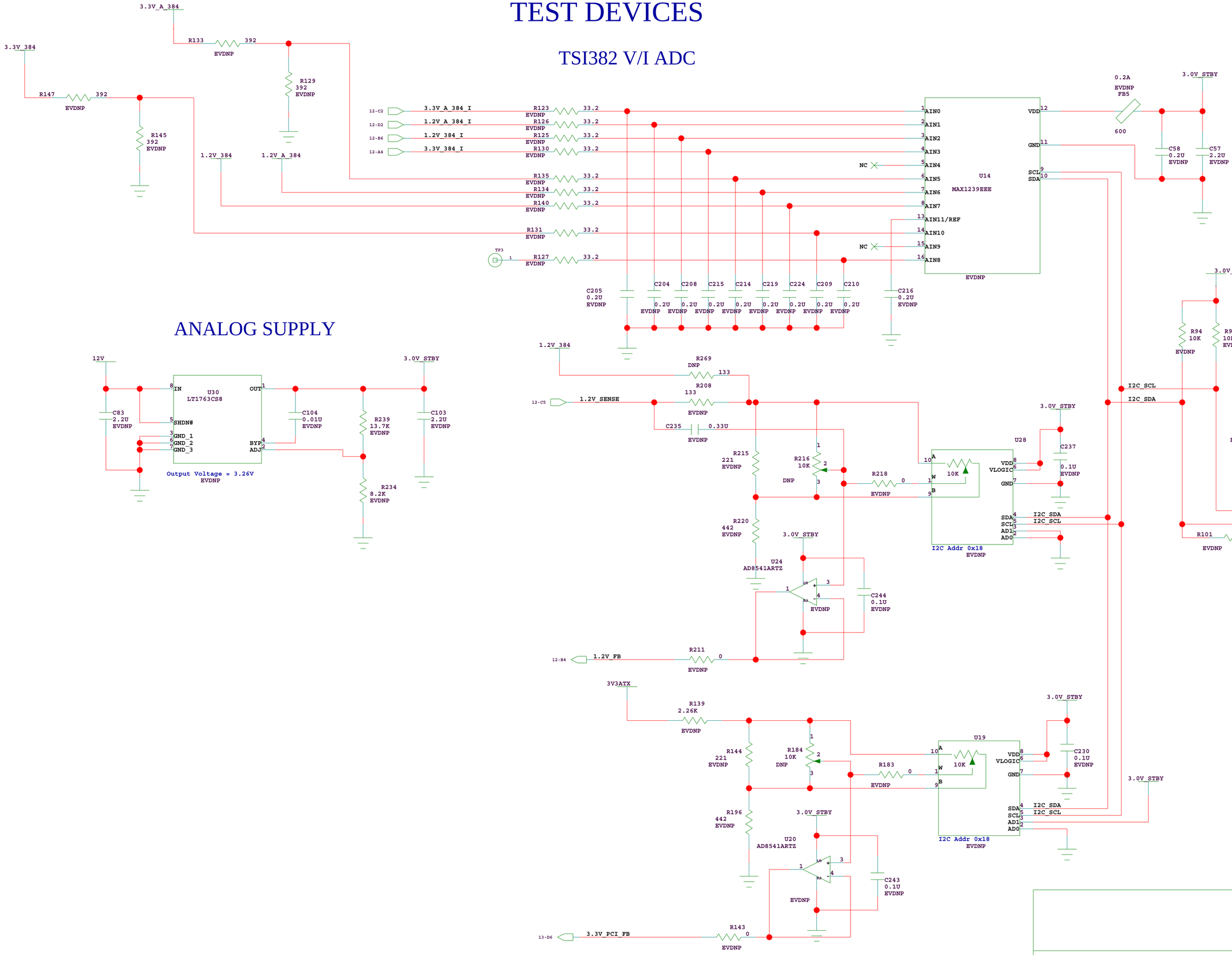
LAST MODIFIED DATE :

9-24-2007_9:40

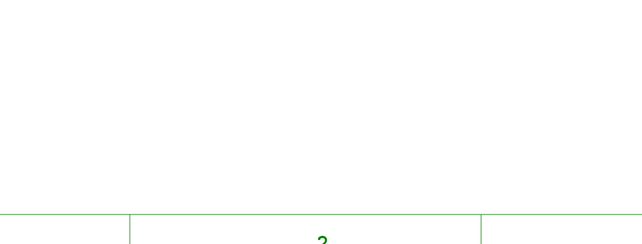
SHEET 13 OF 15

TEST DEVICES

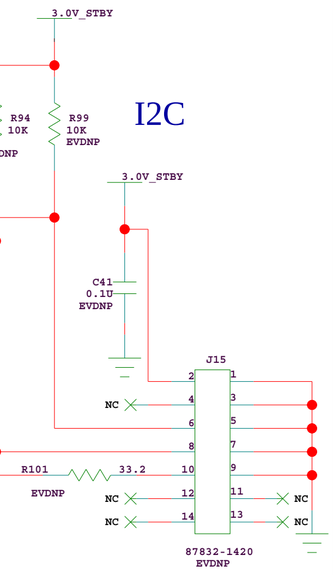
TSI382 V/I ADC



ANALOG SUPPLY



I2C



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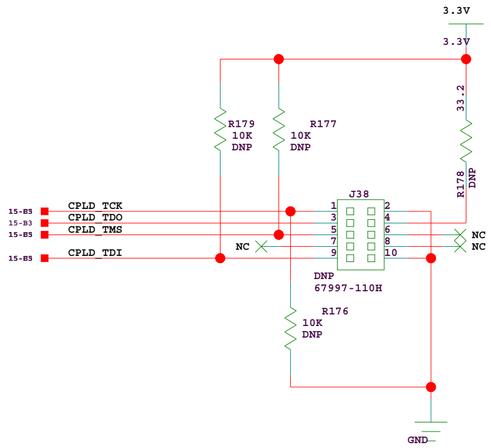
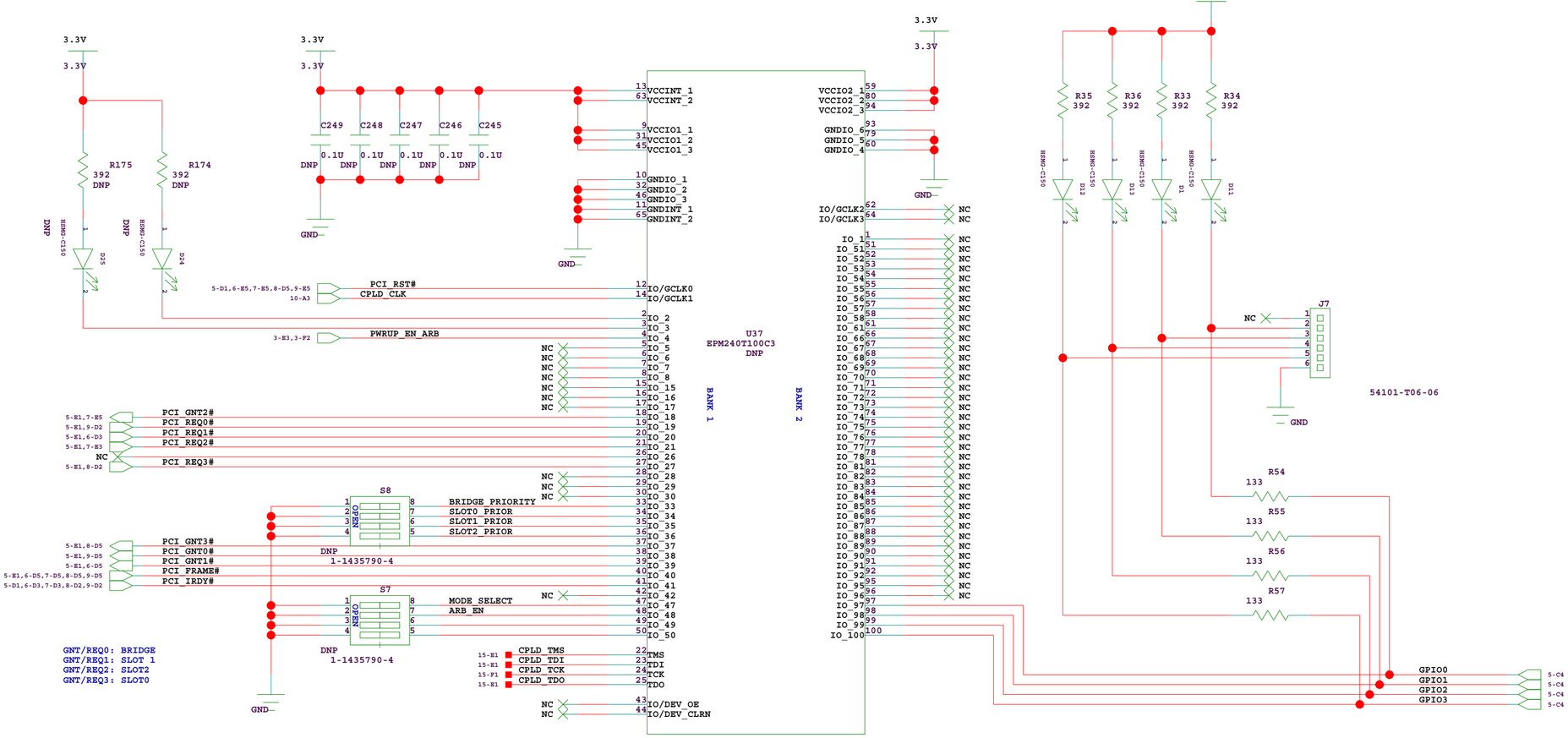
SIZE C	DRAWING NUMBER : 60E2010_SC001	Version: 1.0	DESIGNER : PHILIP LAUZON
LAST MODIFIED DATE : 10-3-2007_16:33		SHEET 14 OF 15	

TEST DEVICES CONT'D

PCIARBITER/GPIO CONTROL





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SIZE: C	DRAWING NUMBER : 60E2010_SC001	Version: 1.0	DESIGNER : PHILIP LAUZON
LAST MODIFIED DATE : 9-24-2007_9:40		SHEET 15 OF 15	