

## Description

The 4DB0232KD1 is a JEDEC compliant DDR4 Data Buffer with dual 4-bit bidirectional “DQ” data registers and “DQS” differential strobes. It is designed for 1.2 VDD operation in DDR4 LRDIMM applications. The DQ host interface side of each 4-bit bidirectional data register is connected to a memory controller while the MDQ interface side is connected to two x4 DRAMs.

All DQ and MDQ inputs are pseudo-differential with an internal voltage reference. All DQ and MDQ output drivers use external VDD termination and are optimized to drive single or dual terminated traces in DDR4 LRDIMM and NVDIMM-P applications. The differential DQS and MDQS strobes are used to synchronously sample the DQ and MDQ 4-bit data at the receiving end and are regenerated and driven by the DDR4 Data Buffer alongside the DQ and MDQ outputs on the opposite side of the device.

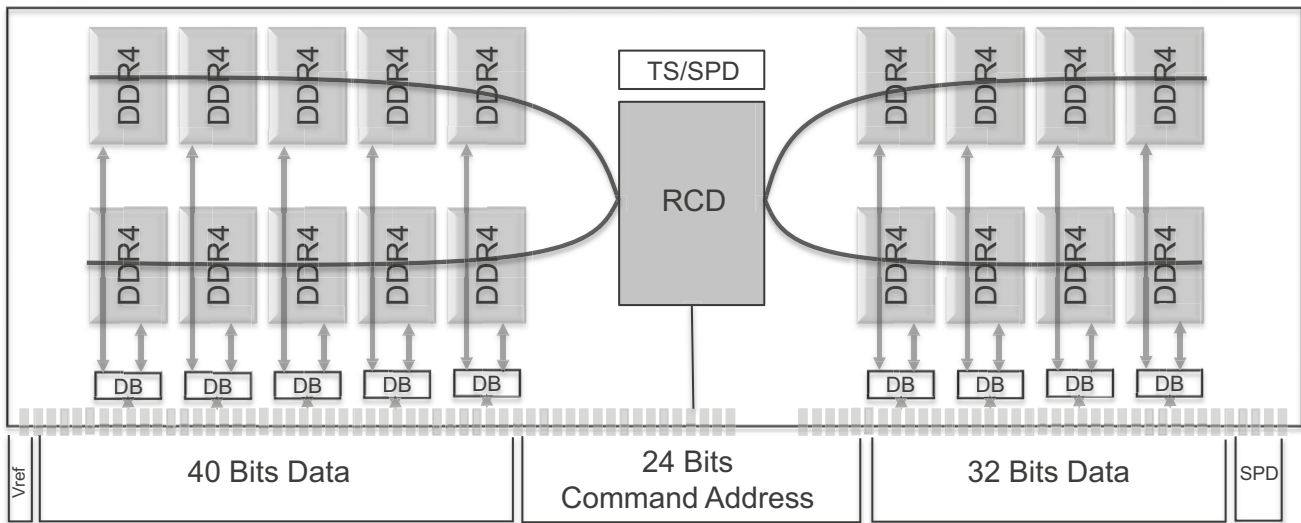
The 4DB0232KD1 also has a control bus interface that is used to synchronously receive control commands from Renesas’ DDR4 Register at data rate speeds (e.g., in LRDIMM applications). This interface is commonly referred to as the BCOM bus. It consists of a 4-bit control bus BCOM[3:0], two dedicated control signals BCKE and BODT, a voltage reference input, and a differential clock input BCK\_t/BCK\_n.

The 4DB0232KD1 supports dedicated pins for ZQ calibration and for parity error alerts.

## Features

- All DDR4 data rates from 1600MT/s to 3200MT/s
- *DDR4DB02 JEDEC Specification r1.0* compliant
- Supports all JEDEC LRDIMM raw card types
- Lower power dissipation reduces dependency on heat sinks in standard server configurations
- 3.0 × 7.5 mm body, 0.5 × 0.5 mm ball pitch, 14 × 5 grid, 53-CVBGA, optimized for DDR4 LRDIMM PCB layout
- Guaranteed operation at commercial grade temperatures

## Block Diagram



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