This is a short form datasheet and is intended to provide an overview only. Additional details are available from Renesas. Contact information may be found on the last page.

FEATURES

HIGHLIGHTS

- Features 15 mHz to 560 Hz bandwidth
- Provides node clock for ITU-T G.8261/G.8262 Synchronous Ethernet (SyncE)
- Supports GR-253-CORE (OC-192) and ITU-T G.813 (STM-64) jitter generation requirements
- Provides clocks for 1 Gigabit and 10 Gigabit Ethernet applications

MAIN FEATURES

- Provides an integrated single-chip solution for Synchronous Equipment Timing Source, including Stratum 3, 4E, 4, SMC, EEC-Option 1 and EEC-Option 2 Clocks
- Supports 1PPS input and output
- Employs PLL architecture to feature excellent jitter performance and minimize the number of external components
- Supports programmable DPLL bandwidth (15 mHz to 560 Hz) and damping factor (1.2 to 20 in 5 steps)
- Supports $1.1X10^{-5}$ ppm absolute holdover accuracy and $4.4X10^{-8}$ ppm instantaneous holdover accuracy
- Provides 2 differential output clocks whose frequencies cover from 1Hz (1PPS) to 644.53125 MHz
  - Includes 25 MHz, 125 MHz and 156.25 MHz for CMOS outputs
  - Includes 25.78125 MHz, 128.90625 MHz and 161.1328125 MHz for CMOS outputs
  - Includes 25 MHz, 125 MHz, 156.25 MHz, 312.5 MHz and 625 MHz for differential outputs
  - Includes 25.78125 MHz, 128.90625 MHz, 161.1328125 MHz, 322.265625 MHz and 644.53125 MHz for differential outputs
- Provides 1 single ended output clock whose frequencies cover from 1 Hz (1PPS) to 156.25 MHz
- Provides 2 differential input clocks whose frequency cover from 1 Hz (1PPS) to 625 MHz
  - Includes 25 MHz, 125 MHz and 156.25 MHz for CMOS inputs
  - Includes 25 MHz, 125 MHz, 156.25 MHz, 312.5 MHz and 625 MHz for differential inputs
- Provides 1 single ended input clock whose frequencies cover from 1 Hz (1PPS) to 156.25 MHz
- Supports Forced or Automatic operating mode switch controlled by an internal state machine
- Automatic state machine supports Free- Run, Locked and Holdover
- Supports manual and automatic selected input clock switch
- Supports automatic hitless selected input clock switch on clock failure
- Supports Telcordia GR-1244-CORE, Telcordia GR-253-CORE, ITU-T G.812, ITU-T G.8262, ITU-T G.813 and ITU-T G.783 recommendations

OTHER FEATURES

- Microprocessor interface modes: I2C and Serial
- IEEE 1149.1 JTAG Boundary Scan
- Single 3.3 V operation with 5 V tolerant CMOS I/Os
- 72-pin QFN package, green package options available

APPLICATIONS

- 1 Gigabit Ethernet and 10 Gigabit Ethernet
- Synchronous Ethernet equipment
- Core and access IP switches / routers
- Gigabit and terabit IP switches / routers
- IP and ATM core switches and access equipment
- Broadband and multi-service access equipment

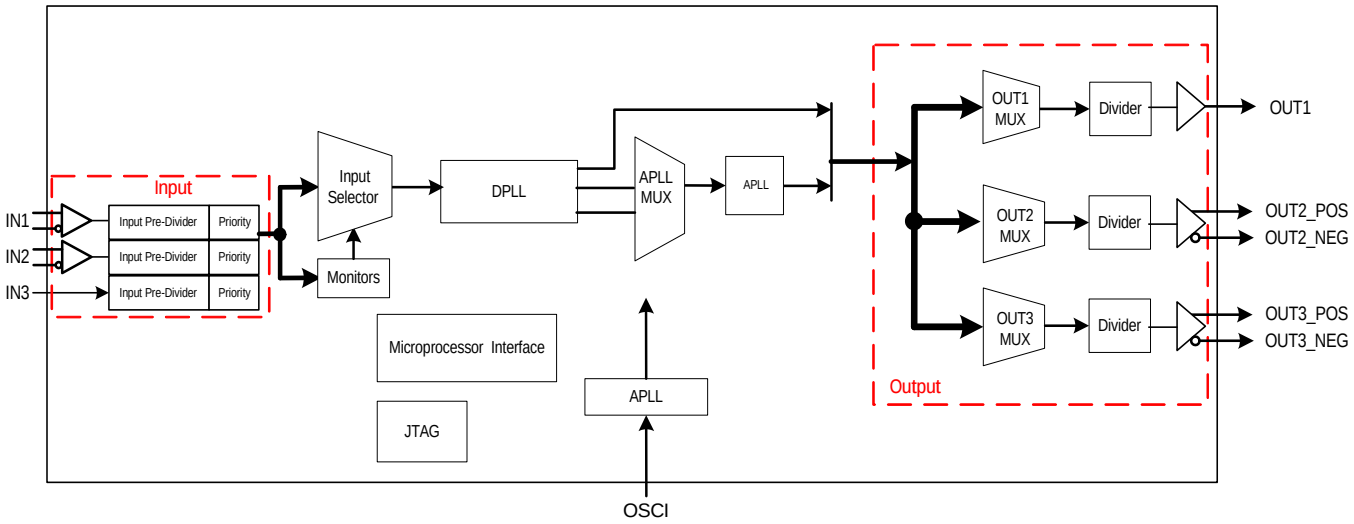


Figure 1. Functional Block Diagram

DESCRIPTION

The 8V89307 is an integrated solution for the Synchronous Equipment Timing Source supporting EEC-Option1, EEC-Option2 clocks in Synchronous Ethernet equipment.

The device has a high quality DPLL to provide system clocks for node timing synchronization within a Synchronous Ethernet network. It also integrates an APLL for better jitter performance.

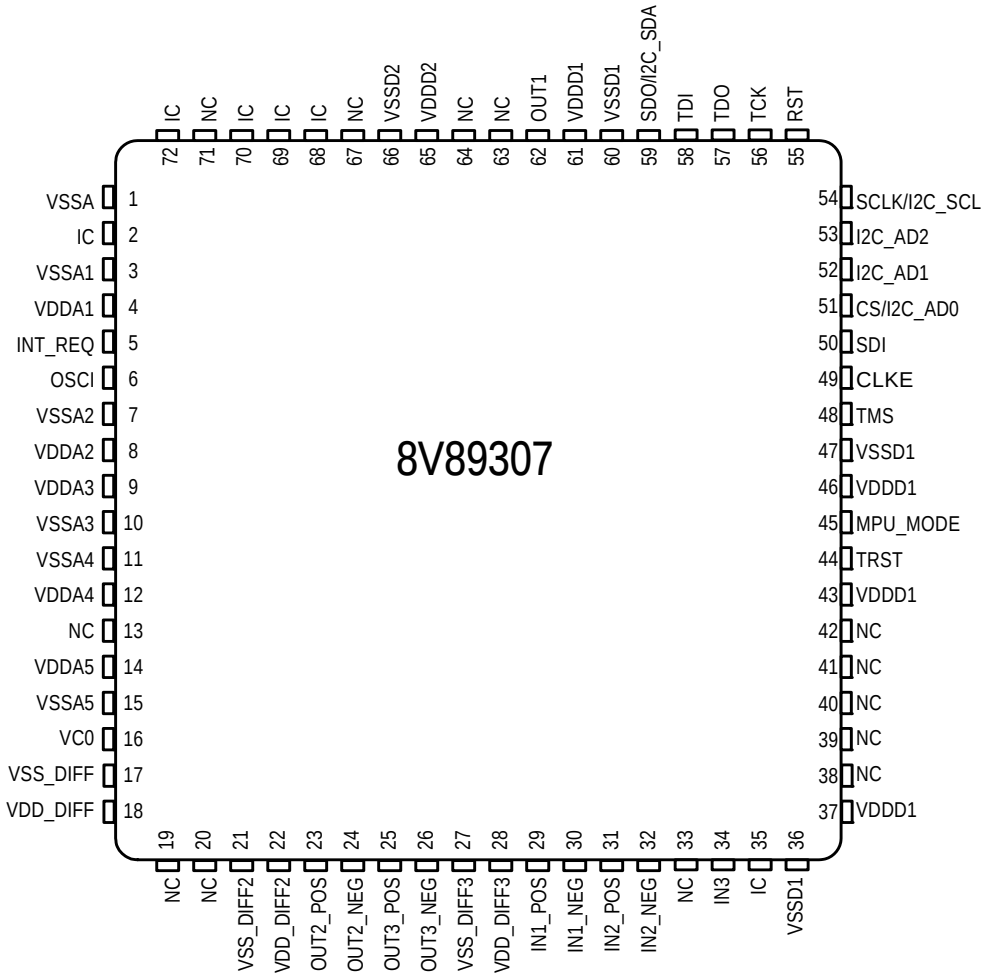
An input clock is automatically or manually selected. It supports three primary operating modes: Free-Run, Locked and Holdover. In Free-Run mode, the DPLL refers to the master clock. In Locked mode, the DPLL locks to the selected input clock. In Holdover mode, the DPLL resorts to the frequency data acquired in Locked mode. Whatever the operating mode is, the DPLL gives a stable performance without being affected by operating conditions or silicon process variations.

The device provides programmable DPLL bandwidths: 15 mHz to 560 Hz and damping factors: 1.2 to 20 in 5 steps. Different settings cover all clock synchronization requirements.

A stable oscillator is required for the master clock in different applications. The master clock is used as a reference clock for all the internal circuits in the device. It can be calibrated within ±741 ppm.

All the read/write registers are accessed through a microprocessor interface. The device supports Serial and I2C interfaces.

1 PIN ASSIGNMENT



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