

DA14195

Audio Processor with ARM, HiFi-3, USB, and Power Management

This short datasheet is an addendum to the DA14195 datasheet.

The DA14195 is a low-power CMOS IC audio processor, optimized for applications like USB headset, headphones, and Bluetooth headsets. It features Arm M0, Tensilica HiFi-3 DSP, integrated battery management, clock oscillators, various digital audio interfaces like USB 2.0, I2S and SPDIF. Program storage resides in a 6-pin Quad SPI (QSPI) Serial Flash.

Key Features

- Processing power
 - 32 kHz up to 165.888 MHz 32-bit Arm[®] Cortex[®]-M0 with 8 kB I/D 4-way associative cache
 - 290.304 MHz 32 bits Tensilica LX4/HiFi-3 DSP
 - 3 Stereo Hardware Sample Rate converter
 - 4 ch SYS-DMA, 12 ch DSP-DMA controllers
 - Crypto engine supporting AES128/256, ECB with CBC and CTR modes and HASH-256 with Random Number Generator, FIPS140-2 compliant
- Development/Debug support
 - Arm 2-wire SWD with 8 hardware breakpoints and 2 watch points
 - Arm instruction and DSP event trace
 - DSP debugger with 1 and 5-wire JTAG interfaces
- Memories
 - 64 kB shared System RAM
 - 256 kB multi bank shared DSP-RAM
 - 32 Byte OTP with factory programmed timestamp
- Power management
 - 1.9 to 5 V Battery voltage, 1.2 V Core voltage
 - Integrated DCDC step-down converter to 1.4 V
 - 4 Independent VDDIO pin groups 1.8 V to 3.45 V
 - Integrated Battery Charging circuit for Li-Ion/Li-Po with NTC protection circuit
- Analog interfaces
 - 2 input 10-bit ADC
 - Integrated Temperature sensor
 - Brown-out supply voltage detectors
- USB Charging detection (Complies with Battery Charging Specification, V1.2)
- Oscillators and PLLs
 - 26/20.736 MHz Crystal oscillator with low power mode
 - 16 MHz RC oscillator for low power mode
 - 32.768 kHz XTAL oscillator output
 - 32 kHz RC oscillator
 - 290.304 MHz SYS-PLL, 48 MHz PLL for USB
- Digital interfaces
 - USB 2.0 HS/FS Device MAC/PHY with DMA
 - 82.944 MHz.1.8-3.3 V Quad SPI interface
 - 27 I/Os with slope control and Programmable Pin Assignment
 - 3 backdrive protected PADs for LEDs
 - Keyboard interface with debouncing per pin.
 - 2 UART Full duplex 9.6-812.5 kBaud with FIFO DMA support and Hardware flow control
 - SPI[™] interface 20.736 MHz (Master/Slave).
 - I2C 100 kHz, 400 kHz (Master/Slave)
 - 2 PCM Interface, 2x32 bits, 192 kHz M/S, I2S.
 - 3x2 channel PDM I/O for digital microphones
 - S/PDIF analog/digital stereo I/O
- Dual 16-bit timers, triple PWM timer, 16-bit capture timer, dual watchdog timer, 32-bit real-time clock
- Temperature range -40 °C to +85 °C
- WLCSP81 0.4 mm pitch, VFBGA96 0.5 mm pitch

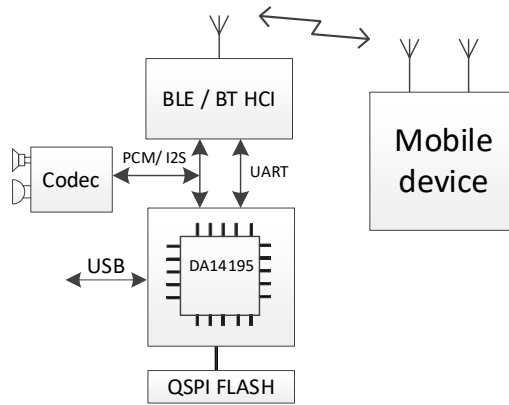


Figure 1. System diagram

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1. Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a maximum temperature of 30 °C and a maximum relative humidity of 60% RH, before the solder reflow process.

The WLCSP packages are qualified for MSL 1.

The VFBGA packages are qualified for MSL 3.

Table 1. MSL classification

MSL level	Floor lifetime
MSL 4	72 hours
MSL 3	168 hours
MSL 1	Unlimited at 30 °C/85% RH

1.1 WLCSP Handling

Manual handling of WLCSP packages should be reduced to the absolute minimum. In cases where it is still necessary, a vacuum pick-up tool should be used. In extreme cases, plastic tweezers can be used. Metal tweezers should not be used, because contact can easily damage the silicon chip. Removing the chip will damage the solder balls, so a removed sample cannot be reused. WLCSP is sensitive to visible and infrared light. Precautions should be taken to shield the chip properly at the final product.

1.2 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from <http://www.jedec.org>.

2. Package Outline Drawings

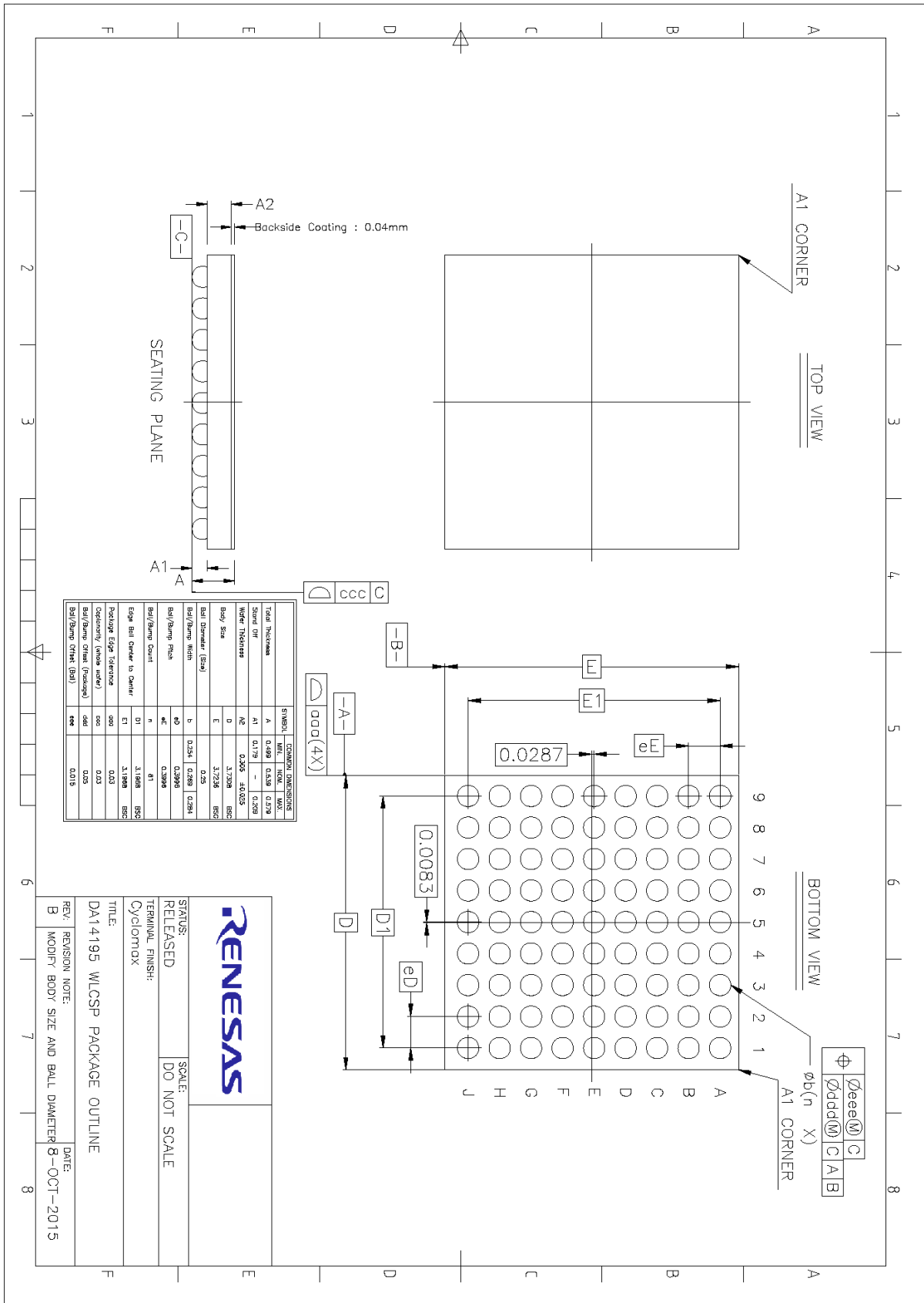


Figure 2. WLCSP81 package outline drawing

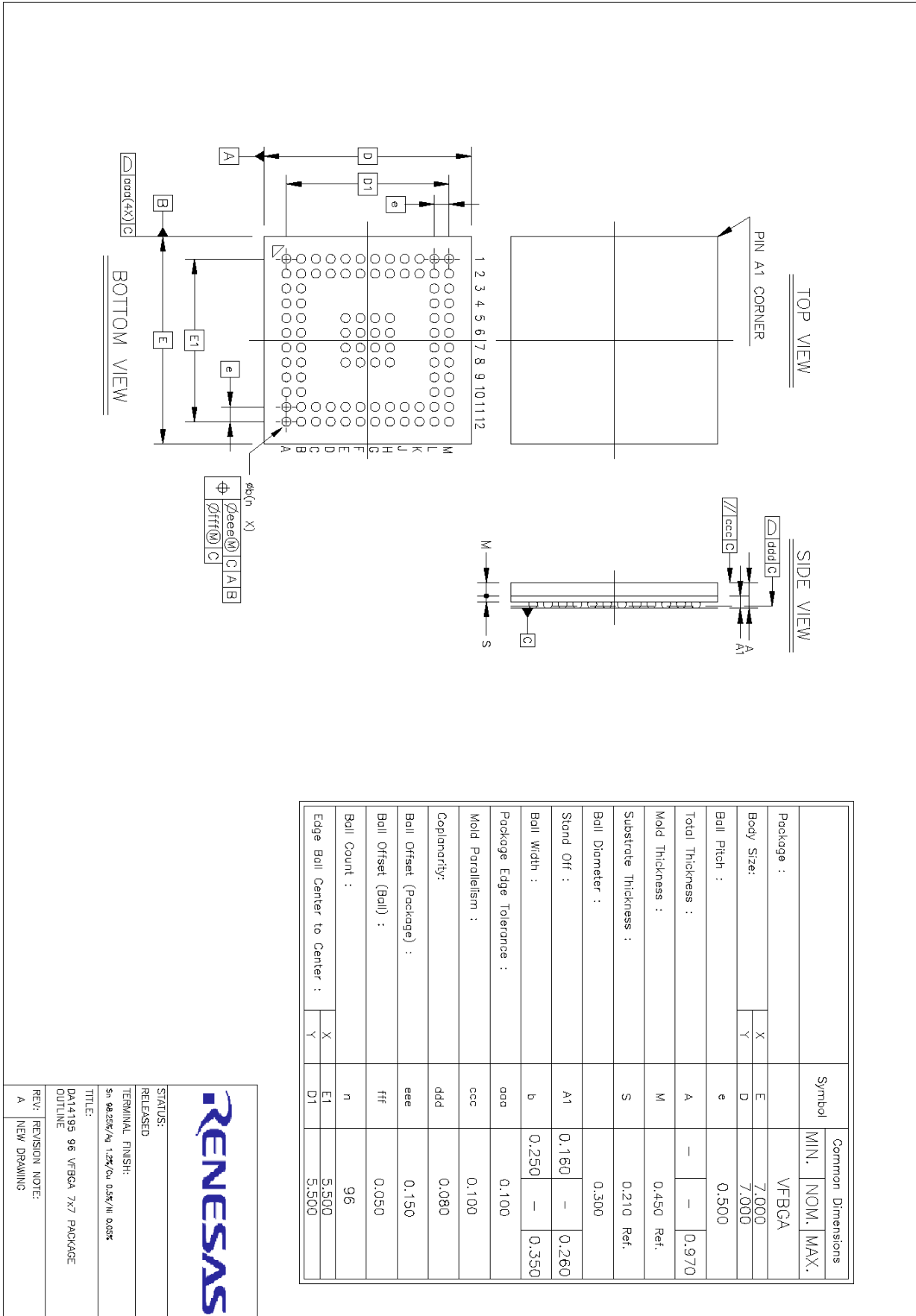


Figure 3. VFBGA96 package outline drawing

3. Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult your Renesas local sales representative.

Table 2. Ordering information (samples)

Part number	Package	Size (mm)	Shipment form	Pack quantities
DA14195-00VD2	WLCSP81	3.73 × 3.73 × 0.57	Reel	100/1000
DA14195-00HJ2	VFBGA96	7 × 7 × 0.97	Reel	100/1000
DA14195-00D01VD2	WLCSP81	3.73 × 3.73 × 0.57	Reel	100/1000
DA14195-00D01HJ2	VFBGA96	7 × 7 × 0.97	Reel	100/1000
DA14195-00R01VD2	WLCSP81	3.73 × 3.73 × 0.57	Reel	100/1000
DA14195-00R01HJ2	VFBGA96	7 × 7 × 0.97	Reel	100/1000
DA14195-00D01HJ2	VFBGA96	7 × 7 × 0.97	Reel	100/1000
DA14195-00D03VD2	WLCSP81	3.73 × 3.73 × 0.57	Reel	100/1000

Table 3. Ordering information (production)

Part number	Package	Size (mm)	Shipment form	Pack quantities
DA14195-00VD2	WLCSP81	3.73 × 3.73 × 0.57	Reel	7500
DA14195-00HJ2	VFBGA96	7 × 7 × 0.97	Reel	3000
DA14195-00D01VD2	WLCSP81	3.73 × 3.73 × 0.57	Reel	7500
DA14195-00D01HJ2	VFBGA96	7 × 7 × 0.97	Reel	3000
DA14195-00R01VD2	WLCSP81	3.73 × 3.73 × 0.57	Reel	7500
DA14195-00R01HJ2	VFBGA96	7 × 7 × 0.97	Reel	3000
DA14195-00D03VD2	WLCSP81	3.73 × 3.73 × 0.57	Reel	7500
DA14195-01D03VD2	WLCSP81	3.73 × 3.73 × 0.57	Reel	7500

Part number legend:

DA14195 RR[XXX]YYZ

RR: Chip Revision Number

XXX: Optional Family derivative

D01: Active Noise Cancelling (ANC) enabled

R01: RTX low latency Sheer Sound CODEC enabled

D03: Custom code enabled

YY: Package code

Z: Packing method (2: reel) Marking code

DA14195 RR[XXX]

4. Revision History

Revision	Date	Description
01.00	June 19, 2024	First release.

RoHS Compliance

Renesas Electronics' suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.