

## RAA271005

General Purpose IC for Power Management Automotive Applications

The [RAA271005](#) is a general-purpose Power Management IC (PMIC) suitable for R-Car SoC series.

The RAA271005 contains five DC/DC switching regulators and 6 low-drop out linear regulators (LDO). DCDC5 switching regulator can be configured to work in buck mode or can be configured as a boost. The RAA271005 PMIC supports low power operation, where three of the switching regulators (Buck3-Buck5) have been optimized to consume low quiescent current.

RAA271005 supports up to ASIL D functional safety, and includes an independent reference for monitoring of the output voltages, dual internal temperature monitors, challenge response watchdog timer, SoC and MCU error pin monitors, reset generator, a dedicated safety-control state machine, and safety shutdown path. An integrated 12-bit ADC monitors all input rails, output rails, internal temperature, and includes additional inputs to monitor external analog sources.

RAA271005 is available in a 6×11 BGA package with 0.65mm pitch. The device is offered as AEC-Q100 Grade 1 operation supporting an ambient temperature range of -40°C to 125°C.

### Applications

- Automotive gateway systems
- Automotive vision systems
- Automotive LIDAR systems
- Ideal power supply for Renesas R-Car S4 SoC

### Features

- Input voltage range 2.7V - 5.5V
- Five High efficiency switching regulators with adjustable output voltages
  - 12A (Buck1);  $V_{OUT}$  from 0.3V to 3.3V
  - 2.5A (Buck2-Buck5);  $V_{OUT}$  from 0.3V to 3.3V
  - Merge-mode 2 x 2.5A regulators = 5A
  - Buck5 can operate as asynchronous boost
- Six Linear Drop Out (LDO) Regulators
  - 4×60mA;  $V_{OUT}$  = 1.8V or 3.3V
  - 2×500mA;  $V_{OUT}$  = 0.6V to 3.3V
- Programmable current limits for all bucks
- 12-bit analog-to-digital converter for monitoring with programmable OV/UV thresholds.
- Programmable power sequence. Fully supports S4 sequence requirements.
  - Low-Iq Deep-stop/Always On (AWO) Mode
  - Suspend-to-RAM/DDR-backup Mode
- Supports R-Car Soc Activation
- Q&A watchdog timer
- Configurable through I<sup>2</sup>C or SPI interface
- SoC and MCU error pin monitors
- [AEC-Q100](#)
- Grade 1 qualified

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# 1. Overview

## 1.1 Typical Applications

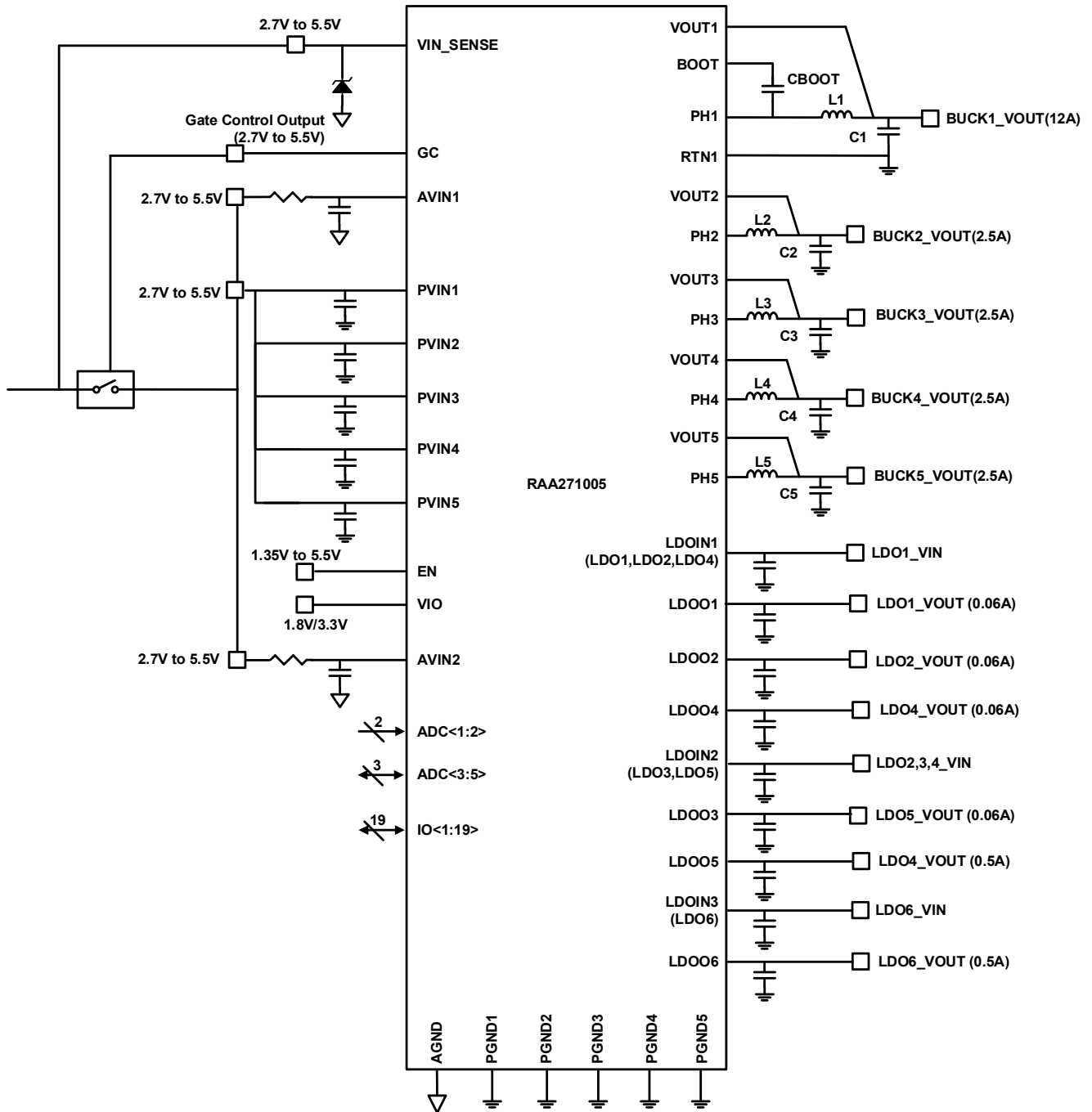


Figure 1. Typical Application with 5 Bucks

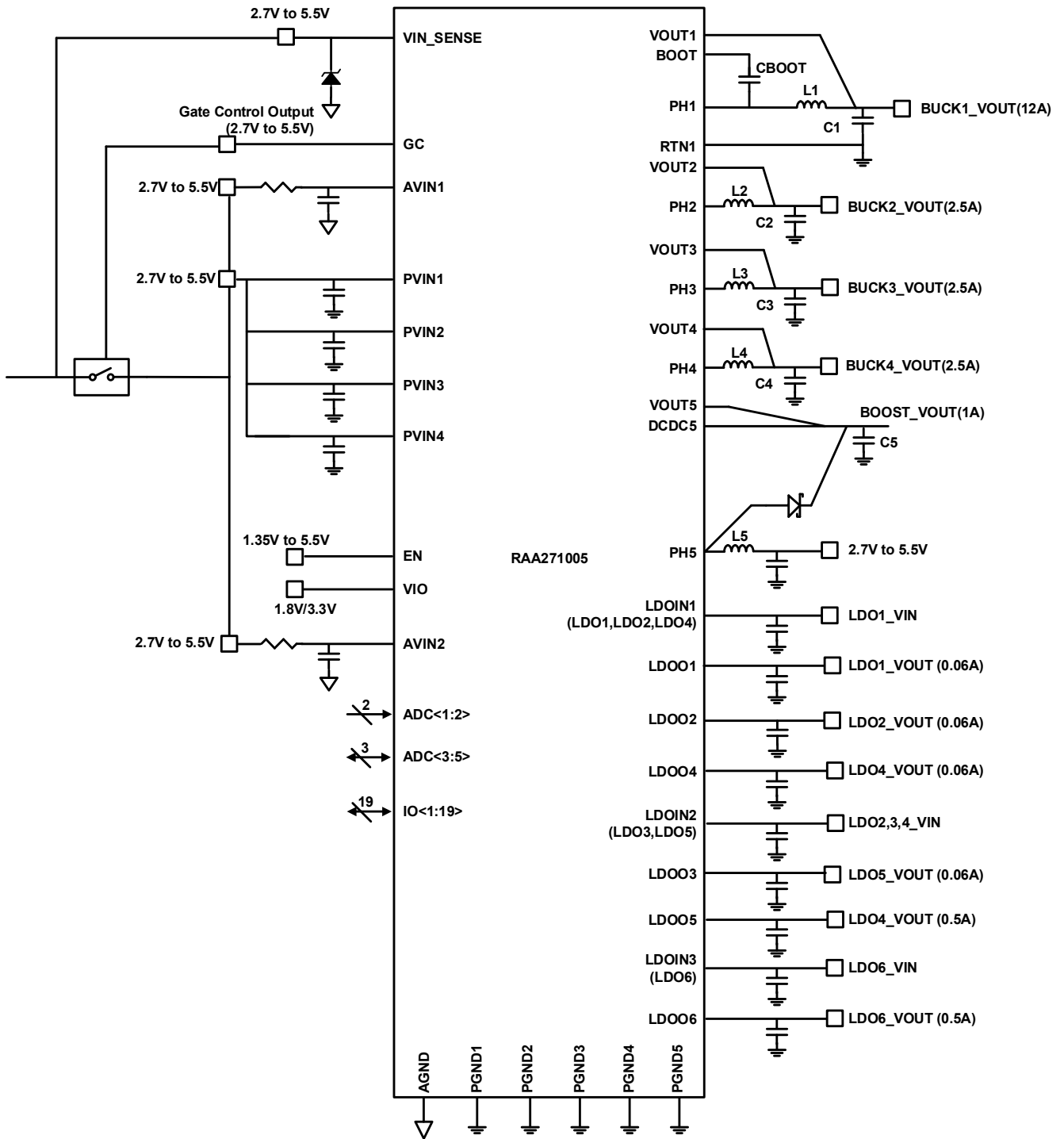


Figure 2. Typical Application with 4 Bucks + 1 Boost

## 1.2 Block Diagram

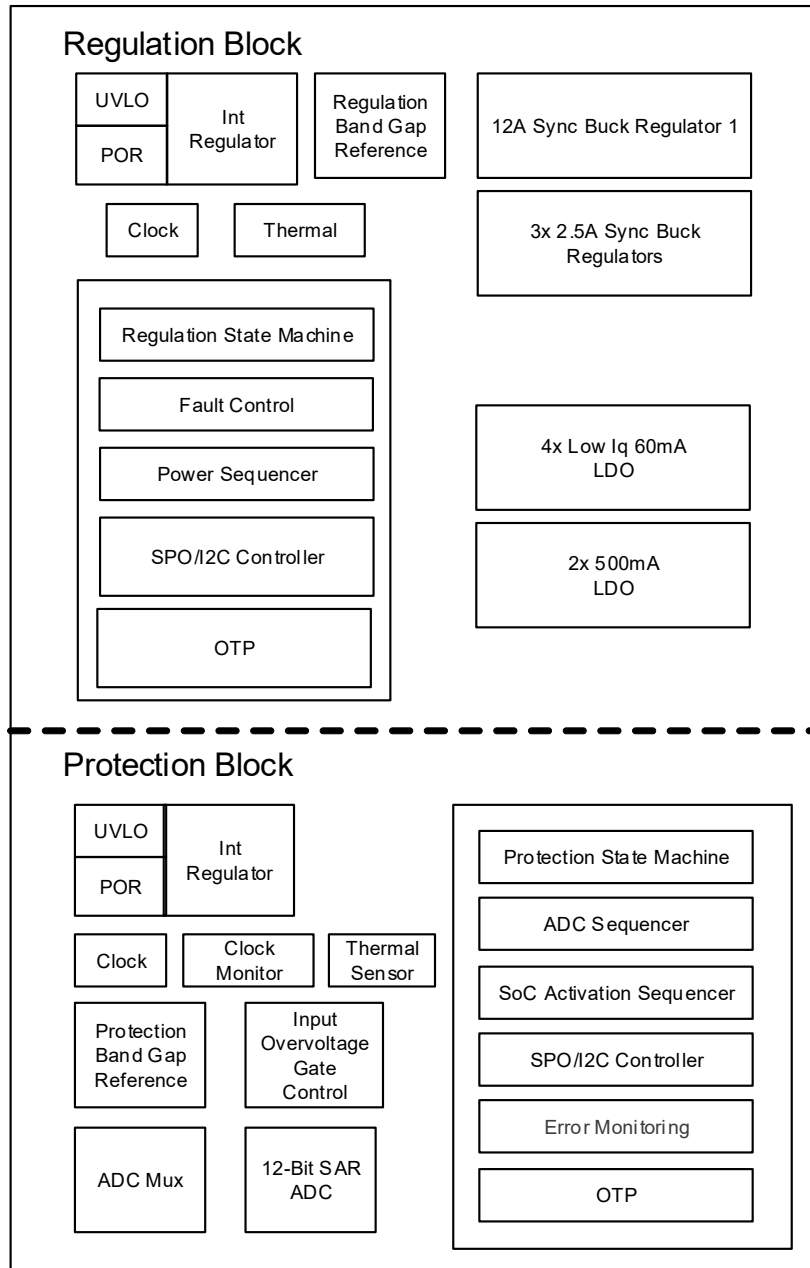


Figure 3. Simplified Block Diagram (Under Development)

## 2. Pin Information

### 2.1 Pin Assignments

	1	2	3	4	5	6
A	IO8	IO11	AGND	ADC4	AVIN2	ADC2
B	IO7	IO9	IO10	ADC5	ADC3	ADC1
C	IO17	IO12	VOUT4	VOUT5	EN	IO13
D	IO15	IO16	VOUT3	RTN1	IO18	IO4
E	PVIN4	AVIN1	LDOO5	VOUT1	IO19	PVIN5/ DCDC5
F	PH4	GC	LDOO6	VOUT2	IO14	PH5
G	PGND4	LDOO4	LDOO3	AGND	VIO	PGND5
H	PGND3	VIN_ SENSE	LDOO2	LDOO1	IO2	PGND2
J	PH3	LDOIN3	LDOIN2	IO6	IO3	PH2
K	PVIN3	BOOT	LDOIN1	IO5	IO1	PVIN2
L	PVIN1	PH1	PGND1	PGND1	PH1	PVIN1

Balls Facing Down

## 2.2 Pin Description

Pin Number	Pin Name	Pin Type	Description
A1	IO8	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.
A2	IO11	Input/Output	
A3	AGND	GND	Analog ground
A4	ADC4	Input/Output	External ADC input or ADC decoder output
A5	AVIN2	Input	Analog supply voltage 2, 2.7V to 5.5V. This should be connected to AVIN1 on PCB.
A6	ADC2	Input	External ADC input
B1	IO7	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.
B2	IO9	Input/Output	
B3	IO10	Input/Output	
B4	ADC5	Input/Output	External ADC input or ADC decoder output
B5	ADC3	Input/Output	External ADC input or ADC decoder output
B6	ADC1	Input	External ADC input
C1	IO17	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.
C2	IO12	Input/Output	
C3	VOUT4	Input	Remote sense of the output voltage of Buck 4
C4	VOUT5	Input	Remote sense of the output voltage of Buck 5.
C5	EN	Input	Chip enable
C6	IO13	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.
D1	IO15	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.
D2	IO16	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.
D3	VOUT3	Input	Remote sense of the output voltage of Buck 3
D4	RTN1	Input	Remote ground sense at the load for Buck 1
D5	IO18	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.
D6	IO4	Input/Output	
E1	PVIN4	Input	Power supply for Buck 4 power stage.
E2	AVIN1	Input	Analog supply voltage 1
E3	LDO05	Output	LDO 5 power output
E4	VOUT1	Input	Remote sense of the output voltage of Buck 1
E5	IO19	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.
E6	PVIN5/ DCDC5	Input	Power supply for Buck 5 power stage.
F1	PH4	Output	Switching node for Buck 4 power stage.
F2	GC	Output	Gate control
F3	LDO06	Output	LDO 6 power output
F4	VOUT2	Input	Remote sense of the output voltage of Buck 2
F5	IO14	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.

Pin Number	Pin Name	Pin Type	Description
F6	PH5	Output	Switching node for Buck 5 power stage.
G1	PGND4	GND	Ground connection for Buck 4 power stage.
G2	LDOO4	Output	LDO 4 power output
G3	LDOO3	Output	LDO 3 power output
G4	AGND	GND	Analog ground
G5	VIO	Input	I/O Supply Voltage
G6	PGND5	GND	Ground connection for Buck 5 power stage.
H1	PGND3	GND	Ground connection for Buck 3 power stage.
H2	VIN_SENSE	Input	Input voltage monitoring pin for input over voltage protection gate control
H3	LDOO2	Output	LDO 2 power output
H4	LDOO1	Output	LDO 1 power output
H5	IO2	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.
H6	PGND2	GND	Ground connection for Buck 2 power stage.
J1	PH3	Output	Switching node for Buck 3 power stage.
J2	LDOIN3	Input	LDO 6 power input
J3	LDOIN2	Input	LDO 3 & 5 power input
J4	IO6	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.
J5	IO3	Input/Output	
J6	PH2	Output	Switching node for Buck 2 power stage.
K1	PVIN3	Input	Power supply for Buck 3 power stage.
K2	BOOT	Input	Supply for boosted gate drive for Buck 1
K3	LDOIN1	Input	LDO 1, 2 & 4 power input
K4	IO5	Input/Output	Refer to IO Pin configuration table for programmability and descriptions.
K5	IO1	Input/Output	
K6	PVIN2	Input	Power supply for Buck 2 power stage.
L1	PVIN1	Input	Power supply for Buck 1 power stage.
L2	PH1	Input	Switching node for Buck 1 power stage.
L3	PGND1	GND	Ground connection for Buck 1 power stage.
L4	PGND1	GND	Ground connection for Buck 1 power stage.
L5	PH1	Output	Switching node for Buck 1 power stage.
L6	PVIN1	Input	Power supply for Buck 1 power stage.



## 2.2.1 IO Pin Assignments

Table 1. IO Pin configuration table

Pin Mode	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8	IO9	IO10	IO11	IO12	IO13	IO14	IO15	IO16	IO17	IO18	IO19
0x0	SCK	SS_B2	SS_B	MOSI	MISO	PGOOD	SDI1	PRESET#	SDO1	SDO2	PRESET OUT	SDI2	EXTPOC#	IRQ#	SDI3	SDI4	PWR_CTRL1	PWR_CTRL2	BKUP
0x1	SCL	SDA	GPIO1	GPIO2	GPIO3	PGOOD	SDI1	PRESET#	SDO1	SDO2	PRESET OUT	SDI2	EXTPOC#	IRQ#	SDI3	SDI4	PWR_CTRL1	PWR_CTRL2	BKUP

## 2.2.2 IO Pin Descriptions

IO Name	Type	Description
PGOOD	Output	Power Good signal to R-Car S4
SDI1 / ERROROUT	Input	R-Car S4 Error Notification Signal
PRESET#	Output	Reset Signal sent to R-Car S4
SDO1 / STB_N*	Output	Standby Control Signal for CAN transceiver
SDO2 / SSP*	Output	Secondary Safety Path Signal
EXTPOC	Output	External Power on Clear Input to the R-Car S4
IRQ#*	Output	Interrupt signal to R-Car S4
PWR_CTRL1,2	Input	Power Control inputs from the R-Car S4 to sequence certain rails
PRESETOUT	Input	Reset notification signal from R-Car S4 SoC
SDI2 / VMONOUT0	Input	Digital CVM Error signal notification from R-Car S4 SoC
SDI3 / VMONOUT1	Input	Digital CVM Error signal notification from R-Car S4 MCU
SDI4	Input	Safety Defined Input
BKUP	Output	Signal indicating the turn-off of non-memory and non-AWO rails in suspend to RAM mode
SS_B, SS_B2	Input	SPI Slave select signals
SCK	Input	SPI clock signal
MOSI	Input	SPI Master Output Slave Input Signal
MISO	Output	SPI Master Input Slave Output Signal
SCL	Input	I2C Clock Signal
SDA	Input/ Output	I2C Data Signal
GPIOx*	Input/ Output	General Purpose IO

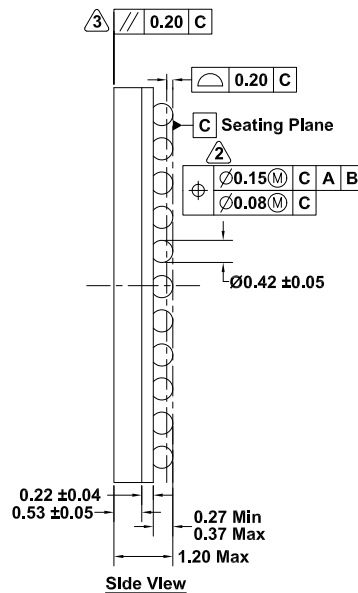
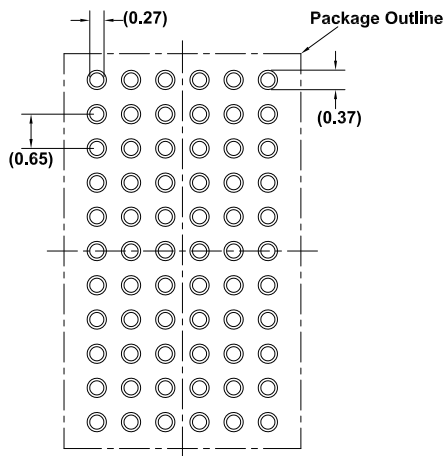
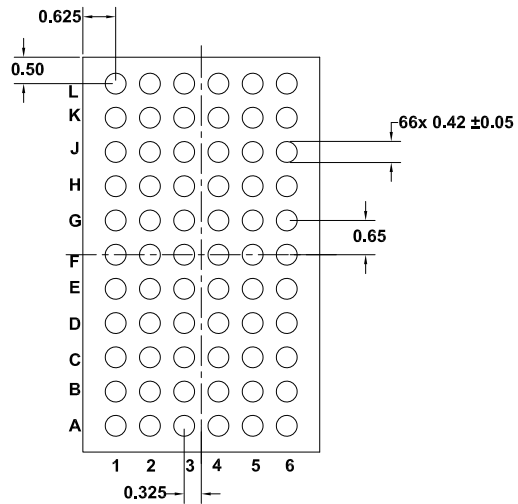
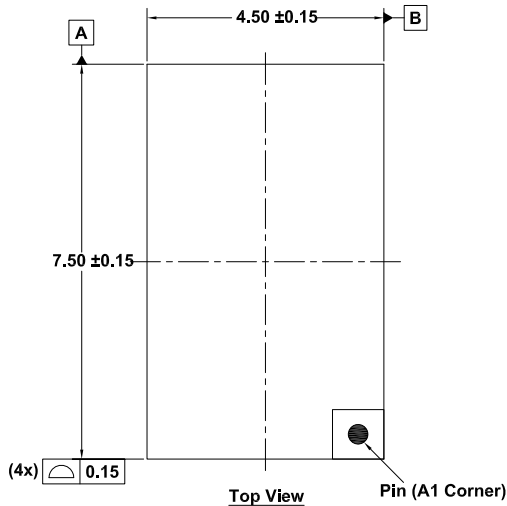
### 3. Package Outline Drawing

For the most recent package outline drawing, see [V66.4.50x7.50](#).

V66.4.50x7.50

66 Low Profile Ball Grid Array Package (LFBGA)

Rev 0, 5/2021



**Notes:**

1. All dimensions and tolerances conform to ASME Y14.5 - 2009.
- ② Datum C (Seating Plane) is defined by the spherical crowns of the solder balls.
- ③ Parallelism measurement shall exclude any effect of mark on top surface of package.
4. Unless otherwise specified, dimensions are in millimeters.

## 4. Revision History

Revision	Date	Description
1.00	Sep 27, 2021	Initial release.

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