

## SC14446A, SC14447A

1.8 V Single Chip for ZBS DECT with RFPA, QSPI, EBI, GPU

This short datasheet is an addendum to the SC14446A, SC14447A datasheet.

The SC14446A, SC14447A are a family of digital CMOS ICs with fully integrated radio transceivers including RF Power Amplifier and baseband processors for Zero Blind Slot (ZBS) DECT & DECT 6.0 CATiQ, Japanese and Korean DECT handsets and base stations supporting extended temperature range.

### Key Features

- Complies with DECT ETS 300 175-2,3 & 8 and DECT 6.0 and Korean DECT (1.7 GHz)
- DCXO for 10.368 MHz/20.736 MHz, 12 MHz (USB only) XTAL with low power mode
- Processing power
  - 82.944 MHz 16 bit CompactRISC™ CR16Cplus with up to 16 kB instruction and data cache
  - Four-channel DMA controller
  - Dual \*) 82.944 MHz Programmable Gen2DSP with Micro Code ROM and Micro Code RAM
  - 82.944 MHz enhanced Graphics Processing Unit
  - DiP Processor supporting CAQ-iq with fast FP search instructions
  - MMU for Extended address range up to 128 MB
- Development/Debug support
  - Serial Debug interface, Nexus Class-1 compliant
  - Performance Timer for Gen2DSP and CR16C
  - Instruction/Data/Event Trace unit
  - Gen2DSP debugger with 2 ch MCROM patching
- Memories
  - 16/2/2 kB Cache/Admin/Trace RAM
  - 24/32 kB, 24/32 kB Shared RAM1/2, ROM1/2
  - 2/16 kB, 96/96 kB MCGRAM1/2, oMCROM1/2
- Power management
  - 1.9 V to 3.45 V operating range
  - 1.8 V operating voltage with 1.8 V to 3.45 V I/O
  - USB Charge control for 2x NiMH and Li-Ion (\*)
  - Dual DCDC converter (boost/buck, boost)
    - Ultra-low power mode (ULP) module to support DECT ULE standard and ULS phones
- Battery voltage comparator with interrupt
- Analog and Audio Interfaces
  - Full dual 8, 16, 32 kHz 16-bit audio CODEC
  - Analog Front End to differential and single ended microphones and 28 Ω
  - CLASS-D amplifier Stereo (2x 8 Ω)/Mono (4 Ω) up to 32 kHz/48 kHz
  - 10 bit ADC for line interface, battery voltage, temperature sensor, headset detection, 4 wire resistive touch screen
  - Opamps for caller-id, ringing, par. set detection
- Digital interfaces
  - 82.944 MHz External Bus Interface to mDDR or Static Memory and PSRAM
  - 41.472 MHz 16 bits wide I/O LCD/Camera bus
  - USB 2.0 FS/LS MAC + PHY with DMA support and USB Battery Charging Specification V1.2
  - 82.944 MHz 1.8 V to 3.3 V Quad SPI interface for serial FLASH with erase suspend/resume support for EEPROM function and CAT-iQ SUOTA
  - General purpose I/O 8 bit ports
  - Keyboard interface with debounce counter
  - Dual UART Full duplex 9600 Bd to 230.4 kBd
  - Dual SPI+™ interface 20.736 MHz (incl. 9 bits)
  - Dual ACCESS bus 100 kHz, 400 kHz, 1.152 MHz
  - PCM+ Interface, M/S, 12x 8 bits, 48 kHz, I2S
- Three general purpose timers. enhanced watch dog
- Radio transceiver
  - Integrated 1.9 GHz/1.7 GHz CMOS transceiver
  - RF PLL lock time: 17 μs typ.
  - Four digital output ports (including two for fast antenna diversity switching)
  - -96 dBm receiver sensitivity
- Integrated 1.9 GHz PA for DECT and Korean DECT
  - High Power Mode EU (HPM): 25.5 dBm
  - High Power Mode USA (HPM): 23.5 dBm
  - Low Power Mode (LPM): 12 dBm
  - "Green" Mode (GPM): 4 dBm

- Low Radiation Mode (LRM): -35 dBm
- Output power ramp and flatness control
- LGA206 and VFBGA113 packages
- Extended temperature range -40 °C to +85 °C

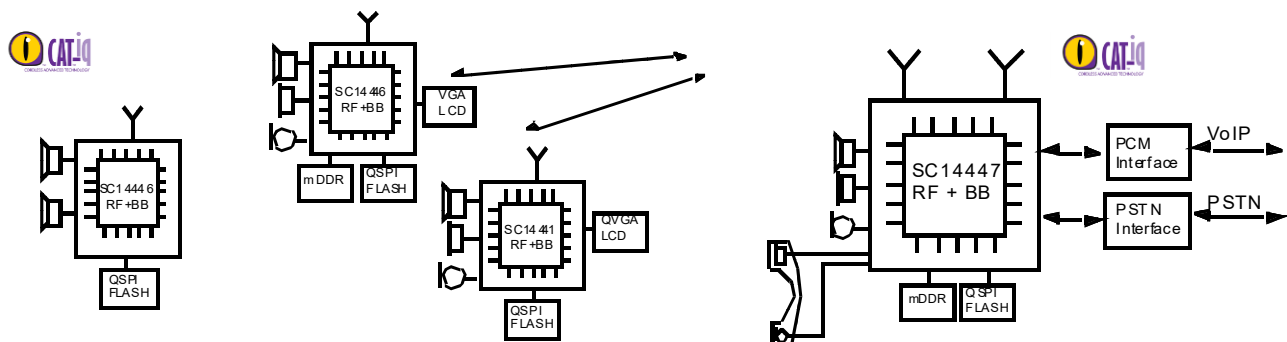


Figure 1. System diagram

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## 1. Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a maximum temperature of 30°C and a maximum relative humidity of 60% RH before the solder reflow process.

The LGA packages are qualified for MSL 4.

**Table 1. MSL classification**

MSL level	Floor lifetime
MSL 4	72 hours
MSL 3	168 hours
MSL 2A	4 weeks
MSL 2	1 year
MSL 1	Unlimited at 30 °C/85% RH

### 1.1 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from <http://www.jedec.org>.

## 2. Package Outline Drawings

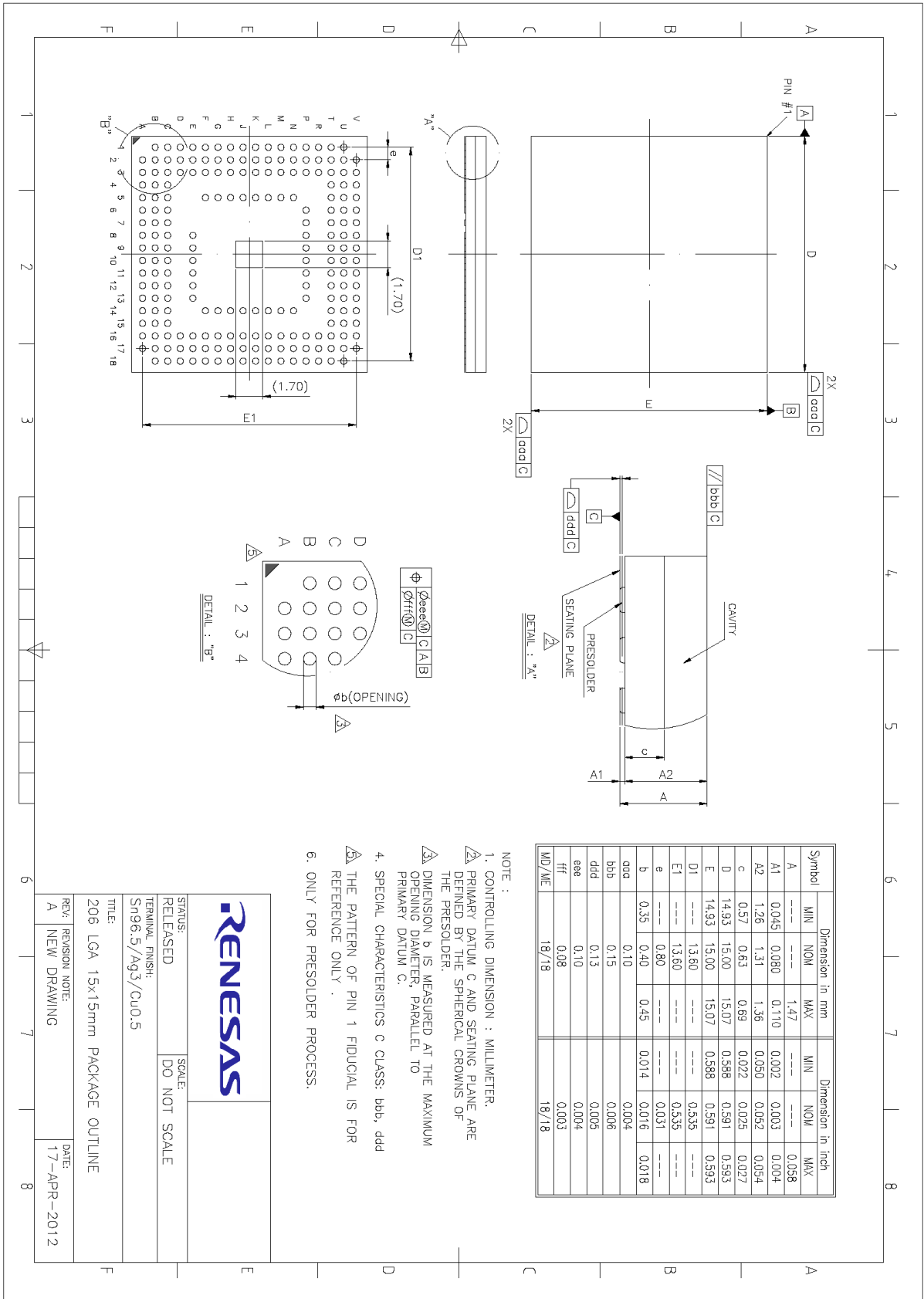


Figure 2. LGA206 package outline drawing

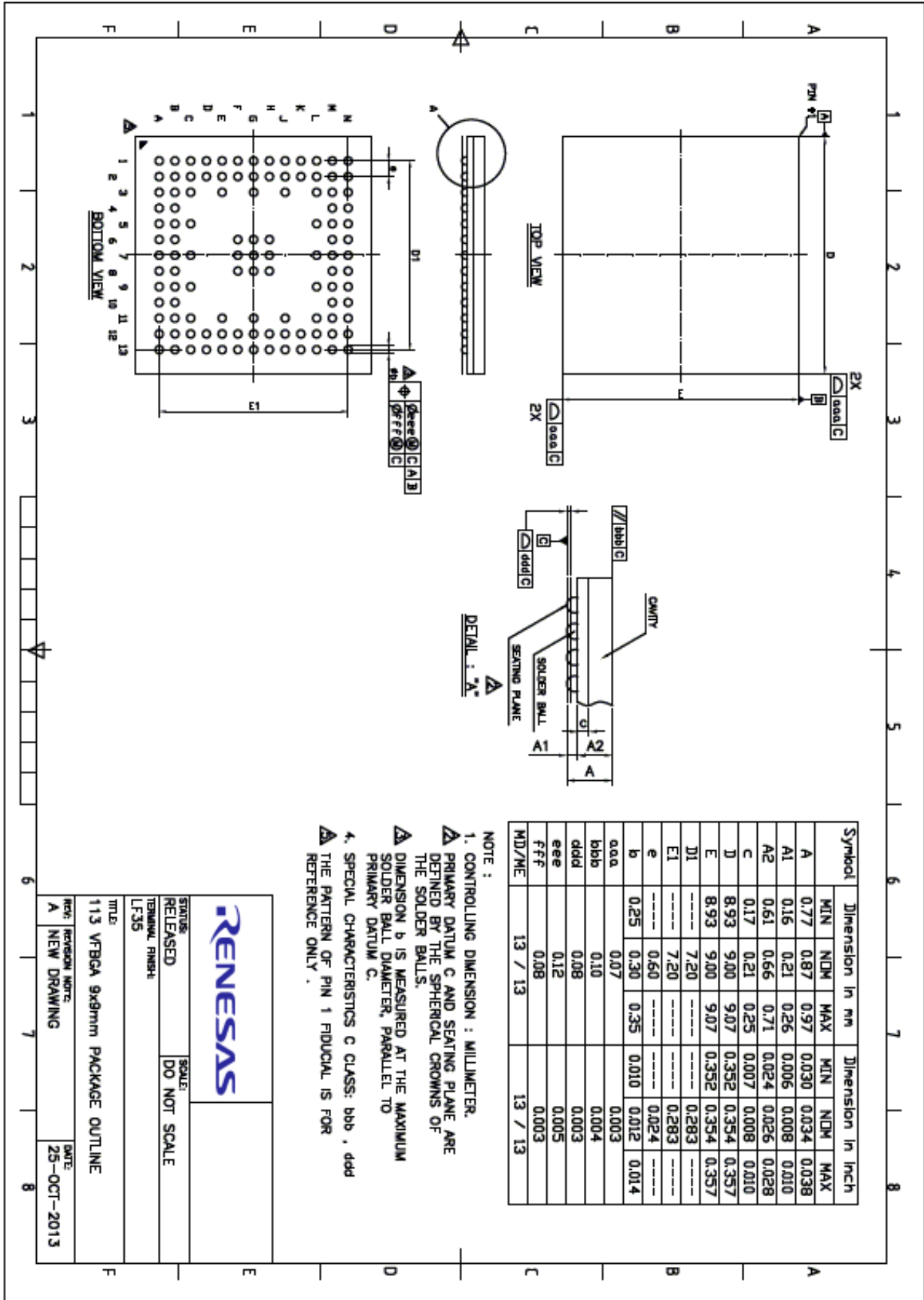


Figure 3. VFBGA113 package outline drawing

### 3. Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult your Renesas local sales representative.

**Table 2. Ordering information**

Part number	Package	Size (mm)	Shipment form	Pack quantity
SC14446A76R101LVPT	LGA206 package	15 x 15	Tray	MOQ 1260
SC14446A76R101USCT	VFPGA113 package	9 x 9	Tray	MOQ 2600
SC14447A76R101LVPT	LGA206 package	15 x 15	Tray	MOQ 1260



## 4. Revision History

Revision	Date	Description
01.00	June 26, 2024	First release.

### RoHS Compliance

Renesas Electronics' suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.