Understanding the Differences in ESD Device-Level Testing

Electrostatic discharge (ESD) is defined as the sudden and momentary electric current that flows between two objects at different electrical potentials. ESD causes equipment failure and network downtime, therefore, causing production losses of multiple billion dollars annually. From portable consumer electronics to industrial automation and process control systems, to military and aerospace applications, every electronics manufacturer must consider ESD during equipment design. To address the wide range of technical requirements in industrial segments, a myriad of testing standards exists today.

This application note explains the differences between the main ESD device level tests according to the Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM).

Contents

1. Human Body Model (HBM)

The human body model (HBM) device-level test is the most commonly used model for ESD testing. It characterizes the susceptibility of an electronic component to ESD damage. The test simulates an electrical discharge of a human onto an electronic component, which could occur if a human has built up residual charge (such as by dragging feet across a carpet with socks on) and touches an electronic device. The failure modes for the HBM testing of integrated circuits typically consist of junction damage, metal penetration, melting of metal layers, contact spiking, and damage to the gate oxides.

The test procedure is set up by applying a high-voltage supply in series with a 1MΩ resistor and a 100pF capacitor. After the capacitor is fully charged, the capacitor is removed from the high-voltage supply and series resistor and applied in series with a 1.5kΩ resistor and the device-under-test (DUT) through the use of a switch. Therefore, the voltage is fully dissipated through the resistor and DUT. Figure 1 is a representation of the circuit previously described. Values for the high-voltage supply vary according to the test level between 0.5kV and 15kV.

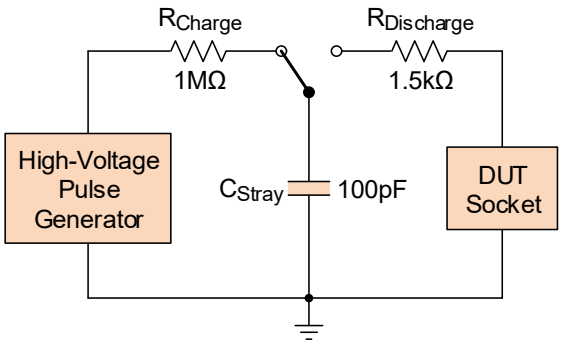

Figure 1. Human Body Model

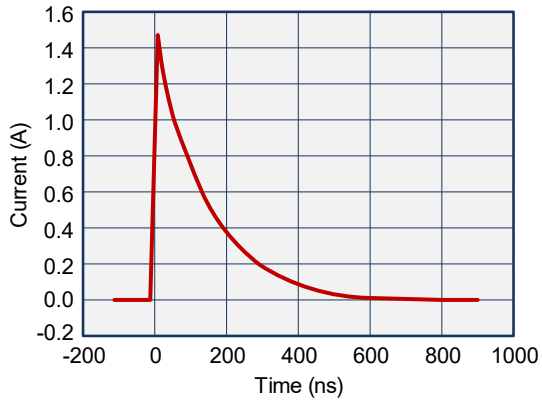

Figure 2. ESD Current During a HBM Discharge

Figure 2 shows a typical oscilloscope readout with an initial current spike of up to 1.4A to 1.5A when the capacitor starts discharging, and the ramp-down until it asymptotically approaches 0A at approximately 500ns. Under test experiences at a single discharge event, the maximum power (Power [W] = Current [A] × Voltage [V]) of the device is 22.5kW on a traditional human body model test.

2. Machine Model (MM)

The machine model (MM) device-level test is less common these days and was first developed in the 1990s. Industrial automation manufacturing sites became increasingly popular at this time to increase output. These machines would become electrically charged after turning on, and the machine would discharge into an electronic component after contact was made. Therefore, MM was made as a test to model this type of ESD event. The failure modes typically seen in MM are similar to the human body model, such as junction damage, melting of the metal layers, and damage to the gate oxides.

The test procedure for MM is set up with a high-voltage supply in series with a resistor and a 200pF capacitor. After the capacitor is fully charged, the capacitor is removed from the high-voltage supply and series resistor and applied in series to a 0.5µH inductor and the device under test (DUT) through the use of a switch. The inductor with the capacitor voltage is dissipated through the DUT. Figure 3 is a representation of the MM test circuit. Traditional values for the high voltage supply can vary, but the most common range from 50V up to 400V.

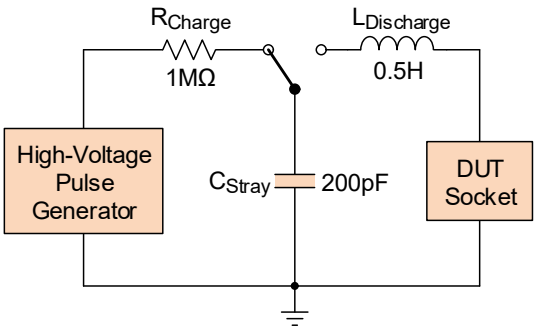

Figure 3. Machine Model

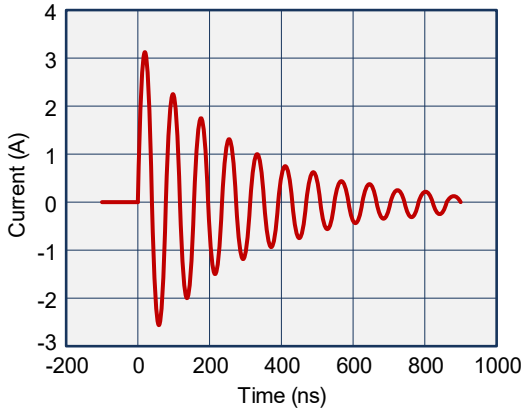

Figure 4. ESD Current During a MM Discharge

When looking at an oscilloscope measurement of current over time (Figure 4), one notices that the R-L-C circuit scenario creates an alternating current. The current reaches around ±3A, which is about four times higher than the peak-to-peak current amplitude of HBM. Furthermore, the dissipation is much longer for the MM, as it is still asymptotically approaching 0A at 900ns. Figure 4 shows a typical scope shot. The maximum power dissipation the DUT experiences during an MM discharge event is around 1.2kW.

Also, an interesting part about MM is that it requires each pin on the DUT to be tested exactly to its standard. The electronic chip is mounted on a specially designed load board that interfaces with an automated ESD tester. Each pin is individually tested while the other pins on the board are grounded. This procedure is carried out until all pins have been tested. Figure 5 provides a graphical image of how the test is carried out.

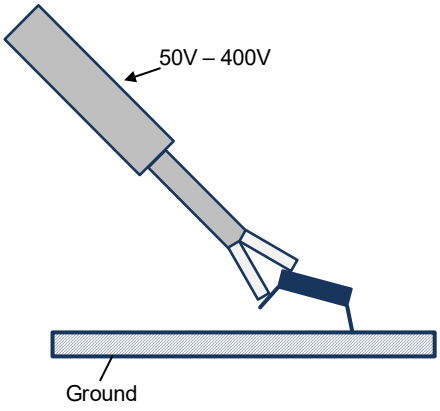

Figure 5. Applying a MM Discharge to a Component

3. Charged Device Model (CDM)

The charged device model (CDM) device-level testing procedure is a simulation of what often happens in an automated manufacturing environment. In this type of environment, machines are known to stay on for an indefinite amount of time. This results in the electronic ICs becoming electrically charged over time. When the part comes into contact with a grounded conductor, the built-up residual capacitance becomes discharged. For the CDM test, the DUT is placed on its back facing upward on a testing board.

The metal field plate and the DUT are separated by an insulating material, which acts as a capacitor between the two objects. The metal field plate is then connected to a high-voltage supply and raised to the required CDM test voltage level. A probe then comes into proximity to the specific pin under test where an ESD event occurs, which is verified by monitoring the ground connection of the pin under test. This test is repeated on each pin on the DUT for three positive and three negative pulses, resulting in six total discharges per pin. Figure 6 shows the equivalent circuit of the charged device model.

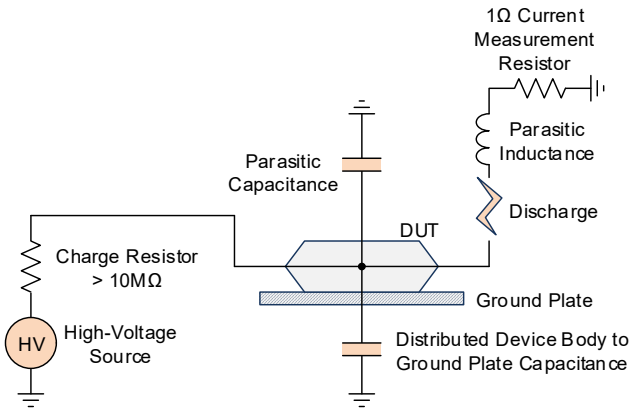

Figure 6. Charged Device Model

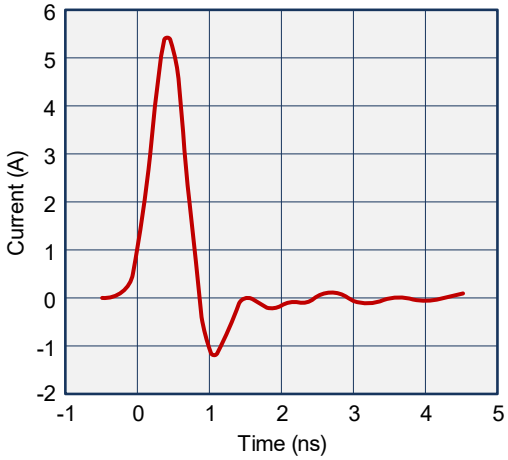

Figure 7. ESD Current During a CDM Discharge

The scope shot in Figure 7 indicates that the CDM discharge is an extremely fast transient. It takes place over a couple of nanoseconds at most, which makes it difficult to test and to model. The result of this test is a high current of 5A to 6A being discharged in less than 1ns. The current has already dissipated by 5ns, making this a succinct, but also volatile test on the device. Because of this fast transient, the failure modes typically seen in CDM tests are gate oxide damage, charge trapping, and junction damage. Figure 7 shows the current waveform during a CDM test.

4. Conclusion

The HBM, MM, and CDM are the most commonly used ESD device-level testing procedures for electronic components. Table 1 summarizes their similarities and differences.

Table 1. ESD Test Comparison

Model	Test Levels (Volts)	Peak Current (A)	Pulse Width (ns)	Rise Time	Typical ESD Failures
HBM	2kV, 4kV, 8kV, 15kV	1.5	Approximately 150	2 to 10ns	Junction Damage, Metal Penetration, Metal Melt, Contact Spiking
MM	100V, 150V, 200V	±3	Approximately 80	Approximately 1ns	Junction Damage, Metal Melting, Gate Oxide Damage
CDM	250V, 500V, 750V, 1kV	5-6	Approximately 1	Less than 400ps	Gate Oxide Damage, Charge Trapping, Junction Damage

5. Revision History

Revision	Date	Description
1.00	May 17, 2022	Initial release.

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(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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